| REVISIONS | | | |
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| LTR | DESCRIPTION | DATE | APPROVED |
| | | | |

Prepared in accordance with ASME Y14.24

Vendor item drawing

| | | | | | | | | | | | | | | | | | | | | | |
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| **REV STATUS OF PAGES** | **REV** | | | | | | | | | | | | | | | | | | | | |
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|---|---|---|
| **PMIC N/A** | **PREPARED BY**<br>RICK OFFICER | **DLA LAND AND MARITIME**<br>**COLUMBUS, OHIO 43218-3990**<br>**http://www.dla.mil/landandmaritime** |
| Original date of drawing<br>YY-MM-DD<br>17-12-01 | **CHECKED BY**<br>RAJESH PITHADIA<br>**APPROVED BY**<br>CHARLES F. SAFFLE | TITLE<br>MICROCIRCUIT, LINEAR, 0.1 GHz to 3.0 GHz, 1 dB LSB, 5 BIT, GaAs DIGITAL STEP ATTENUATOR, MONOLITHIC SILICON |
| | **SIZE** A / **CODE IDENT. NO.** 16236 | **DWG NO.** **V62/17617** |
| | **REV** | **PAGE** 1 **OF** 14 |

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V012-18

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 0.1 GHz to 3.0 GHz, 1 dB least significant bit (LSB), 5 bit, gallium arsenide (GaAs) digital step attenuator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/17617 | - | 01 | X | E |
|---|---|---|---|---|
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| Device type | Generic | Circuit function |
|---|---|---|
| 01 | HMC470A-EP | 0.1 GHz to 3.0 GHz, 1 LSB, 5 bit, GaAs digital step attenuator |

1.2.2 Case outline(s). The case outline(s) are as specified herein.

| Outline letter | Number of pins | JEDEC PUB 95 | Package style |
|---|---|---|---|
| X | 16 | MO-220-VEED-4 | Lead frame chip scale package |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| F | Tin-lead alloy (BGA/CGA) |
| Z | Other |

1.3 Absolute maximum ratings. 1/

Supply voltage ($V_{DD}$) ..... 7 V
Digital control input voltage ..... -1 V to $V_{DD}$ + 1 V
RF input power 2/:
(All attenuation states, f = 250 MHz to 3 MHz, $T_{CASE}$ = 85°C)
$V_{DD}$ = 3 V ..... 25 dBm
$V_{DD}$ = 5 V ..... 27 dBm
Continuous power dissipation ($P_D$) : 3/
$T_{CASE}$ = 85°C ..... 0.5 W
$T_{CASE}$ = 125°C ..... 0.19 W
Junction temperature range ($T_J$) ..... 150°C
Storage temperature range ($T_{STG}$) ..... -65°C to +150°C
Reflow 4/ (moisture sensitivity level 3 (MSL3) rating) ..... 260°C
Thermal resistance, junction to case ($\theta_{JC}$) ..... 130°C/W 5/ 6/
Thermal resistance, junction to ambient ($\theta_{JA}$) ..... 297°C/W 5/
Electrostatic discharge (ESD) rating:
Human body model (HDM) ..... 250 V (class 1A)

1.4 Recommended operating conditions. 7/

Supply voltage range ($V_{DD}$) ..... 3 V to 5 V
Operating case temperature range ($T_C$) ..... -55°C to +125°C

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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ For power derating at frequencies less than 250 MHz, see figure 3.
3/ See figure 4.
4/ See the ordering guide in the manufacturer’s datasheet for more information.
5/ Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with five thermal vias. See JEDEC JESD-51.
6/ The device is set to maximum attenuation state.
7/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at https://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Power derating at frequencies less than 250 MHz graph. The power derating at frequencies less than 250 MHz graph shall be as shown in figure 4.

3.5.5 Maximum power dissipation versus case temperature graph. The maximum power dissipation versus case temperature graph shall be as shown in figure 5.

3.5.6 Digital control input interface circuit. The digital control input interface circuit shall be as shown in figure 6.

3.5.7 RF1, RF2 interface circuit. The RF1, RF2 interface circuit shall be as shown in figure 7.

3.5.8 Input P0.1 dB versus frequency at minimum attenuation state for various temperatures graph with supply voltage at 5 V. The input P0.1 dB versus frequency at minimum attenuation state for various temperatures graph with supply voltage at 5 V shall be as shown in figure 8.

3.5.9 Input P0.1 dB versus frequency at minimum attenuation state for various temperatures graph with supply voltage at 3 V. The input P0.1 dB versus frequency at minimum attenuation state for various temperatures graph with supply voltage at 3 V shall be as shown in figure 9.

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Frequency range | | | 25°C | 01 | 0.1 | 3.0 | GHz |
| Insertion loss | | 0.1 GHz to 1.5 GHz | 25°C | 01 | 1.3 typical | | dB |
| | | | | | | 1.6 | |
| | | 1.5 GHz to 2.3 GHz | | | 1.5 typical | | |
| | | | | | | 1.8 | |
| | | 2.3 GHz to 3.0 GHz | | | 1.7 typical | | |
| | | | | | | 2.0 | |
| Attenuation control range | | Between minimum and maximum attenuation states, 0.1 GHz to 3.0 GHz | 25°C | 01 | 31 typical | | dB |
| Attenuation step size | | Between any successive attenuation states, 0.1 GHz to 3.0 GHz | 25°C | 01 | 1 typical | | dB |
| Attenuation step error | | Between any successive attenuation states, 0.1 GHz to 33 GHz | 25°C | 01 | $< \pm 0.2$ typical | | dB |
| Attenuation state error | | Referenced to insertion loss state, all attenuation states, 0.1 GHz to 2.3 GHz | 25°C | 01 | -(0.3 + 2% of attenuation state) | +(0.3 + 2% of attenuation state) | dB |
| | | Referenced to insertion loss state, 1 dB to 15 dB attenuation states, 2.3 GHz to 3.0 GHz | | | -(0.3 + 3% of attenuation state) | +(0.3 + 3% of attenuation state) | |
| | | Referenced to insertion loss state, 16 dB to 31 dB attenuation states, 2.3 GHz to 3.0 GHz | | | -(0.3 + 6% of attenuation state) | +(0.3 + 6% of attenuation state) | |
| Return loss | | RF1 and RF2 pins, all attenuation states, 0.1 GHz to 3.0 GHz | 25°C | 01 | 14 typical | | dB |
| Relative phase | | Between minimum and maximum states, 0.1 GHz to 1.5 GHz | 25°C | 01 | 12 typical | | Degrees |
| | | Between minimum and maximum states, 1.5 GHz to 3.0 GHz | | | 27 typical | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Switching characteristics. Between all attenuation states. | | | | | | | |
| Rise and fall time | $t_{RISE}$, $t_{FALL}$ | 10% to 90% of RF output | 25°C | 01 | 50 typical | | ns |
| On and off time | $t_{ON}$, $t_{OFF}$ | 50% $V_{CTL}$ to 90% of RF output | 25°C | 01 | 70 typical | | ns |
| Input linearity, 3/ 0.1 dB compression | P0.1dB | All attenuation states, 250 MHz to 3.0 GHz, $V_{DD}$ = 3 V | 25°C | 01 | 25 typical | | dBm |
| | | All attenuation states, 250 MHz to 3.0 GHz, $V_{DD}$ = 5 V | | | 27 typical | | |
| Input linearity, 3/ third order intercept | IP3 | 10 dBm per tone, 1 MHz spacing | 25°C | 01 | 50 typical | | dBm |
| Supply current | $I_{DD}$ | | 25°C | 01 | 1.7 typical | | mA |
| Digital control inputs. | | V1 to V5 pins | | | | | |
| Low voltage | $V_{INL}$ | | 25°C | 01 | 0 | 0.8 | V |
| High voltage | $V_{INH}$ | | 25°C | 01 | 2.0 | $V_{DD}$ | V |
| Low current | $I_{INL}$ | | 25°C | 01 | 1 typical | | µA |
| High current | $I_{INH}$ | | 25°C | 01 | 40 typical | | µA |

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, $V_{DD}$ = 3 V to 5 V, V1 to V5 control pins voltage ($V_{CTL}$) = 0 V or $V_{DD}$, $T_{CASE}$ = 25°C, 50 Ω system.

3/ Input linearity performance degrades at frequencies less than 250 MHz; see figure 8 and figure 9.

Case X

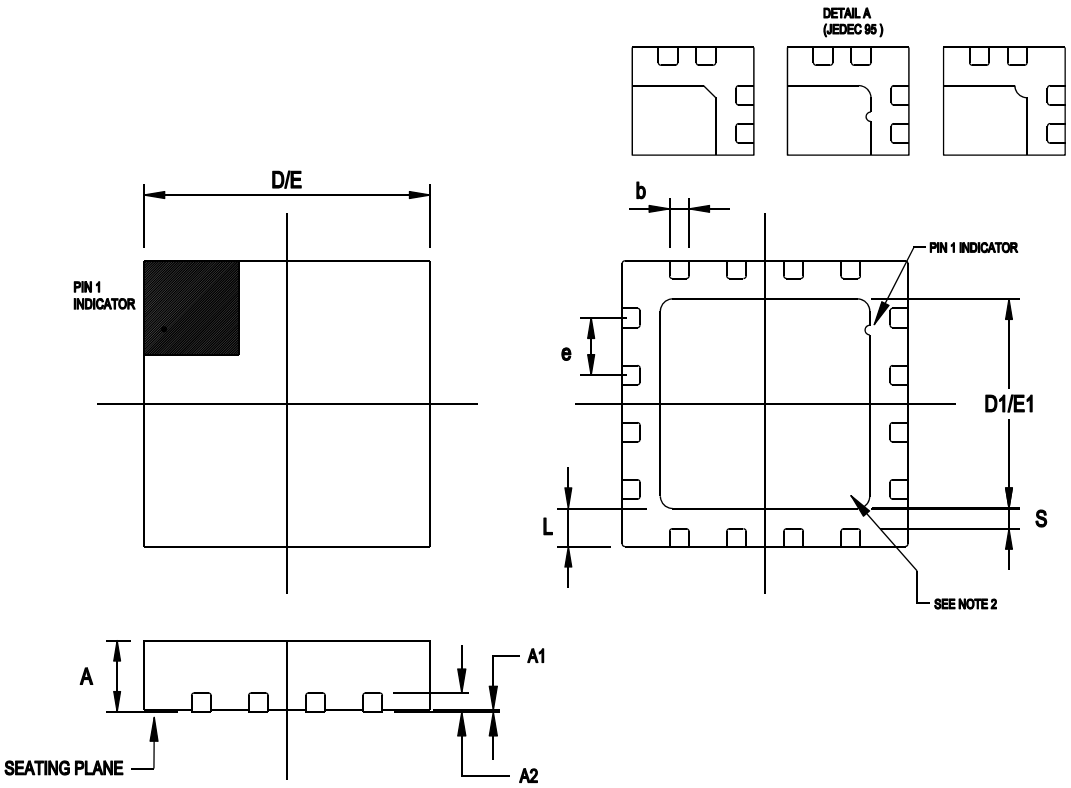


FIGURE 1. Case outline.

| DLA LAND AND MARITIME<br>COLUMBUS, OHIO | SIZE<br>A | CODE IDENT NO.<br>16236 | DWG NO.<br>V62/17617 |
|---|---|---|---|
| | | REV | PAGE 7 |

| Symbol | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Inches | | | Millimeters | | |
| | Minimum | Nominal | Maximum | Minimum | Nominal | Maximum |
| A | .0314 | .0334 | .0354 | 0.80 | 0.85 | 0.90 |
| A1 | .0031 COPLANARITY | .0007 | .0019 | 0.08 COPLANARITY | 0.02 | 0.05 |
| A2 | .0079 REF | | | 0.203 REF | | |
| b | .0078 | .0098 | .0118 | 0.20 | 0.25 | 0.30 |
| D/E | .1141 | .1181 | .1220 | 2.90 | 3.00 | 3.10 |
| D1/E1 | .0629 | .0669 | .0708 | 1.60 | 1.70 | 1.80 |
| e | .0196 BSC | | | 0.50 BSC | | |
| L | .0137 | .0157 | .0177 | 0.35 | 0.40 | 0.45 |
| S | .0078 | --- | --- | 0.20 | --- | --- |

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
3. Falls within reference to JEDEC MO-220-VEED-4.

FIGURE 1. Case outline - Continued.

| Device type | 01 | |
|---|---|---|
| Case outline | X | |
| Terminal number | Terminal symbol | Description |
| 1 | $V_{DD}$ | Power supply. See figure 6 for the interface schematic. |
| 2 | RF1 | RF input or output of the attenuator. The RF1 pin is dc coupled to $V_{DD}$ and ac matched to 50 Ω. An external dc blocking capacitor is required. Select the capacitor value for the lowest frequency of operation. See figure 7 for the interface schematic. |
| 3 | NIC | Not internally connected. These pins are not internally connected; however, all data shown herein was measured when these pins were connected to the RF/dc ground of the evaluation board. |
| 4 | ACG1 | AC grounding capacitor pins. Leave these pins not connected when operating above 700 MHz. For frequencies less than 700 MHz, connect capacitors larger than 100 pF as close to the ACGx pins as possible. |
| 5 | ACG2 | |
| 6 | ACG3 | |
| 7 | ACG4 | |
| 8 | ACG5 | |
| 9 | ACG6 | |
| 10 | NIC | Not internally connected. These pins are not internally connected; however, all data shown herein was measured when these pins were connected to the RF/dc ground of the evaluation board. |
| 11 | RF2 | RF input or output of the attenuator. The RF2 pin is dc coupled to $V_{DD}$ and ac matched to 50 Ω. An external dc blocking capacitor is required. Select the capacitor value for the lowest frequency of operation. See figure 7 for the interface schematic. |
| 12 | V1 | Parallel control voltage inputs. These pins select the required attenuation see figure 3. See figure 6 for the interface schematic. |
| 13 | V2 | |
| 14 | V3 | |
| 15 | V4 | |
| 16 | V5 | |
| | EPAD | Exposed pad. The exposed pad must be connected to ground for proper operation. |

FIGURE 2. Terminal connections.

| Digital control input SEE NOTE 1 | | | | | Attenuation state (dB) |
|---|---|---|---|---|---|
| V1 | V2 | V3 | V4 | V5 | |
| High | High | High | High | High | 0 (reference) |
| High | High | High | High | Low | 1 |
| High | High | High | Low | High | 2 |
| High | High | Low | High | High | 4 |
| High | Low | High | High | High | 8 |
| Low | High | High | High | High | 16 |
| Low | Low | Low | Low | Low | 31 SEE NOTE 2 |

NOTES:

1. Any combination of the control input states shown in figure 3 provides an attenuation equal to the sum of the bits selected.
2. 31 represents the sum total of all low logic states of the attenuator. 1 + 2 + 4 + 8 + 16 = 31

FIGURE 3. Truth table.

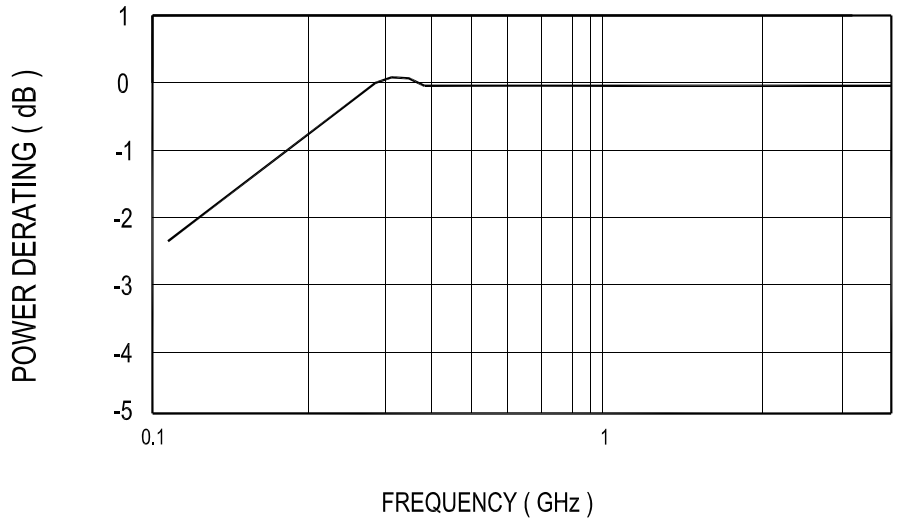


FIGURE 4. Power derating at frequencies less than 250 MHz.

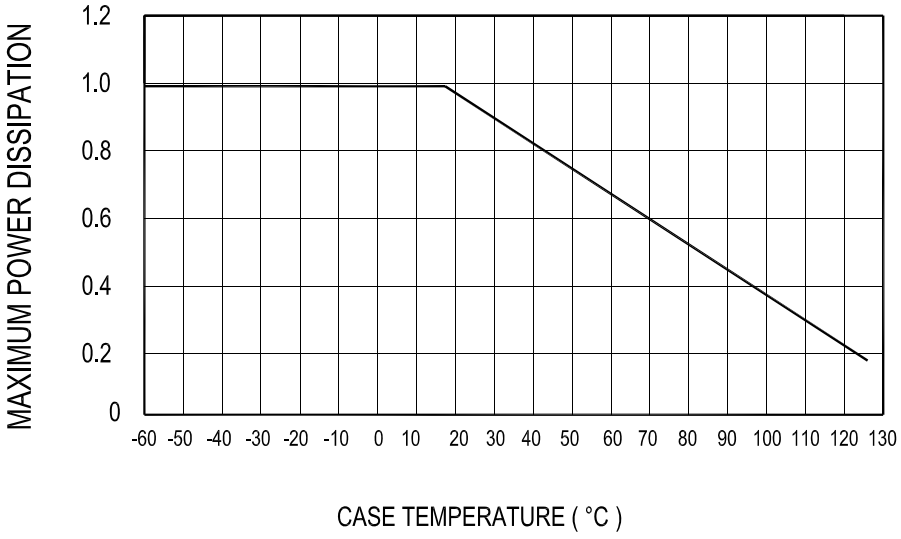


FIGURE 5. Maximum power dissipation versus case temperature graph.

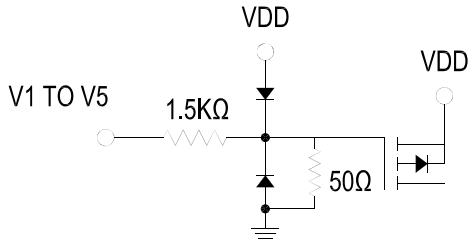


FIGURE 6. Digital control input interface circuit.

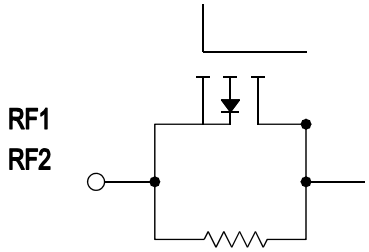


FIGURE 7. RF1, RF2 interface schematic.

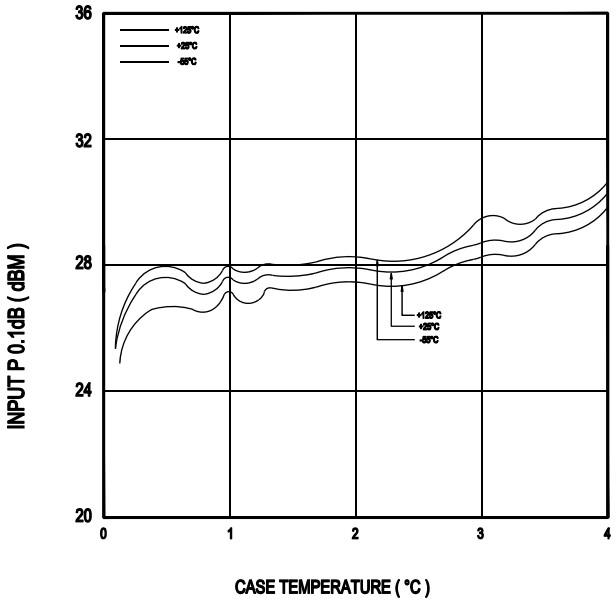


FIGURE 8. Input P0.1 dB versus frequency at minimum attenuation state for various temperatures graph with supply voltage at 5 V.

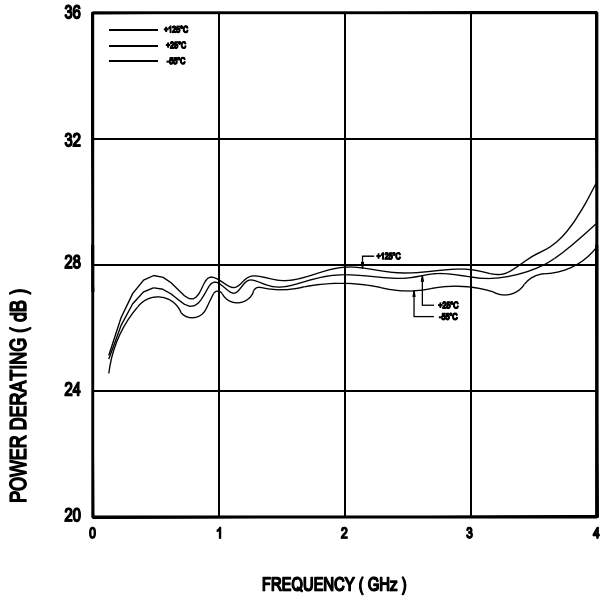


FIGURE 9. Input P0.1 dB versus frequency at minimum attenuation state for various temperatures graph with supply voltage at 3 V.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

| Vendor item drawing administrative control number 1/ | Device manufacturer CAGE code | Mode of transportation and quantity | Top side marking | Vendor part number |
|---|---|---|---|---|
| V62/17617-01XE | 24355 | Reel, 50 units | Y6U | HMC470ATCPZ-EP-PT |
| V62/17617-01XE | 24355 | Reel, 500 units | Y6U | HMC470ATCPZ-EP-RL7 |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

| CAGE code | Source of supply |
|---|---|
| 24355 | Analog Devices<br>Route 1 Industrial Park<br>P.O. Box 9106<br>Norwood, MA 02062<br>Point of contact: Raheen Business Park<br>Limerick, Ireland |