REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add description of footnotes 8/ and 9/ to TABLE I. Under FIGURE 1, replace numerical limits with symbols on the case outline and add dimensions table. Update document paragraphs to current requirements. - ro	23-06-26	J. Eschmeyer

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A							
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15							

PMIC N/A

Original date of drawing

YY-MM-DD

17-09-11

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TITLE
MICROCIRCUIT, LINEAR-DIGITAL, ROBUST 5 kV RMS ISOLATED RS-485 TRANSCEIVER WITH LEVEL 4 DO-160G EMC AND FULL ±42 V PROTECTION, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/17611
REV A		PAGE 1 OF 15

AMSC N/A

5962-V022-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance robust 5 kV root mean square (RMS) isolated RS-485 transceiver with level 4 DO-160G electromagnetic compatibility (EMC) and full ±42 V protection microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/17611	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADM2795E-EP	Robust 5 kV RMS isolated RS-485 transceiver with level 4 DO-160G EMC and full ±42 V protection

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MS-013-AA	Standard small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

V_{DD1}	-0.5 V to +7 V
V_{DD2}	-0.5 V to +7 V
Digital input / output voltage (DE, $\overline{RE}$, TxD, RxD)	-0.3 V to V_{DD1} + 0.3 V
Driver output / receiver input voltage	±48 V
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Maximum junction temperature	150°C
Continuous total power dissipation	405 mW
Lead temperature:	
Soldering (10 seconds)	300°C
Vapor phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD (A, B pins tested to GND_2)	
IEC 61000-4-2 contact discharger	±8 kV
IEC 61000-4-2 air discharger	±15 kV
EFT (A, B Pins Tested to GND_2)	
IEC 61000-4-4 Level 4 protection	±2 kV
Surge (A, B pins tested to GND_2)	
IEC 61000-4-5 level 5 surge protection	±4 kV
EMC performance from A, B bus pins across the isolation barrier to GND_1:	
ESD	
IEC 61000-4-2 contact discharger	±9 kV
IEC 61000-4-2 air discharger	±8 kV
EFT	
IEC 61000-4-4	±2 kV
Surge	
IEC 61000-4-5	±4 kV
Human body model (HBM), ESD protection (A, B pins tested to GND_2)	>±30 kV
HBM ESD protection (all pins)	±6 kV
DO-160G section 25 ESD protection air discharge	±15 kV
Field induced charged device model ESD (FICDM)	±1.25 kV

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ T_A = 25°C, unless otherwise noted.

1.4 Maximum continuous working voltage. 3/

Parameter	Max	Unit	Reference standard 4/
AC voltage			
Bipolar waveform			
Basic insulation	849	V peak	50-year minimum insulation lifetime
Reinforced insulation	768	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Unipolar waveform			
Basic insulation	1698	V peak	50-year minimum insulation lifetime
Reinforced insulation	885	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
DC voltage			
Basic insulation	1092	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Reinforced insulation	543	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1

1.5 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA} 5/	θ_{JC} 5/	Unit
Case X	59.7	28.3	°C/W

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

INTERNATIONAL ELECTROTECHNICAL COMMISSION (IEC)

IEC 60749-26 – Electrostatic discharge (ESD) sensitivity testing - Human Body Model (HBM)
IEC 61000-4-2 – Testing and measurement techniques – Electrostatic Discharge Immunity Test
IEC 61000-4-4 – Testing and measurement techniques – Electrical Fast Transient / Burst Immunity Test
IEC 61000-4-5 – Testing and Measurement techniques – Surge Immunity Test

(Copies of these documents are available online at http:/www.iec.ch.)

3/ The maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the manufacturer data sheet for more details.
4/ Insulation lifetime for the specified test condition is greater than 50 years.
5/ Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with no vias. See JEDEC JESD51.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Input capacitance (A, B) versus junction temperature. The input capacitance (A, B) versus junction temperature shall be as shown in figure 5.

3.5.6 Driver voltage measurement. The driver voltage measurement shall be as shown in figure 6.

3.5.7 Driver enable / disable. The driver enable / disable shall be as shown in figure 7.

3.5.8 Driver voltage measurement over common-mode voltage range. The driver voltage measurement over common-mode voltage range shall be as shown in figure 8.

3.5.9 Receiver propagation delay. The receiver propagation delay shall be as shown in figure 9.

3.5.10 Driver propagation delay. The driver propagation delay shall be as shown in figure 10.

3.5.11 Receiver enable / disable. The receiver enable / disable shall be as shown in figure 11.

3.5.12 Driver propagation delay, rise / fall timing. The driver propagation delay, rise / fall timing shall be as shown in figure 12.

3.5.13 Driver enable / disable timing. The driver enable / disable timing shall be as shown in figure 13.

3.5.14 Receiver propagation delay. The receiver propagation delay shall be as shown in figure 14.

3.5.15 Receiver enable / disable timing. The receiver enable / disable timing shall be as shown in figure 15.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
SUPPLY CURRENT section						
Power supply current						
Logic side	I_{DD1}	Unloaded output, DE = V_{DD1}, $\overline{RE}$ = 0 V			10	mA
TxD/RxD data rate = 2.5 Mbps		Unloaded output, DE = V_{DD1}, $\overline{RE}$ = 0 V			10	mA
Bus side	I_{DD2}	Unloaded output, DE = V_{DD1}, $\overline{RE}$ = 0 V			12	mA
TxD/RxD data rate = 2.5 Mbps		Unloaded output, DE = V_{DD1}, $\overline{RE}$ = 0 V			90	mA
		DE = V_{DD1}, $\overline{RE}$ = 0 V, V_{DD2} = 5.5 V, R = 27 Ω, see FIGURE 6			130	mA
		DE = V_{DD1}, $\overline{RE}$ = 0 V, V_{DD2} = 5.5 V, R = 27 Ω, see FIGURE 6		94		mA
		DE = V_{DD1}, $\overline{RE}$ = 0 V, V_{DD2} = 3.0 V, R = 27 Ω, see FIGURE 6		46		mA
Supply current in shutdown mode	ISHDN	DE = 0 V, $\overline{RE}$ = V_{DD1}			10	mA
DRIVER section						
Differential outputs						
Differential output voltage	$\lvert V_{OD}\rvert$	$V_{DD2} \geq 3.0$ V, R = 27 Ω or 50 Ω, see FIGURE 6	1.5		5.0	V
		$V_{DD2} \geq 4.5$ V, R = 27 Ω or 50 Ω, see FIGURE 6	2.1		5.0	V
	$\lvert V_{OD3}\rvert$	$V_{DD2} \geq 3.0$ V, V_{CM} = −25 V to +25 V, see FIGURE 8	1.5		5.0	V
		$V_{DD2} \geq 4.5$ V, V_{CM} = −25 V to +25 V, see FIGURE 8	2.1		5.0	V
Change in differential output voltage for complementary output states	$\Delta\lvert V_{OD}\rvert$	R = 27 Ω or 50 Ω, see FIGURE 6			0.2	V
Common-mode output voltage	V_{OC}	R = 27 Ω or 50 Ω, see FIGURE 6			3.0	V
Change in common-mode output voltage for complementary output states	$\Delta\lvert V_{OC}\rvert$	R = 27 Ω or 50 Ω, see FIGURE 6			0.2	V
Short-circuit output current						
V_{OUT} = Low	I_{OSL}	−42 V ≤ V_{SC} ≤ +42 3/	-250		+250	mA
V_{OUT} = High	I_{OSH}	−42 V ≤ V_{SC} ≤ +42 3/	-250		+250	mA
Logic inputs (DE, $\overline{RE}$, TxD)						
Input threshold low	V_{IL}	1.7 V ≤ V_{DD1} ≤ 5.5 V			0.33 × V_{DD1}	V
Input threshold high	V_{IH}	1.7 V ≤ V_{DD1} ≤ 5.5 V	0.7 V_{DD1}			V
Input current	I_{TxD}	0 V ≤ V_{IN} ≤ V_{DD1}			+1	mA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
RECEIVER section 2/						
Differential inputs						
Differential input threshold voltage	V_{TH}	−25 V ≤ V_{CM} ≤ +25 V	-200	-125	-30	mV
Input voltage hysteresis	V_{HIS}	−25 V ≤ V_{CM} ≤ +25 V		30		mV
Input current (A, B)	I_I	DE = 0 V, V_{DD2} = 0 V/5 V, V_{IN} = ±25 V	-1.0		+1.0	mA
		DE = 0 V, V_{DD2} = 0 V/5 V, V_{IN} = ±42 V	-1.0		+1.0	
Input capacitance (A, B)	C_{AB}	T_A = 25°C, see FIGURE 5		150		pF
Line input resistance	R_{IN}	−25 V ≤ V_{CM} ≤ +25 V, up to 256 nodes supported	96			kΩ
Logic outputs						
Output voltage low	V_{OLRxD}	IORxD = 3.0 mA, VA − VB = −0.2 V			0.2	V
Output voltage high	V_{OHRxD}	IORxD = −3.0 mA, VA − VB = 0.2 V	V_{DD1} -0.2			V
Short-circuit current		V_{OUT} = GND or V_{DD1}, $\overline{RE}$ = 0 V			100	mA
Three-state output leakage current	I_{OZR}	$\overline{RE}$ = V_{DD1}, RxD = 0 V or V_{DD1}			±2	µA
Common-mode transient immunity 4/		V_{CM} ≥ 1 kV, transient magnitude ≥ 800 V	75	125		kV/µs
TIMING SPECIFICATIONS section 5/						
DRIVER 6/						
Maximum data rate			2.5			Mbps
Propagation delay	t_{DPLH}, t_{DPHL}	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see FIGURE 10 and FIGURE 12		30	500	ns
Differential skew	t_{SKEW}			10	50	ns
Rise / fall times	t_R, t_F			40	130	ns
Enable time	t_{ZH}, t_{ZL}	R_L = 110 Ω, C_L = 50 pF,		500	2500	ns
Disable time	t_{HZ}, t_{LZ}	see FIGURE 7 and FIGURE 13		500	2500	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
TIMING SPECIFICATIONS section – continued. 5/						
RECEIVER 7/						
Propagation delay,	t_{PLH}, t_{PHL}	$V_{ID} \geq \pm 1.5$ V, C_L = 15 pF, See FIGURE 9 and FIGURE 14		120	200	ns
		$V_{ID} \geq \pm 600$ mV, C_L = 15 pF, See FIGURE 9 and FIGURE 14		140	220	
Skew	t_{SKEW}	$V_{ID} \geq \pm 1.5$ V, C_L = 15 pF, See FIGURE 9 and FIGURE 14		4	40	ns
Enable time		R_L = 1 kΩ, C_L = 15 pF, see FIGURE 11 and FIGURE 15		10	50	ns
Disable time				10	50	ns
RxD pulse width distortion		C_L = 15 pF, $V_{ID} \geq \pm 1.5$ V, see FIGURE 9 and FIGURE 14			40	ns
PACKAGE CHARACTERISTICS section						
Resistance (input to output) 8/	R_{I-O}			10^{13}		Ω
Capacitance (input to output) 8/	C_{I-O}	f = 1 MHz		2.2		pF
Input capacitance 9/	C_I			4.0		pF
Input capacitance, A and B Pins	C_{AB}	T_A = 25°C, see FIGURE 5		150		pF
IC junction to ambient thermal resistance	θ_{JA}	Thermocouple located at center of package underside		59.7		°C/W

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ 1.7 V ≤ V_{DD1} ≤ 5.5 V, 3 V ≤ V_{DD2} ≤ 5.5 V, T_A = −55°C to +125°C. All min/max specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications at T_A = 25°C, V_{DD1} = V_{DD2} = 5.0 V, unless otherwise noted.

3/ V_{SC} is the short-circuit voltage at the RS-485 A or B bus pin.

4/ Common-mode transient immunity is the maximum common-mode voltage slew rate that can be sustained while maintaining specification compliant operation. VCM is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common mode voltage slew rates apply to both rising and falling common-mode voltage edges.

5/ V_{DD1} = 1.7 V to 5.5 V, V_{DD2} = 3.0 V to 5.5 V, T_A = T_{MIN} to T_{MAX} (−55°C to +125°C), unless otherwise noted.

6/ See FIGURE 10 for the definition of RLDIFF.

7/ Receiver propagation delay, skew, and pulse width distortion specifications are tested with a receiver differential input voltage (V_{ID}) of ≥ ±600 mV or ≥ ±1.5 V, as noted.

8/ The device is considered a 2 terminal device: pin 1 through pin 8 are shorted together, and pin 9 through pin 16 are shorted together.

9/ Input capacitance is from any digital input pin to ground.

Case X

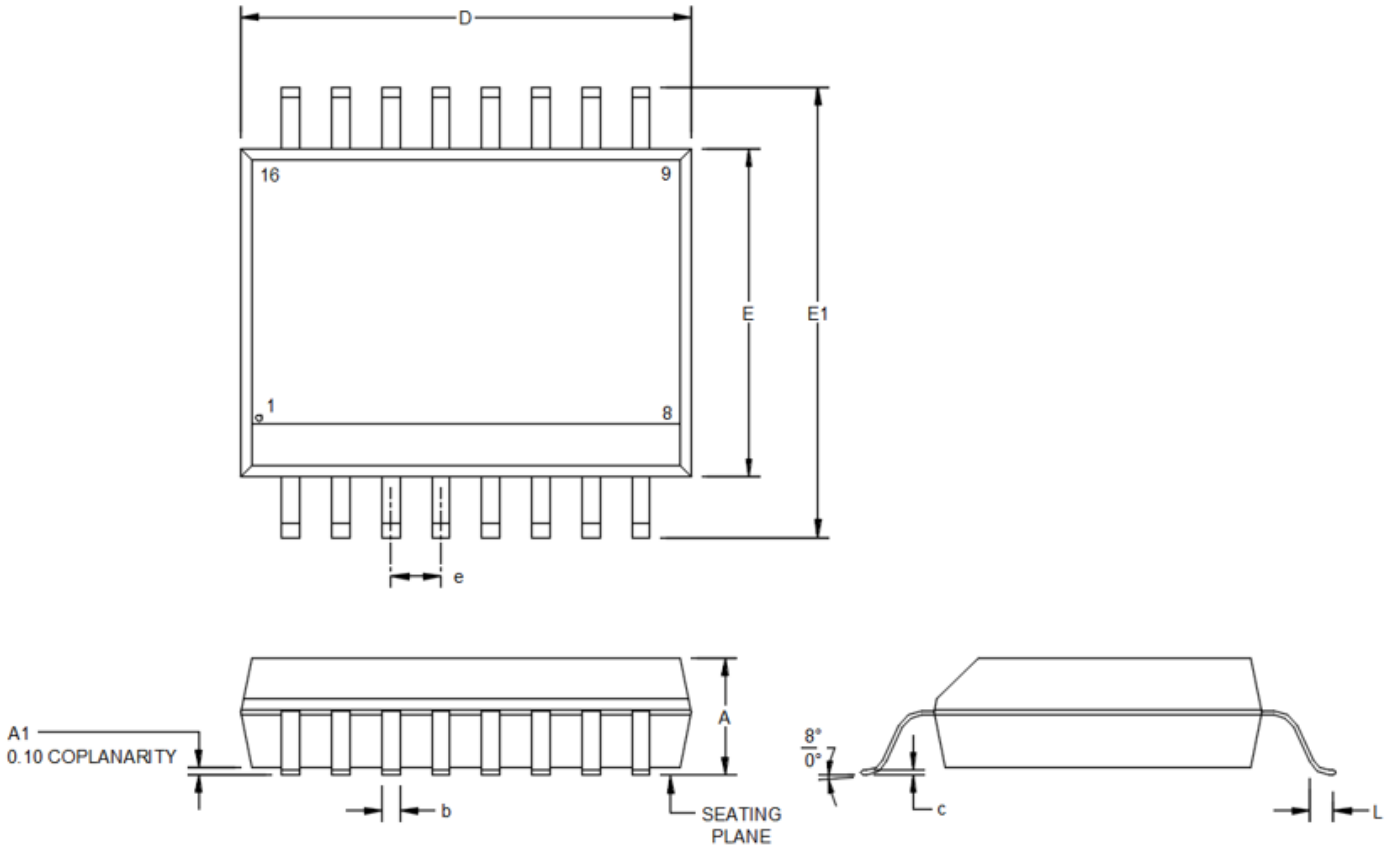

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/17611
		REV A	PAGE 9

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	.0925	.1043	2.35	2.65
A1	.0039	.0118	0.10	0.30
b	.0122	.0201	0.31	0.51
c	.0079	.0130	0.20	0.33
D	.3976	.4134	10.10	10.50
E	.2913	.2992	7.40	7.60
E1	.3937	.4139	10.00	10.65
L	.0157	.0500	0.40	1.27

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-013-AA.

FIGURE 1. Case outline - Continued.

Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{DD1}	16	V_{DD2}
2	GND_1	15	GND_2
3	TxD	14	B
4	DE	13	V_{DD2}
5	$\overline{RE}$	12	GND_2
6	RxD	11	A
7	NIC	10	GND_2
8	GND_1	9	GND_2

NIC = Not Internally connected.

FIGURE 2. Terminal connections.

Terminal number	Terminal symbol	Description
1	V_{DD1}	1.7 V to 5.5 V Flexible logic interface supply.
2	GND_1	Ground 1, logic side.
3	TxD	Transmit data input. Data to be transmitted by the driver is applied to this input.
4	DE	Driver output enable. A high level on this pin enables the driver differential outputs, A and B. A low level places them into a high impedance state.
5	$\overline{RE}$	Receiver enable input. This pin is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
6	RxD	Receiver output data. This output is high when (A – B) > −30 mV and low when (A – B) < –200 mV.
7	NIC	Not internally connected. This pin is not internally connected.
8	GND_1	Ground 1, logic side.
9	GND_2	Isolated ground 2, bus side.
10	GND_2	Isolated ground 2, bus side.
11	A	Noninverting driver output / receiver input. When the driver is disabled, or when V_{DD1} or V_{DD2} is powered down, pin A is put into a high impedance state to avoid overloading the bus.
12	GND_2	Isolated ground 2, bus side.
13	V_{DD2}	3 V to 5.5 V power supply. Pin 13 must be connected externally to pin 16.
14	B	Inverting driver output / receiver input. When the driver is disabled, or when V_{DD1} or V_{DD2} is powered down, pin B is put into a high impedance state to avoid overloading the bus.
15	GND_2	Isolated ground 2,bus side.
16	V_{DD2}	3 V to 5.5 V power supply. Pin 16 must be connected externally to pin 13.

FIGURE 3. Terminal function.

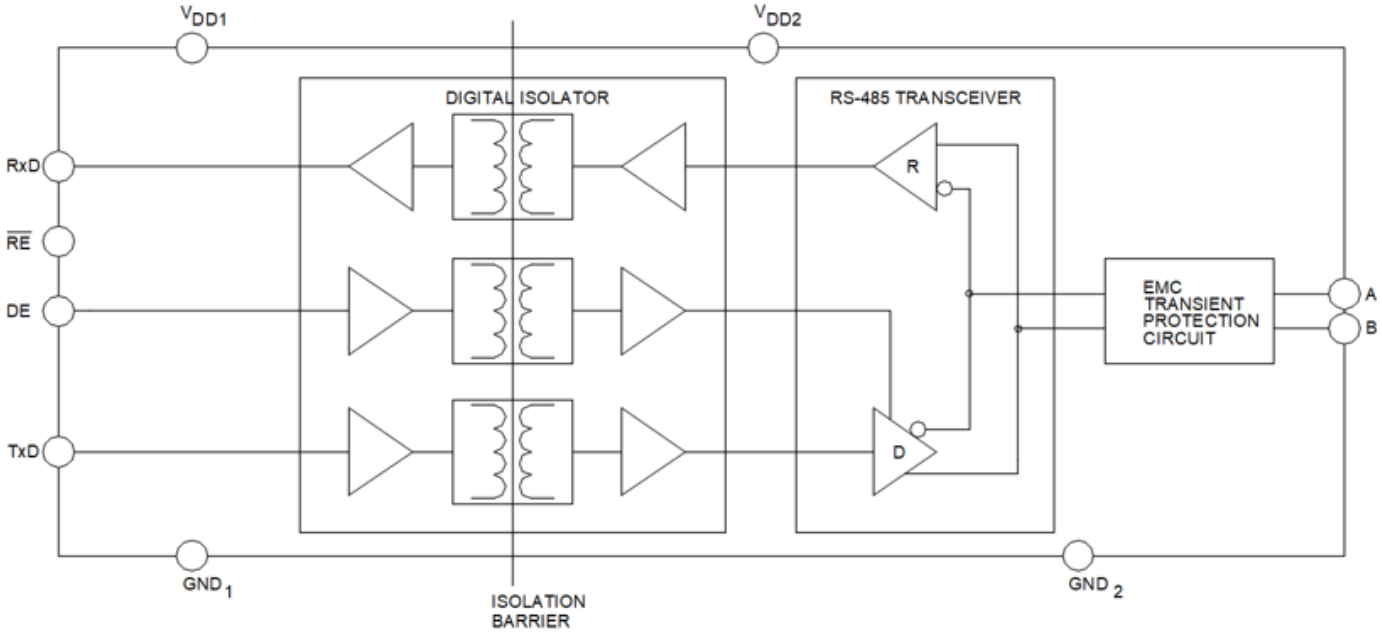

FIGURE 4. Functional block diagram.

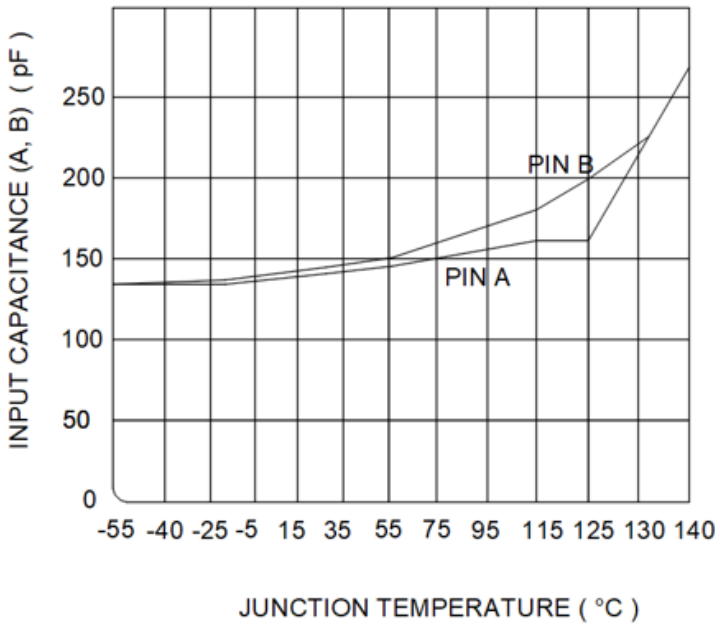

FIGURE 5. Input Capacitance (A, B) versus Junction Temperature.

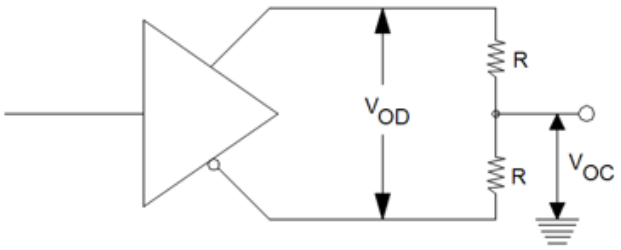

FIGURE 6. Driver Voltage Measurement.

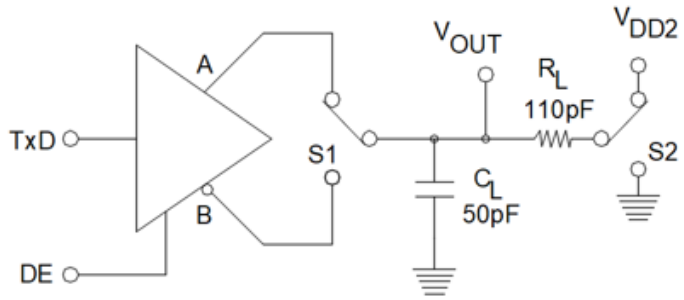

FIGURE 7. Driver Enable/Disable.

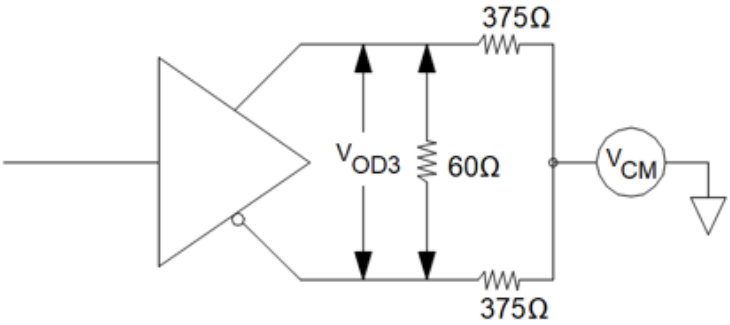

FIGURE 8. Driver Voltage Measurement over Common-Mode Voltage Range.

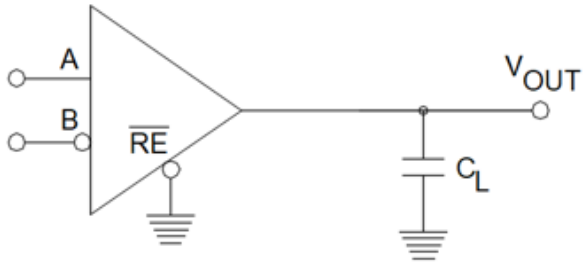

FIGURE 9. Receiver Propagation Delay.

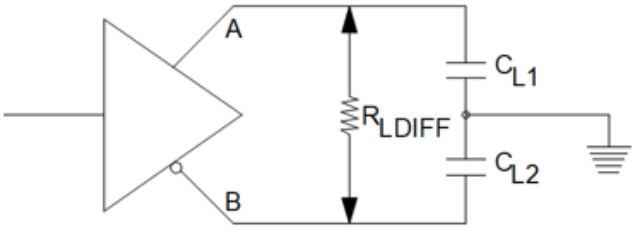

FIGURE 10. Driver Propagation Delay.

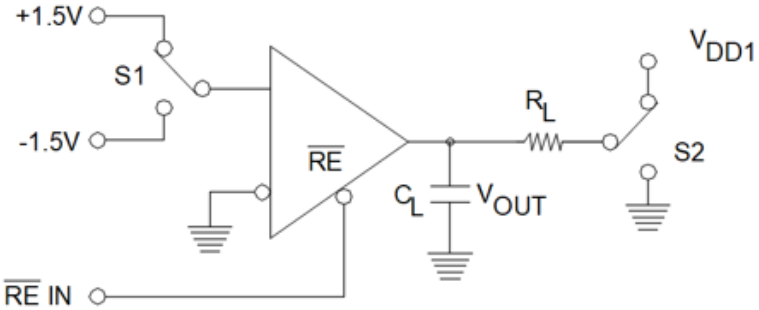

FIGURE 11. Receiver Enable/Disable.

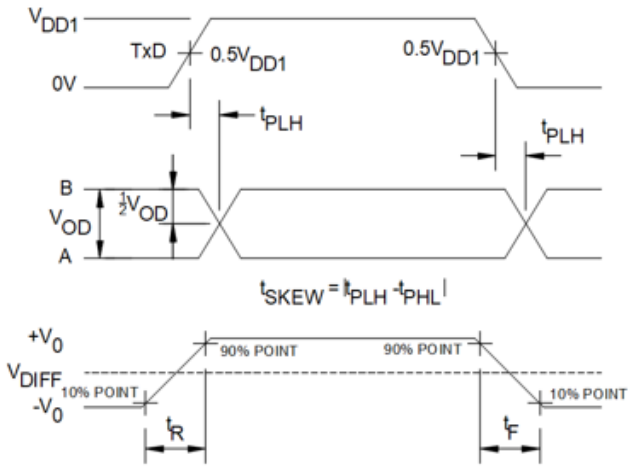

FIGURE 12. Driver Propagation Delay, Rise/Fall Timing.

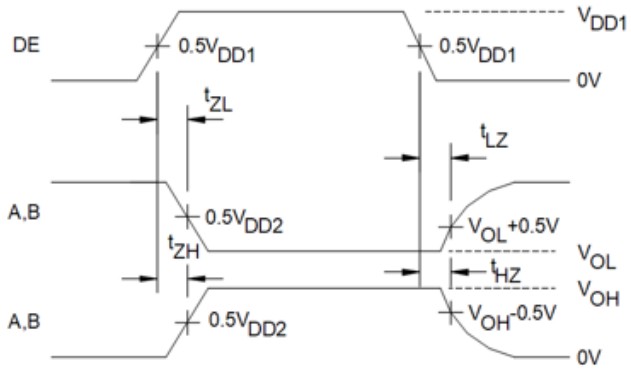

FIGURE 13. Driver Enable/Disable Timing.

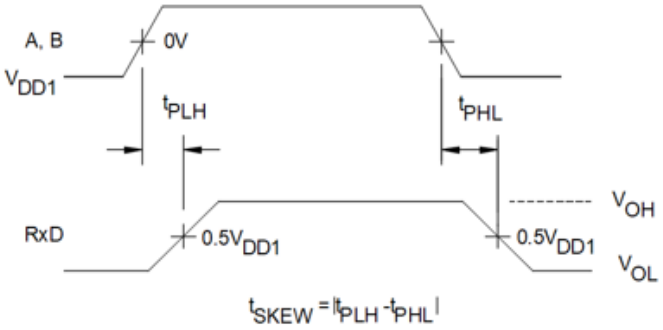

FIGURE 14. Receiver Propagation Delay.

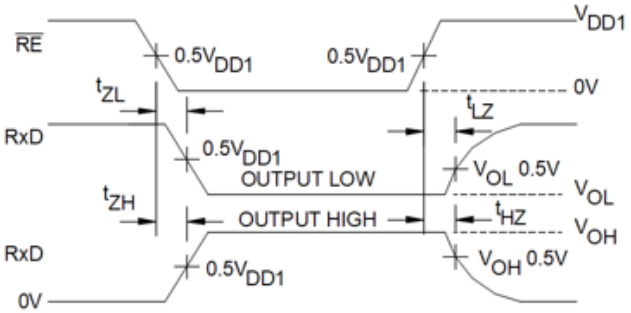

FIGURE 15. Receiver Enable/Disable Timing.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/17611-01XE	24355	Tube, 47 units	ADM2795ETRWZ-EP
		Reel, 400 units	ADM2795ETRWZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123