REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17				

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 17-09-11	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 16-BIT, 1 MSPS, 8-CHANNEL, DATA ACQUISITION SYSTEM, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/17609**
	REV	**PAGE** 1 **OF** 17

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AMSC N/A

5962-V065-17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16-Bit, 1 MSPS, 8-Channel Data Acquisition System microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/17609	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADAS3022 –EP	16-Bit, 1 MSPS, 8-Channel Data Acquisition System

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	40	JEDEC MO-220-VJJD-5	Lead Frame Chip Scale Package (LFCSP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Analog Inputs/Outputs:	
INx, COM to AGND	VSSH – 0.3 V to VDDH + 0.3 V
AUX+, AUX- to AGND	-0.3 V to AVDD + 0.3 V
REFx to AGND	AGND – 0.3 V to AVDD + 0.3V
REFIN to AGND	AGND – 0.3 V to +2.7 V
REFIN to AGND	±0.3 V
Ground Voltage Differences	
AGND, RGND, DGND	±0.3 V
Supply Voltages	
VDDH to AGND	-0.3 V to +16.5 V
VSSH to AGND	+0.3 V to -16.5 V
AVDD, DVDD, VIO to AGND	-0.3 V to +7 V
ACAP, DCAP, RCAP to GND	-0.3 V to + 2.7 V
Digital Inputs/Outputs	
CNV, DIN, SCK, RESET, PD, $\overline{CS}$ to DGND	-0.3 V to VIO + 0.3 V
SDO, BUSY to DGND	-0.3 V to VIO + 0.3 V
Internal Power Dissipation	2 W
Junction temperature	125°C
Storage temperature range	-65°C to 150°C
Thermal Impedance	
θ_{JA}	44.1°C/W
θ_{JC}	0.28°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Load Circuit for Digital Interface Timing. The Load Circuit for Digital Interface Timing shall be as shown in figure 5.

3.5.6 Voltage Level for Timing. The Voltage Level for Timing shall be as shown in figure 6.

3.5.7 General Timing Diagram. The General Timing Diagram shall be as shown in figure 7.

TABLE I. Electrical performance characteristics. 1/

Test	Test conditions 2/	Limits			Unit 3/
		Min	Typ	Max	
RESOLUTION		16			Bits
ANALOG INPUTS—IN[7:0], COM					
Operating Input Voltage Range	VIN	−VSSH + 2.5		VDDH − 2.5	V
Differential Input Voltage Range, VIN	VIN+ − VIN− PGIA gain = 0.16, VIN = 49.15 V p-p PGIA gain = 0.2, VIN = 40.96 V p-p PGIA gain = 0.4, VIN = 20.48 V p-p PGIA gain = 0.8, VIN = 10.24 V p-p PGIA gain = 1.6, VIN = 5.12 V p-p PGIA gain = 3.2, VIN = 2.56 V p-p PGIA gain = 6.4, VIN = 1.28 V p-p	 −6 × VREF −5 × VREF −2.5 × VREF −1.25 × VREF −0.625 × VREF −0.3125 × VREF −0.1563 × VREF		 +6 × VREF +5 × VREF +.5 × VREF +1.25 × VREF +0.625 × VREF +0.3125 × VREF +0.1563 × VREF	V
Input Impedance, ZIN		500			MΩ
Channel Off Leakage			±0.6		nA
Channel On Leakage			±0.02		nA
Common-Mode Voltage Range (VCM) 4/	VIN+, VIN−; full-scale differential inputs PGIA gain = 0.4 PGIA gain = 0.8 PGIA gain = 1.6 PGIA gain = 3.2 PGIA gain = 6.4	 -5.12 -7,68 -8.96 -9.60 -9.92		 +5.12 +7,68 +8.96 +9.60 +9.92	V
ANALOG INPUTS—AUX+, AUX−					
Differential Input Voltage Range		$-V_{REF}$		$+V_{REF}$	V
THROUGHPUT					
Conversion Rate One channel and one pair Two channels and two pairs Four channels and four pairs Eight channels		 0 0 0 0		 1000 500 250 125	kSPS
Transient Response	Full-scale step			520	ns
DC ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error PGIA gain = 0.16, 0.2, 0.4, 0.8, and 1.6 PGIA gain = 3.2 PGIA gain = 6.4	 PGIA gain = 0.16, 0.2, 0.4, 0.8, and 1.6 PGIA gain = 3.2 PGIA gain = 6.4	 -2 -3 -5	 ±0.6 ±1.0 ±1.5	 +2 +3 +5	LSB
Differential Linearity Error PGIA gain = 0.16, 0.2, 0.4, 0.8, and 1.6 PGIA gain = 3.2 PGIA gain = 6.4	 PGIA gain = 0.16, 0.2, 0.4, 0.8, and 1.6 PGIA gain = 3.2 PGIA gain = 6.4	 -0.9 -0.9 -0.9	 ±0.6 ±0.75 ±0.75	 +1.0 +31.25 +51.25	LSB
Transition Noise External reference PGIA gain = 0.16, 0.2, 0.4, 0.8, and 1.6 PGIA gain = 3.2 PGIA gain = 6.4	 	 	 5 7 11	 	LSB
Gain Error	External reference, all PGIA gains, T_A = 25°C	-9		+9	LSB
Gain Error Temperature Drift	External reference, all PGIA gains			0.1	ppm/°C

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions 2/	Limits			Unit 3/
		Min	Typ	Max	
DC ACCURACY - Continued					
Offset Error	External reference, TA = 25°C				
	PGIA gain = 0.16, 0.2, 0.4, and 0.8	-3.0	+0.2	+3.0	LSB
	PGIA gain = 1.6	-4.0	+0.2	+4.0	
	PGIA gain = 3.2	-7.5	+0.2	+7.5	
	PGIA gain = 6.4	-12.5	+0.2	+12.5	
Offset Error Temperature Drift	External reference				
	PGIA gain = 0.16, 0.2, 0.4, and 0.8		0.1	0.5	ppm/°C
	PGIA gain = 1.6		0.2	1.0	
	PGIA gain = 3.2		0.4	2.0	
	PGIA gain = 6.4		0.8	4.0	
Total Unadjusted Error	External reference, ambient temperature (T_A) = 25°C				
	PGIA gain = 0.16, 0.2, 0.4, 0.8, 1.6, and 3.2	-9		+9	LSB
	PGIA gain = 6.4	-15		+15	
AC ACCURACY 5/					
Signal-to-Noise Ratio (SNR)	f_{IN} = 10 kHz				
	PGIA gain = 0.16	90.0	91.5		dB
	PGIA gain = 0.2	90.0	91.5		
	PGIA gain = 0.4	89.5	91.5		
	PGIA gain = 0.8	89.0	91.0		
	PGIA gain = 1.6	88.0	89.7		
	PGIA gain = 3.2	86.0	86.8		
	PGIA gain = 6.4	83.0	84.5		
Signal-to-Noise-and-Distortion (SINAD)	Input frequency (f_{IN}) = 10 kHz				
	PGIA gain = 0.16	88.0	90.0		dB
	PGIA gain = 0.2	88.0	90.0		
	PGIA gain = 0.4	88.5	91.0		
	PGIA gain = 0.8	88.5	90.5		
	PGIA gain = 1.6	87.5	89.5		
	PGIA gain = 3.2	85.5	86.5		
	PGIA gain = 6.4	82.5	84.0		
Dynamic Range	f_{IN} = 10 kHz, −60 dB input				
	PGIA gain = 0.16	91.0	92.0		dB
	PGIA gain = 0.2	91.0	92.0		
	PGIA gain = 0.4	90.5	91.5		
	PGIA gain = 0.8	90.0	91.0		
	PGIA gain = 1.6	89.0	90.0		
	PGIA gain = 3.2	86.0	87.0		
	PGIA gain = 6.4	83.5	85.0		
Total Harmonic Distortion (THD)	f_{IN} = 10 kHz, all PGIA gains		-100		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 10 kHz, all PGIA gains		101		dB
Channel to Channel Crosstalk	f_{IN} = 10 kHz, all channels inactive		-120		dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions 2/	Limits			Unit 3/
		Min	Typ	Max	
AC ACCURACY - Continued 5/					
Common-Mode Rejection Ratio (CMRR)	f_{IN} = 2 kHz PGIA gain = 0.16, 0.2, 0.4, and 0.8 PGIA gain = 1.6 PGIA gain = 3.2 PGIA gain = 6.4	 90.0 90.0 90.0 90.0	 110.0 105.0 98.0 98.0		dB
−3 dB Input Bandwidth	−40 dBFS		8		MHz
AUXILIARY ADC INPUT CHANNEL					
DC Accuracy Integral Nonlinearity Error Differential Nonlinearity Error Gain Error Offset Error	External reference	 -1.5 -0.8 -2.5 -5	 ±0.5 ±0.6 ±0.2 ±0.2	 +1.5 +1.0 +2.5 +5	 LSB
AC Performance SNR SINAD THD SFDR	Internal reference	 90.0 89.5	 93.0 92.5 -105 110		 dB
INTERNAL REFERENCE					
REF1 and REF2 Output Voltage	T_A = 25°C	4.088	4.096	4.104	V
REF1 and REF2 Output Current	T_A = 25°C		250		µA
REF1 and REF2 Temperature Drift	REFEN = 1 REFEN = 0		±5 ±1		ppm/°C
REF1 and REF2 Line Regulation Internal Reference Buffer Only	AVDD = 5 V ± 5%		 20 4		µV/V
REFIN Output Voltage 6/	T_A = 25°C	2.495	2.500	2.505	V
Turn-On Settling Time	C_{REFIN}, C_{REF1}, C_{REF2} = 10 µF and 0.1 µF		100		ms
EXTERNAL REFERENCE					
Voltage Range	REFx input REFIN input (buffered)	 4.000	 4.096 2.5	 4.104 2.505	 V
Current Drain	V_{REF} = 4.096 V		100		µA
TEMPERATURE SENSOR					
Output Voltage	T_A = 25 °C		275		mV
Temperature Sensitivity			800		µV/°C
DIGITAL INPUTS					
Logic Levels Input Voltage Low, V_{IL} Input Voltage High, V_{IH} Input Low Current, I_{IL} Input High Current, I_{IH}	 VIO > 3 V VIO ≤ 3 V VIO > 3 V VIO ≤ 3 V	 -0.3 -0.3 0.7 x VIO 0.9 x VIO -1 -1		 +0.3 x VIO +0.1 x VIO VIO + 0.3 VIO + 0.3 +1 +1	 V V V V µA µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions 2/	Limits			Unit 3/
		Min	Typ	Max	
DIGITAL OUTPUTS 7/					
Data Format			Twos complement		
Output Low Voltage, V_{OL}	I_{SINK} = +500 µA			0.4	V
Output High Voltage, V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES	(PD = 0)				
VIO		1.8		AVDD + 0.3	V
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
VDDH	VDDH > input voltage + 2.5 V	14.25	15	15.75	V
VSSH	VSSH < input voltage − 2.5 V	-15.75	-15	-14.25	V
VDDH Capacitance, I_{VDDH}	PGIA gain = 0.16		3.0	3.5	mA
	PGIA gain = 0.2		3.0	3.5	mA
	PGIA gain = 0.4		3.5	4.0	mA
	PGIA gain = 0.8		5.0	5.5	mA
	PGIA gain = 1.6		8.5	9.5	mA
	PGIA gain = 3.2		15.5	17.5	mA
	PGIA gain = 6.4		15.5	17.5	mA
	All PGIA gains, PD = 1		100		µA
Current at VSSH Supply, I_{VSSH}	PGIA gain = 0.16	-3.0	-2.5	21.0	mA
	PGIA gain = 0.2	-3.0	-2.5	19.0	mA
	PGIA gain = 0.4	-3.5	-3.0	17.5	mA
	PGIA gain = 0.8	-5.5	-4.5	16.0	mA
	PGIA gain = 1.6	-9.5	-8.0		mA
	PGIA gain = 3.2	-17.5	-15		mA
	PGIA gain = 6.4	-17.5	-15		mA
	All PGIA gains, PD = 1		10		µA
Current at AVDD, I_{AVDD}	PGIA gain = 6.4, reference buffer enabled		18		mA
	All other PGIA gains, reference buffer enabled		16		mA
	PGIA gain = 6.4, reference buffer disabled		14		mA
	All other PGIA gains, reference buffer disabled		12		mA
	All PGIA gains, PD = 1		100		µA
Current at DVDD, I_{DVDD}	All PGIA gains, PD = 0		2.5	3.5	mA
	All PGIA gains, PD = 1		1.0		µA
Current at VIO, I_{VIO}	VIO = 3.3 V, PD = 0		0.30	1.2	mA
	PD = 1		10		µA
Power Supply Sensitivity At T_A = 25°C	External reference				
	PGIA gain = 0.16, 0.2, 0.4, and 0.8; VDDH/VSSH ± 5%		±0.5		LSB
	PGIA gain = 3.2, VDDH/VSSH ± 5%		±1.0		
	PGIA gain = 6.4, VDDH/VSSH ± 5%		±2.0		
	PG PGIA gain = 0.16, AVDD/DVDD ± 5%		±0.6		
	PGIA gain = 0.2, AVDD/DVDD ± 5%		±0.8		
	PGIA gain = 0.4, AVDD/DVDD ± 5%		±1.0		
	PGIA gain = 0.8, AVDD/DVDD ± 5%		±1.5		
	PGIA gain = 1.6, AVDD/DVDD ± 5%		±2.0		
	PGIA gain = 3.2, AVDD/DVDD ± 5%		±3.5		
	PGIA gain = 6.4, AVDD/DVDD ± 5%		±7.0		
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	-55		+105	°C

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 9/	Limits			Unit
			Min	Typ	Max	
TIMING SPECIFICATIONS						
Time Between Conversions	t_{CYC}					
Warp Mode, 10/ CMS = 0			1		1000	µs
Normal Mode (Default), CMS = 1			1.1			µs
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}					
Warp Mode, CMS = 0				825		ns
Normal Mode (Default), CMS = 1				925	1000	ns
Auxiliary ADC Input Channel Acquisition Time	t_{ACQ}		600			ns
CNV Pulse Width	t_{CH}		10			ns
CNV High to Hold Time (Aperture Delay)	t_{AD}			2		ns
CNV High to Busy Delay	t_{CBD}				520	ns
Safe Data Access Time During Conversion	t_{DDC}				500	ns
Quiet Conversion Time (BUSY High)	t_{QUIET}					
Warp Mode, CMS = 0					400	ns
Normal Mode (Default), CMS = 1					500	ns
Data Access During Quiet Conversion Time	t_{DDCA}					
Warp Mode, CMS = 0					200	ns
Normal Mode (Default), CMS = 1					300	ns
SCK Period	t_{SCK}		15			ns
SCK Low Time	t_{SCKL}		5			ns
SCK High Time	t_{SCKH}		5			ns
SCK Falling Edge to Data Valid	t_{SDOH}		4			ns
SCK Falling Edge to Data Valid Delay	t_{SDOD}					
VIO > 4.5 V					12	ns
VIO > 3.0 V					18	ns
VIO > 2.7 V					24	ns
VIO > 2.3 V					25	ns
VIO > 1.8 V					37	ns
$\overline{CS}$/RESET/PD Low to SDO	t_{EN}					
VIO > 4.5 V					15	ns
VIO > 3.0 V					16	ns
VIO > 2.7 V					18	ns
VIO > 2.3 V					23	ns
VIO > 1.8 V					28	ns
$\overline{CS}$/RESET/PD High to SDO High Impedance	t_{DIS}				25	ns
DIN Valid Setup Time from SCK Rising Edge	t_{DINS}		4			ns
DIN Valid Hold Time from SCK Rising Edge	t_{DINH}		4			ns
CNV Rising to $\overline{CS}$	t_{CCS}		5			ns
RESET/PD High Pulse	t_{RH}		5			ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ VDDH = 15 V ± 5%, VSSH = −15 V ± 5%, AVDD = DVDD = 5 V ± 5%, VIO = 1.8 V to AVDD, internal voltage reference (VREF) = 4.096 V, sampling frequency (fS) = 1 MSPS unless otherwise noted. All specifications TMIN to TMAX, unless otherwise noted.

3/ LSB means least significant bit and changes depending on the voltage range.

4/ The common-mode voltage (VCM) for a PGIA gain of 0.16 or 0.2 is 0 V.

5/ All ac accuracy specifications expressed in decibels are referred to a full-scale range (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise noted.

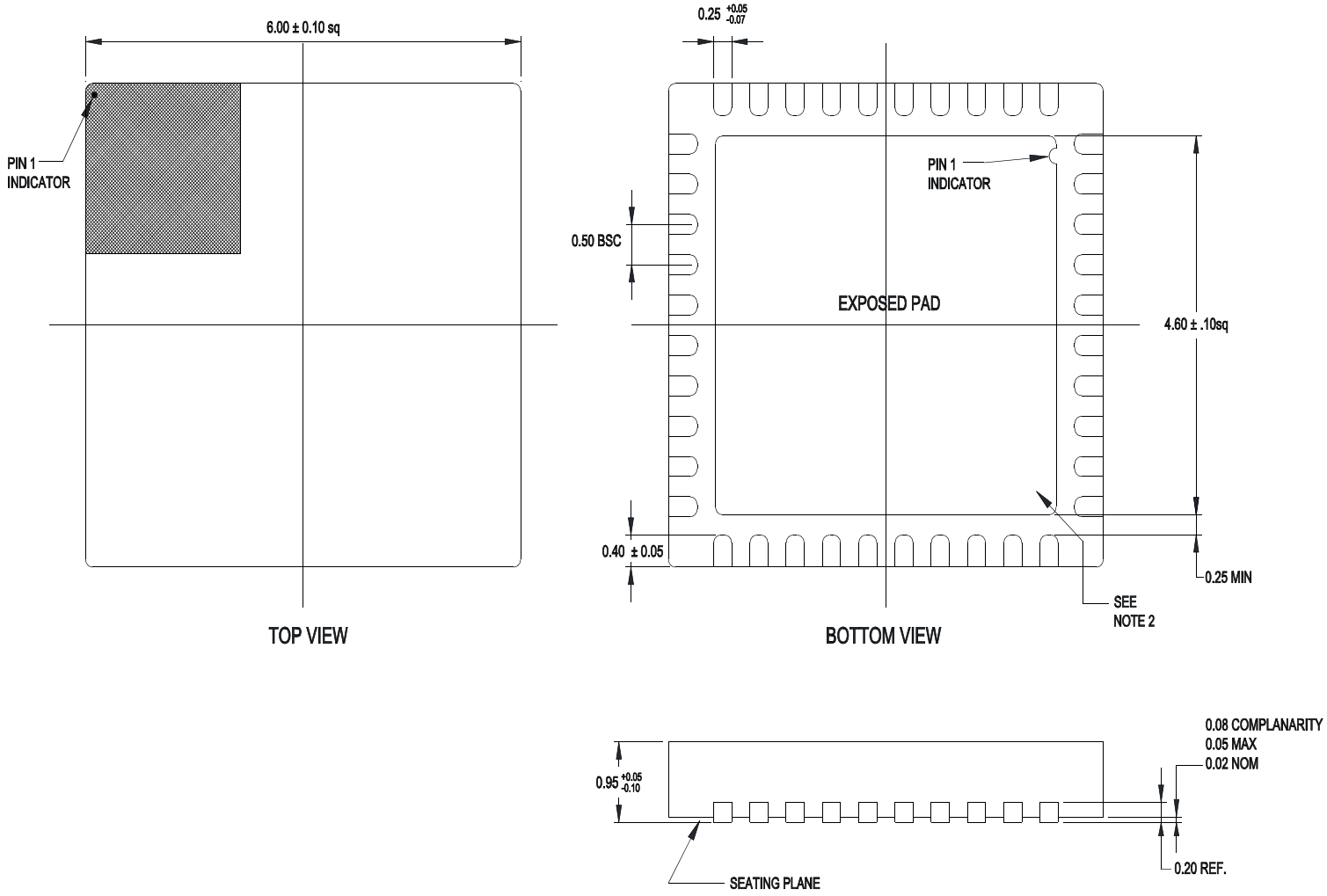
6/ This is the output from the internal band gap reference.

7/ There is no pipeline delay. Conversion results are available immediately after a conversion is complete.

8/ The differential input common-mode voltage (VCM) range changes according to the maximum input range selected and the high voltage power supplies (VDDH and VSSH). Note that the specified operating input voltage of any input pin requires 2.5 V of headroom from the VDDH and VSSH supplies; therefore, (VSSH + 2.5 V) ≤ INx/COM ≤ (VDDH − 2.5 V).

9/ VDDH = 15 V ± 5%, VSSH = −15 V ± 5%, AVDD = DVDD = 5 V ± 5%, VIO = 1.8 V to AVDD, internal reference, V_{REF} = 4.096 V, f_S = 1 MSPS unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Case X



NOTES:
1. All linear dimensions are in millimeters.
2. For the proper connection of the exposed PAD, refer to the pin configuration and function description of this data sheet.
3. Falls within JEDEC MO-220-VJJD-5.

FIGURE 1. Case outline.

Case outline X							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	IN0	11	$\overline{CS}$	21	DGND	31	RCAP
2	IN1	12	DIN	22	DGND	32	REFIN
3	IN2	13	RESET	23	AGND	33	REF1
4	IN3	14	NC	24	AGND	34	REF2
5	AUX+	15	PD	25	DCAP	35	RGND
6	IN4	16	SCK	26	ACAP	36	REFN
7	IN5	17	VIO	27	DVDD	37	REFN
8	IN6	18	SDO	28	AVDD	38	VSSH
9	IN7	19	BUSY	29	NC	39	VDDH
10	COM	20	CNV	30	NC	40	AUX-

FIGURE 2. Terminal connections.

Case outline X			
Terminal number	**Mnemonic**	**Type**	**Description**
1 to 4	IN0 to IN3	AI	Input Channel 0 to Input Channel 3.
5	AUX+	AI	Auxiliary Input Channel Positive Input.
6 to 9	IN4 to IN7	AI	Input Channel 4 to Input Channel 7.
10	COM	AI	IN[7:0] Common Channel Input. The IN[7:0] input channels can be referenced to a common point. The maximum voltage on this pin is ±10.24 V for all PGIA gains except for a PGIA gain of 0.16, in which case, the maximum voltage on this pin is ±12.228 V. AUX+ and AUX− are not referenced to COM.
11	$\overline{CS}$	DI	Chip Select. Active low signal. Enables the digital interface for writing and reading data. Use this pin when sharing the serial bus. For a dedicated ADAS3022-EP serial interface, $\overline{CS}$ can be tied to DGND or CNV to simplify the interface.
12	DIN	DI	Data Input. Serial data input used for writing the 16-bit configuration word (CFG) that is latched on SCK rising edges. CFG is an internal register that is updated on the rising edge of the end of a conversion, which is the falling edge of BUSY. The configuration register can be written to during and after a conversion.
13	RESET	DI	Asynchronous Reset. A low to high transition resets the ADAS3022-EP. The current conversion, if active, is aborted and CFG is reset to the default state.
14, 29, 30	NC	N/A	No Connect. This pin is not connected internally.
15	PD	DI	Power-Down. A low to high transition powers down the ADAS3022-EP, minimizing the bias current. Note that this pin must be held high until the user is ready to power on the device; after powering on the device, the user must wait 100 ms until the reference is enabled and then wait for the completion of two dummy conversions before the device is ready to convert.
16	SCK	DI	Serial Clock Input. The DIN and SDO data sent to and from the ADAS3022-EP are synchronized with SCK.

FIGURE 3. Terminal function.

Case outline X - Continued			
Terminal number	**Mnemonic**	**Type**	**Description**
17	VIO	P	Digital Interface Supply. Nominally, this supply is at the same voltage as the supply of the host interface: 1.8 V, 2.5 V, 3.3 V, or 5 V.
18	SDO	DO	Serial Data Output. The conversion result is output on this pin and is synchronized to SCK falling edges. The conversion result is output in twos complement format.
19	BUSY	DO	Busy Output. An active high signal on this pin indicates that a conversion is in process. Reading or writing data during the quiet conversion phase (t_{QUIET}) may cause incorrect bit decisions.
20	CNV	DI	Convert Input. A conversion is initiated on the rising edge of this pin.
21, 22	DGND	P	Digital Ground. Connect these pins to the system digital ground plane.
23, 24	AGND	P	Analog Ground. Connect these pins to the system analog ground plane.
25	DCAP	P	Internal 2.5 V Digital Regulator Output. Decouple this internally regulated output using a 10 µF capacitor and a 0.1 µF local capacitor.
26	ACAP	P	Internal 2.5 V Analog Regulator Output. This regulator supplies power to the internal ADC core and all of the supporting analog circuits with the exception of the internal reference. Decouple this internally regulated output using a 10 µF capacitor and a 0.1 µF local capacitor.
27	DVDD	P	Digital 5 V Supply. Decouple this supply using a 10 µF capacitor and a 0.1 µF local capacitor.
28	AVDD	P	Analog 5 V Supply. Decouple this supply using a 10 µF capacitor and a 0.1 µF local capacitor.
31	RCAP	P	Internal 2.5 V Analog Regulator Output. This regulator supplies power to the internal reference. Decouple this pin using a 1 µF capacitor connected to RCAP and a 0.1 µF local capacitor.
32	REFIN	AI/O	Internal 2.5 V Band Gap Reference Output, Reference Buffer Input, or Reference Power-Down Input. See the Voltage Reference Input/Output section of the ADAS3022 data sheet for more information
33, 34	REF1, REF2	AI/O	Reference Input/Output. Regardless of the reference method, these pins need individual decoupling using external 10 µF ceramic capacitors connected as close to REF1, REF2, and REFN as possible. REF1 and REF2 must be tied together externally.
35	RGND	P	Reference Supply Ground. Connect this pin to the system analog ground plane.
36, 37	REFN	P	Reference Input/Output Ground. Connect the 10 µF capacitors on REF1 and REF2 to these pins, and connect these pins to the system analog ground plane.
38	VSSH	P	High Voltage Analog Negative Supply. Nominally, the supply of this pin should be −15 V. Decouple this pin using a 10 µF capacitor and a 0.1 µF local capacitor.
39	VDDH	P	High Voltage Analog Positive Supply. Nominally, the supply of this pin should be +15 V. Decouple this pin using a 10 µF capacitor and a 0.1 µF local capacitor.
40	AUX-	AI	Auxiliary Input Channel Negative Input.
	EPAD		Exposed Paddle. Connect the exposed paddle to VSSH.

FIGURE 3. Terminal function - Continued.

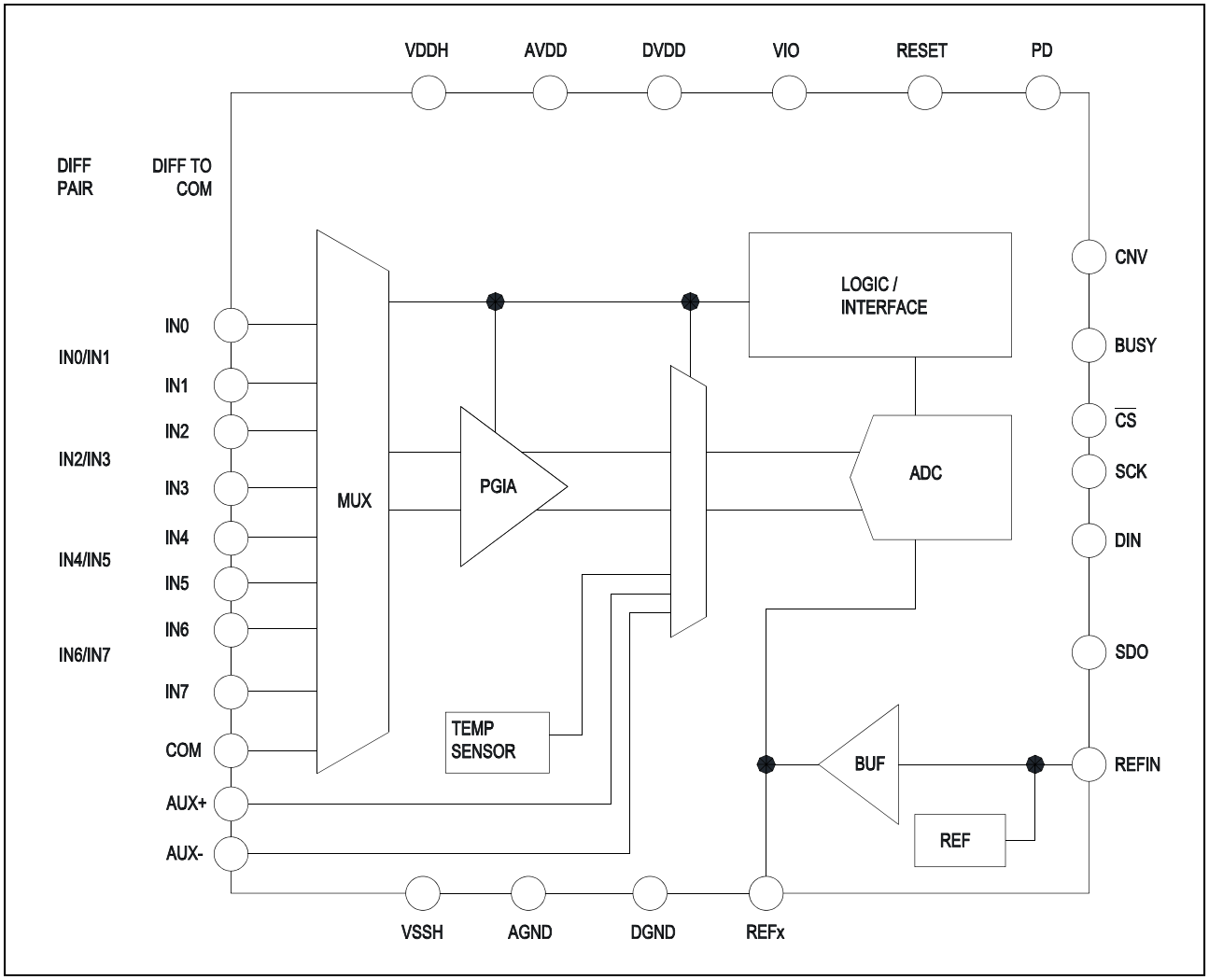


FIGURE 4. Functional block diagram.

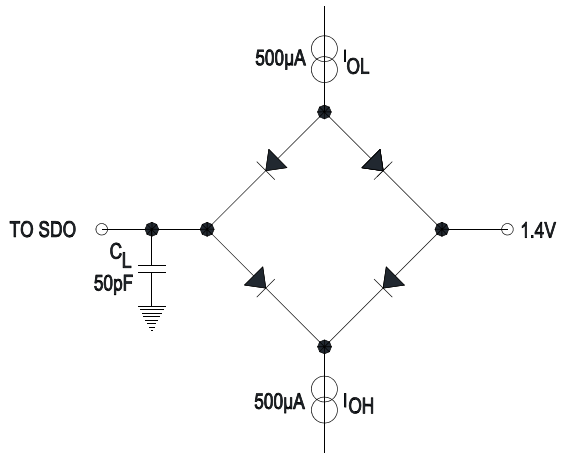
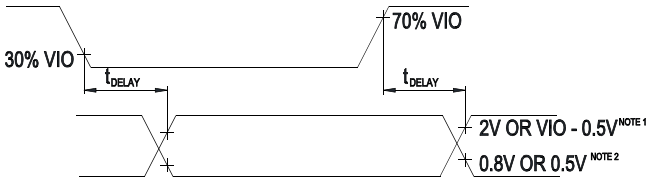
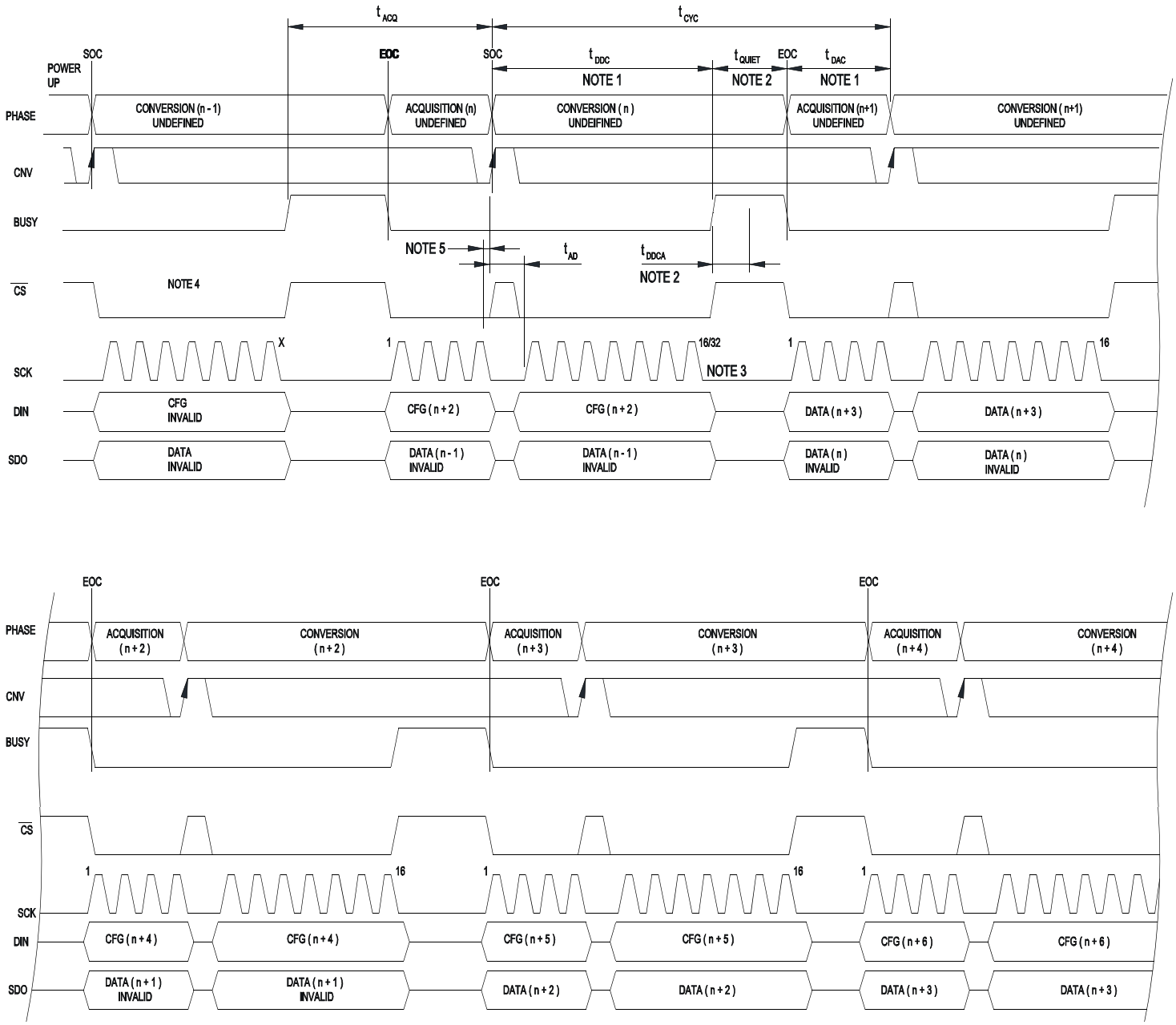


FIGURE 5: Load circuit for Digital Interface.



Notes:
1. 2 V If VIO > 2.5 V; VIO – 0.5 V if VIO < 2.5 V
2. 0.8 V If VIO > 2.5 V; 0.5 V if VIO < 2.5 V

FIGURE 6. Voltage Levels for Timing.



NOTES:

1. Data access can occur during a conversion (t_{DDC}) after conversion (t_{DAC}), or both during and after a conversion. The conversion result and the CFG register are updated at the end of a conversion (EOC).
2. Data access can also occur up to tDDCA while BUSY is active (see ADAS3022 data sheet for details). All of the BUSY time can be used to acquire data.
3. A total of 16 SCK falling edges is required for a conversion result. An addition 16 edges are required to READ back the CFG result associated with the current conversion.
4. $\overline{CS}$ can be held Low or connected to CNV. $\overline{CS}$ will full independent control is shown in this figure.
5. For optimal performance, data access should not occur during the sampling edge. A minimum time of aperture delay (tAD) should elapse prior to data access.

FIGURE 7. General Timing Diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Order Quantity	Vendor part number
V62/17609-01XE	24355	Tray unit = 490	ADAS3022SCPZ-EP
		Reel units = 2500	ADAS3022SCPZ-EP-RL

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106