REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current VID description requirements. - PHN	23-05-22	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
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REV	A	A	A	A	A	A	A	A	A	A	A											
SHEET	1	2	3	4	5	6	7	8	9	10	11											

PMIC N/A

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Original date of drawing

YY MM DD

17-08-21

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TITLE
MICROCIRCUIT, LINEAR-DIGITAL, 0.1 GHz TO 6.0 GHz, 0.5 dB LEAST SIGNIFICANT BIT (LSB), 6-Bit, DIGITAL ATTENUATOR, GALLIUM ARSENIDE (GaAs)

SIZE	CAGE CODE	DWG NO.
A	16236	V62/17606
REV A		PAGE 1 OF 11

AMSC N/A

5962-V092-23

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 0.1 GHz to 6.0 GHz, 0.5 dB LSB, 6 Bit, GaAs Digital Attenuator microcircuit, with an operating temperature range of -55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/17606	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	HMC624A –EP	0.1 GHz to 6.0 GHz, 0.5 dB LSB, 6 Bit, GaAs Digital Attenuator

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	24	JEDEC MO-220-VGGD-8	Lead Frame Chip Scale Package [LFCSP]

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage ..... 5.6 V
Digital Control Input voltage ..... -1 V to V_{DD} + 1 V
RF Input Power 2/ (All Attenuation States, f = 250 MHz to 6 GHz, T_{CASE} = 105°C)
V_{DD} = 3 V ..... 25 dBm
V_{DD} = 5 V ..... 28 dBm
Continuous Power Dissipation, P_{DISS} (T_{CASE} = 105°C) ..... 0.36 W
Temperature:
Junction, T_J ..... 150°C
Operating ..... -55°C to +105°C
Storage ..... -65°C to 150°C
Reflow 3/ (Moisture Sensitivity Level 3 (MSL3) Rating) ..... 260°C
ESD Sensitivity:
Human Body Model (HBM) ..... 300 V

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JC}	Unit
Case X	116	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org).

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ For power derating at frequencies less than 250 MHz, see FIGURE 9.
3/ See the Ordering Guide in Section 6.3 for more information.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 ATTIN, ATTOUT Interface Schematic. The ATTIN, ATTOUT Interface Schematic shall be as shown in figure 5.

3.5.6 ACGx Pin Interface Schematic. The ACGx Pin Interface Schematic shall be as shown in figure 6.

3.5.7 Digital Control Input Interface. The Digital Control Input Interface shall be as shown in figure 7.

3.5.8 SEROUT Pin Interface. The SEROUT Pin Interface shall be as shown in figure 8.

3.5.9 Power Derating at Frequency <250 MHz the Power Derating at Frequency <250 MHz shall be as shown in figure 9.

TABLE I. Electrical performance characteristics. 1/

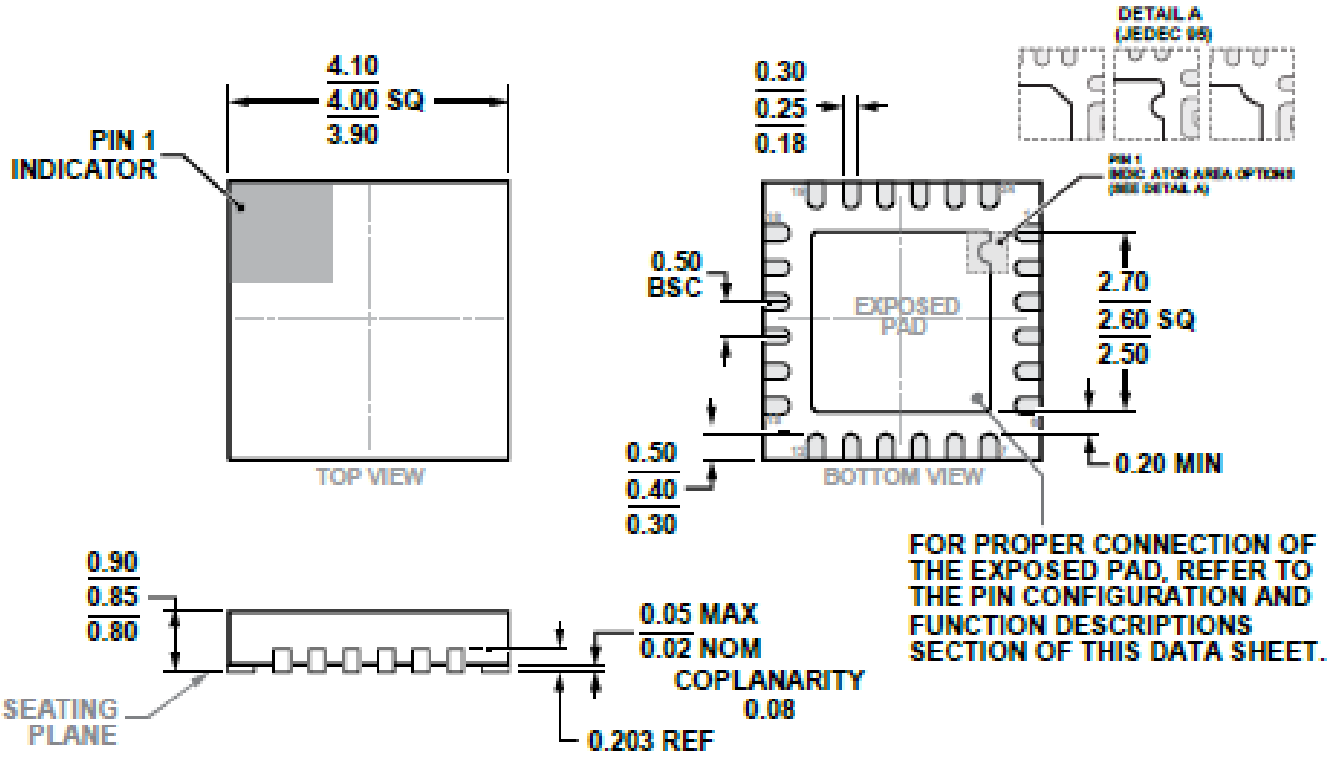
Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
FREQUENCY RANGE			0.1		6.0	GHz
INSERTION LOSS		0.1 GHz to 3 GHz		1.6	2.4	dB
		3 GHz to 6.0 GHz		2.3	3.8	dB
ATTENUATION		0.1 GHz to 6.0 GHz				
Range		Between minimum and maximum attenuation states		31.5		dB
Step Size		Between any successive attenuation states		0.5		dB
Step Error		Between any successive attenuation states		<±0.2		dB
State Error		All attenuation states, referenced to insertion loss state				
0.1 GHz to 0.8 GHz			−(0.1 + 5% of attenuation state)		+(0.1 + 5% of attenuation state	dB
0.8 GHz to 6.0 GHz			−(0.3 + 3% of attenuation state)		+(0.3 + 3% of attenuation state)	dB
RETURN LOSS (ATTIN and ATTOUT)		All attenuation states, 0.1 GHz to 6.0 GHz		15		dB
RELATIVE PHASE		Between minimum and maximum attenuation states				
100 MHz to 3 GHz				25		Degrees
3 GHz to 6.0 GHz				50		Degrees
SWITCHING CHARACTERISTICS		Between all attenuation states				
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		60		ns
On and Off Time	t_{ON}, t_{OFF}	50% VCTL to 90% of RF output		90		ns
INPUT LINEARITY 3/		All attenuation states, 250 MHz to 6.0 GHz				
0.1 dB Compression	P0.1dB	V_{DD} = 3 V		27		dBm
		V_{DD} = 5 V		33		dBm
Third-Order Intercept	IP3	V_{DD} = 3 V to 5 V, 10 dBm per tone, 1 MHz spacing		55		dBm
SUPPLY CURRENT	I_{DD}	V_{DD} = 3 V to 5 V		3		mA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
DIGITAL CONTROL INPUTS		P/S, CLK, SERIN, LE, D0 to D5, PUP1, and PUP2 pins				
Voltage						
Low	V_{INL}	V_{DD} = 3 V	0		0.5	V
		V_{DD} = 5 V	0		0.8	V
High	V_{INH}	V_{DD} = 3 V	2		3	V
		V_{DD} = 5 V	2		5	V
Current		V_{DD} = 3 V to 5 V				
Low	I_{INL}			15		µA
High	I_{INH}			65		µA
DIGITAL CONTROL OUTPUT		SEROUT				
Voltage						
Low	V_{OUTL}			0		V
High	V_{OUTL}			V_{DD}		V
Current						
Low	I_{OUTL}				1	mA
High	I_{OUTH}				1	mA
TIMING SPECIFICATIONS						
Minimum serial period	t_{SCK}		70			ns
Control setup time	t_{CS}		15			
Control hold time	t_{CH}			20		
LE setup time	t_{LN}		15			
Minimum LE pulse width	t_{LEW}			10		
Minimum LE pulse spacing	t_{LES}			630		
Serial clock hold time from LE	t_{CKN}			0		
Data hold time from LE	t_{PH}			10		
Data setup time to LE	t_{PS}			2		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ V_{DD} = 3 V to 5 V, control input voltage (V_{CTL}) = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.
3/ Input linearity performance degrades at frequencies less than 250 MHz; see Figure in manufacturer data sheet.



NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-220-VGGD-8.
3. For proper connection of the Exposed PAD, Refer to the Terminal Configuration and Terminal functions section of this data sheet.

FIGURE 1. Case outline.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P/S	24	D0
2	CLK	23	D1
3	SERIN	22	D2
4	LE	21	D3
5	GND	20	D4
6	ATTIN	19	D5
7	ACG1	18	VDD
8	ACG2	17	PUP1
9	ACG3	16	PUP2
10	ACG4	15	SEROUT
11	ACG5	14	GND
12	ACG6	13	ATTOUT

NOTES:
1. The EXPOSED PAD must be connected to ground for proper operation.

FIGURE 2. Terminal connections.

Terminal Number	Mnemonic	Description
1	P/S	Parallel/Serial Mode Select. For parallel mode operation, set this pin to low. For serial mode operation, set this pin to high.
2	CLK	Serial Interface Clock Input.
3	SERIN	Serial Interface Data Input.
4	LE	Latch Enable Input.
5, 14	GND	Ground. These pins must be connected to ground.
6	ATTIN	Attenuator RF Input. This pin can also be used as an output because the design is bidirectional. ATTIN is dc-coupled and ac matched to 50 Ω. An external dc blocking capacitor is required
7 to 12	ACG1 to ACG6	AC Grounding Capacitor Pins. These pins can be left unconnected when operating above 700 MHz. For frequencies less than 700 MHz, connect capacitors larger than 100 pF as close to the ACGx pins as possible. Select the capacitor value for the lowest frequency of operation.
13	ATOUT	Attenuator RF Output. This pin can also be used as an input because the design is bidirectional. ATTOUT is dc-coupled and ac matched to 50 Ω. An external dc blocking capacitor is required.
15	SEROUT	Serial Interface Data Output. Serial input data is delayed by six clock cycles.
16, 17	PUP2, PUP1	Power-Up State Selection Pins. These pins set the attenuation value at power-up.
18	VDD	Power Supply.
19 to 24	D5 to D0	Parallel Control Voltage Inputs. These pins select the required attenuation. There is no internal pull-up or pull-down resistor on these pins; therefore, they must always be kept at a valid logic level (VIH or VIL) and not be left floating.
	EPAD	Exposed Pad. The exposed pad must be connected to ground for proper operation

FIGURE 3. Terminal function.

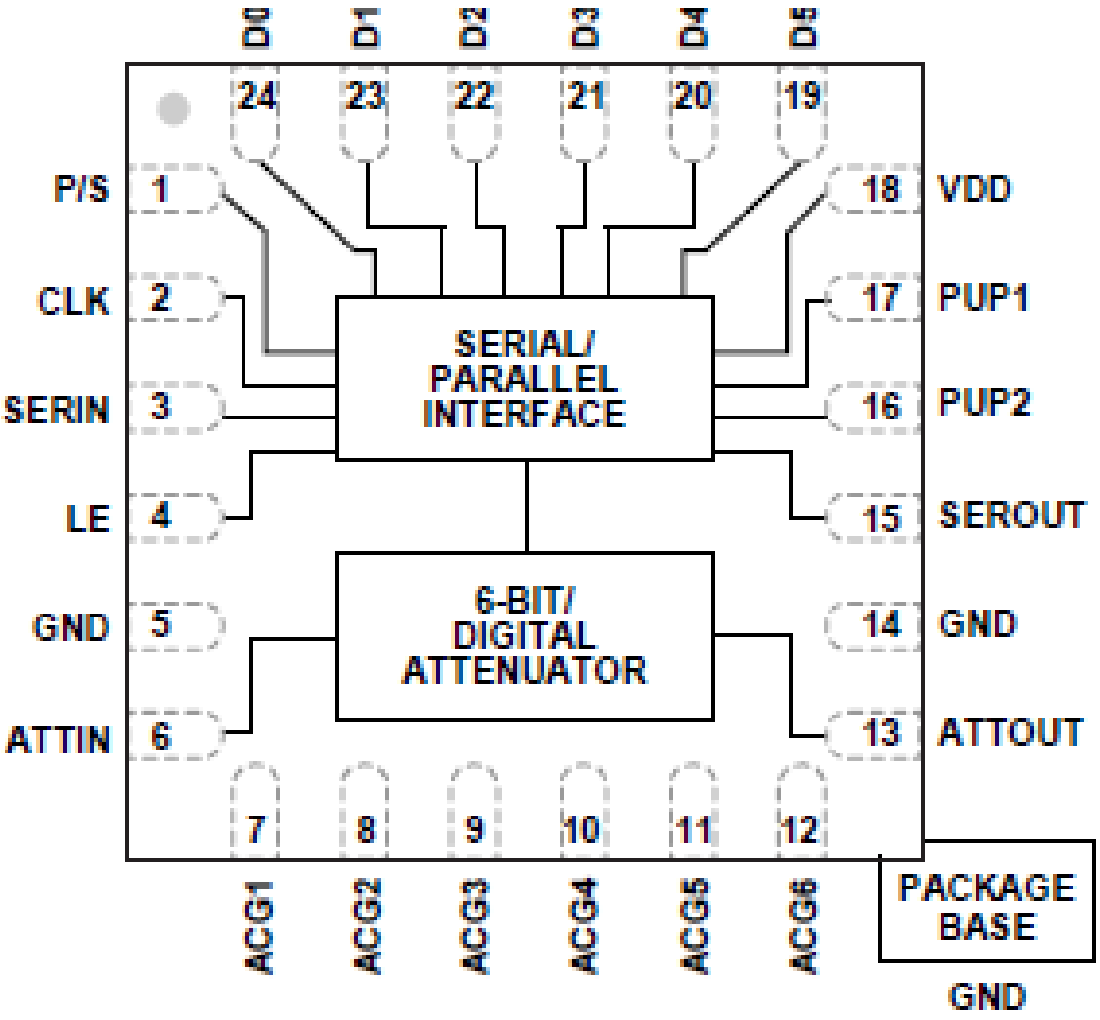


FIGURE 4. Functional block diagram.

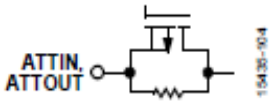


FIGURE 5. ATTIN, ATTOUT Interface Schematic.

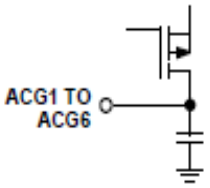


FIGURE 6. ACGx Pin Interface Schematic.

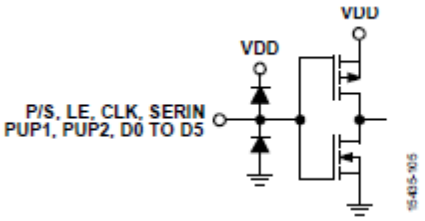


FIGURE 7. Digital Control Input Interface.

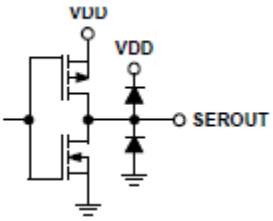


FIGURE 8. SEROUT Pin Interface.

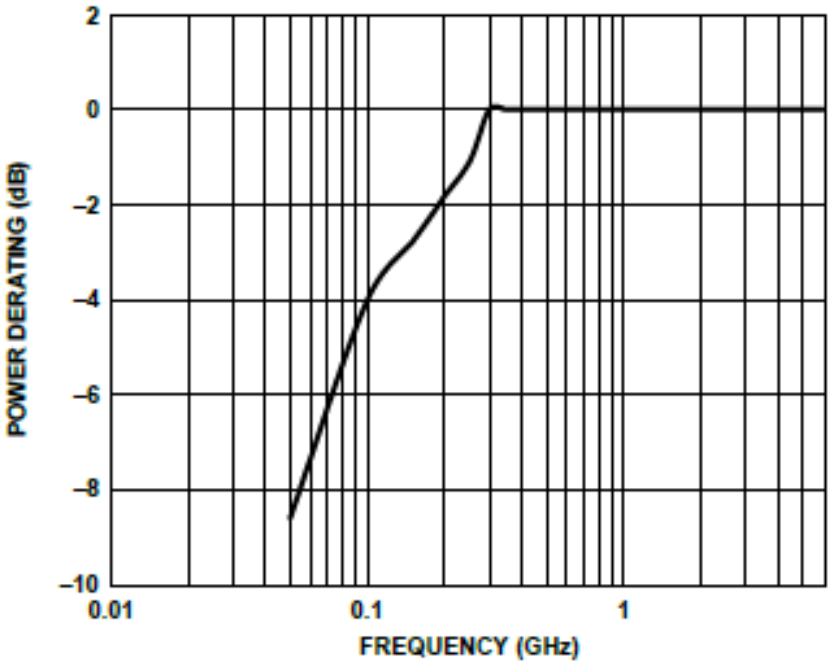


FIGURE 9. Power Derating at Frequency <250 MHz.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	MSL Rating 2/	Order Quantity	Vendor part number
V62/17606-01XE	24355	MSL3	Tray units = 50	HMC624ACPSZ-EP-PT
		MSL3	Reel units = 500	HMC624ACPSZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ See the Absolute Maximum rating in Section 1.3

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106