REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Under paragraph 6.3, delete the tube quantity of 36 units and replace with 96 units. - ro	17-06-05	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	A	A																			
PAGE	18	19																			

REV STATUS OF PAGES	**REV**	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil/

Original date of drawing
YY-MM-DD

17-04-17

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

TITLE

MICROCIRCUIT, DIGITAL-LINEAR, MULTIPLE RANGE, 16 BIT, BIPOLAR/UNIPOLAR VOLTAGE OUTPUT DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**	**DWG NO.**
A	**16236**	**V62/17605**

REV **A**

PAGE 1 **OF** 19

AMSC N/A

5962-V061-17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance multiple range, 16 bit, bipolar/unipolar voltage output digital to analog converter (DAC) with 7 ppm/°C reference microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/17605	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5761R-EP	Multiple range, 16 bit, bipolar/unipolar voltage output digital to analog converter (DAC) with 7 ppm/°C reference

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-153-AB	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Positive analog supply voltage (V_{DD}) to analog ground (AGND) ..... -0.3 V to +34 V
Negative analog supply voltage (V_{SS}) to analog ground (AGND) ..... +0.3 V to -17 V
V_{DD} to V_{SS} ..... -0.3 V to +34 V
Digital supply voltage (DV_{CC}) to digital ground (DGND) ..... -0.3 V to +7 V
Digital inputs to DGND ..... -0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital outputs to DGND ..... -0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Internal reference voltage output (V_{REFIN}) / External reference voltage input (V_{REFOUT}) to DGND ..... -0.3 V to +7 V
Analog output (V_{OUT}) to AGND ..... V_{SS} to V_{DD}
AGND to DGND ..... -0.3 V to +0.3 V
Storage temperature range ..... -65°C to +150°C
Junction temperature range (T_J) ..... +150°C
Power dissipation (P_D) ..... See figure 4
Electrostatic discharge (ESD):
Human body model (HBM) ..... 4 kV
Thermal resistance, junction to ambient (θ_{JA}) ..... 113°C/W 3/

1.4 Recommended operating conditions. 4/

Operating temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Unless otherwise specified, T_A = +25°C. Transient currents of up to 200 mA do not cause silicon controlled rectifier (SCR) latch up.
3/ JEDEC 2S2P test board, still air (0 m/sec airflow).
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Maximum power dissipation. The maximum power dissipation shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Static performance.	External reference 3/ and terminal reference, outputs unloaded.						
Programmable output ranges			-55°C to +125°C	01	0	5	V
					0	10	
					0	16	
					0	20	
					-2.5	+7.5	
					-3	+3	
					-5	+5	
					-10	+10	
Resolution			-55°C to +125°C	01	16		Bits
Relative accuracy (INL)		External reference 3/ and internal reference	-55°C to +125°C	01	-8	+8	LSB
Differential nonlinearity (DNL)			-55°C to +125°C	01	-1	+1	LSB
Zero scale error		All ranges except ±10 V and 0 V to 20 V, external reference 3/	-55°C to +125°C	01	-6	+6	mV
		0 V to 20 V, ±10 V ranges, external references 3/			-10	+10	
		All ranges except ±5 V, ±10 V, and 0 V to 20 V, internal reference			-6	+6	
		±5 V range, internal reference			-8	+8	
		0 V to 20 V range, internal reference			-9	+9	
		±10 V range, internal reference			-13	+13	
Zero scale temperature coefficient (TC) 4/		Unipolar ranges, external reference 3/ and internal reference	+25°C	01	±5 typical		µV/°C
		Bipolar ranges, external reference 3/ and internal reference			±15 typical		
Bipolar zero error		All bipolar ranges except ±10 V	-55°C to +125°C	01	-5	+5	mV
		±10 V output range			-7	+7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Static performance – continued.		External reference 3/ and terminal reference, outputs unloaded.					
Bipolar zero 4/ temperature coefficient (TC)		±3 V range, external reference 3/ and internal reference	+25°C	01	±2 typical		µV/°C
		All bipolar ranges except ±3 V range, external reference 3/ and internal reference			±5 typical		
Offset error		All ranges except ±10 V and 0 V to 20 V, external reference 3/	-55°C to +125°C	01	-6	+6	mV
		0 V to 20 V, ±10 V ranges, external reference 3/			-10	+10	
		All ranges except ±5 V, ±10V, and 0 V to 20 V, internal reference			-6	+6	
		±5 V range, internal reference			-8	+8	
		0 V to 20 V range, internal reference			-9	+9	
		±10 V range, internal reference			-18	+18	
Offset error 4/ temperature coefficient (TC)		Unipolar ranges, external reference 3/ and internal reference	+25°C	01	±5 typical		µV/°C
		Bipolar ranges, external reference 3/ and internal reference			±15 typical		
Gain error		External reference 3/	-55°C to +125°C	01	-0.1	+0.1	%FSR
		Internal reference			-0.15	+0.15	
Gain error temperature coefficient (TC) 4/		External reference 3/ and internal reference	+25°C	01	±1.5 typical		ppm FSR/ °C
Total unadjustable error	TUE	External reference 3/	-55°C to +125°C	01	-0.1	+0.1	%FSR
		Internal reference			-0.15	+0.15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Reference input (external) 4/							
Reference input voltage	V_{REF}	±1% for specified performance	+25°C	01	2.5 typical		V
Input current			+25°C	01	±0.5 typical		µA
			-55°C to +125°C		-2	+2	
Reference range			-55°C to +125°C	01	2	3	V
Reference input (internal) 4/							
Output voltage		±3 mV, at ambient temperature	+25°C	01	2.5 typical		V
Voltage reference temperature coefficient (TC)			+25°C	01	7 typical		ppm/°C
			-55°C to +125°C			25	
Output impedance			+25°C	01	25 typical		kΩ
Output voltage noise		0.1 Hz to 10 Hz	+25°C	01	6 typical		µVp-p
Noise spectral density		At ambient; f = 10 kHz	+25°C	01	10 typical		nV/$\sqrt{Hz}$
Line regulation			+25°C	01	6 typical		µV/V
Thermal hysteresis		First temperature cycle	+25°C	01	±80 typical		ppm
Start up time		Coming out of power down mode with a 10 nF capacitor on the V_{REFIN}/V_{REFOUT} pin improves noise performance; outputs unloaded	+25°C	01	3.5 typical		ms

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output characteristics 4/							
Output voltage range		See the device data sheet for the different output voltage ranges available.	-55°C to +125°C	01	$-V_{OUT}$	$+V_{OUT}$	
		V_{DD}/V_{SS} = ±11 V, ±10 V output range			-10	+10	V
		V_{DD}/V_{SS} = ±11 V, ±10 V output range with 5% overrange			-10.5	+10.5	
Capacitive load stability			-55°C to +125°C	01		1	nF
Headroom		R_{LOAD} = 1 kΩ for all ranges except 0 V to 16 V and 0 V to 20 V ranges (R_{LOAD} = 2 kΩ)	+25°C	01	0.5 typical		V
			-55°C to +125°C			1	
Output voltage temperature coefficient (TC)		±10 V range, external reference	+25°C	01	±3 typical		ppm FSR/ °C
Short circuit current		Short on the V_{OUT} pin	+25°C	01	25 typical		mA
Resistive load		All ranges except 0 V to 16 V and 0 V to 20 V	-55°C to +125°C	01		1	kΩ
		0 V to 16 V, 0 V to 20 V ranges				2	
Load regulation		Outputs unloaded	+25°C	01	0.3 typical		mV/mA
DC output impedance		Outputs unloaded	+25°C	01	0.5 typical		Ω
Logic inputs 4/	DV_{CC} = 1.7 V to 5.5 V, JEDEC compliant						
Input voltage high	V_{IH}		-55°C to +125°C	01	0.7 x DV_{CC}		V
Input voltage low	V_{IL}		-55°C to +125°C	01		0.3 x DV_{CC}	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Logic inputs – continued. 4/		DV_{CC} = 1.7 V to 5.5 V, JEDEC compliant					
Input current, leakage current		SDI, SCLK, $\overline{SYNC}$	-55°C to +125°C	01	-1	+1	µA
		$\overline{LDAC}$, $\overline{CLEAR}$, $\overline{RESET}$ pins held high			-1	+1	
		$\overline{LDAC}$, $\overline{CLEAR}$, $\overline{RESET}$ pins held low			-55		
Pin capacitance		Per pin, outputs unloaded	+25°C	01	5 typical		pF
Logic outputs		(SDO, $\overline{ALERT}$) 4/					
Output voltage low	V_{OL}	DV_{CC} = 1.7 V to 5.5 V, sinking 200 µA	-55°C to +125°C	01		0.4	V
Output voltage high	V_{OH}	DV_{CC} = 1.7 V to 5.5 V, sourcing 200 µA	-55°C to +125°C	01	DV_{CC} – 0.5		V
High impedance, SDO pin, leakage current			-55°C to +125°C	01	-1	+1	µA
Pin capacitance			+25°C	01	5 typical		pF
Power requirements							
Single supply	V_{DD}		-55°C to +125°C	01	4.75	30	V
	V_{SS}		+25°C		0 typical		
Dual supply	V_{DD}		-55°C to +125°C	01	4.75	16.5	V
	V_{SS}				-16.5	0	
	DV_{CC}				1.7	5.5	
	I_{DD}	Outputs unloaded, external reference	+25°C		5.1 typical		mA
			-55°C to +125°C			6.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power requirements – continued.							
Dual supply – continued.	I_{SS}	Outputs unloaded	+25°C	01	1 typical		mA
			-55°C to +125°C			3	
	DI_{CC}	V_{IH} = DV_{CC}, V_{IL} = DGND	+25°C		0.005 typical		µA
			-55°C to +125°C			1	
Power dissipation		±11 V operation, output unloaded	+25°C	01	67.1 typical		mW
DC power supply rejection ratio 4/	PSRR	V_{DD} ± 10%, V_{SS} = -15 V	+25°C	01	0.1 typical		mV/V
		V_{SS} ± 10%, V_{SS} = +15 V			0.1 typical		
AC power supply rejection ratio 4/	PSRR	V_{DD} ±200 mV, 50 Hz/60 Hz, V_{SS} = -15 V, internal reference, C_{LOAD} = 100 pF	+25°C	01	65 typical		dB
		V_{SS} ±200 mV, 50 Hz/60 Hz, V_{DD} = +15 V, internal reference, C_{LOAD} = 100 pF			65 typical		
		V_{DD} ±200 mV, 50 Hz/60 Hz, V_{SS} = -15 V, external reference, C_{LOAD} = unloaded			80 typical		
		V_{SS} ±200 mV, 50 Hz/60 Hz, V_{DD} = +15 V, external reference, C_{LOAD} = unloaded			80 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC performance characteristics.							
Dynamic performance							
Output voltage settling time		20 V step to 1 LSB at 16 bit resolution	+25°C	01	9 typical		μs
			-55°C to +125°C			12.5	
		10 V step to 1 LSB at 16 bit resolution	+25°C		7.5 typical		
			-55°C to +125°C			8.5	
		512 LSB step to 1 LSB at 16 bit resolution	-55°C to +125°C			5	
Digital to analog glitch impulse		±10 V range	+25°C	01	8 typical		nV-sec
		0 V to 5 V range			1 typical		
Glitch impulse peak amplitude		±10 V range	+25°C	01	15 typical		mV
		0 V to 5 V range			10 typical		
Power on glitch			+25°C	01	100 typical		mVp-p
Digital feedthrough			+25°C	01	0.6 typical		nV-sec
Output noise, 0.1 Hz to 10 Hz bandwidth			+25°C	01	15 typical		μVp-p
Output noise, 100 kHz bandwidth		0 V to 20 V and 0 V to 16 V ranges, 2.5 V external reference	+25°C	01	45 typical		μV rms
		0 V to 10 V, ±10 V, and -2.5 V to +7.5 V ranges, 2.5 V external reference			35 typical		
		±5 V range, 2.5 V external reference			25 typical		
		0 V to 5 V and ±3 V ranges, 2.5 V external reference			15 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC performance characteristics - continued.							
Dynamic performance - continued.							
Output noise spectral density at 10 kHz		±10 V range, 2.5 V external reference	+25°C	01	80 typical		nV/$\sqrt{Hz}$
		±3 V range, 2.5 V external reference			35 typical		
		±5 V, 0 V to 10 V, and -2.5 V to +7.5 V ranges, 2.5 V external reference			70 typical		
		0 V to 20 V range, 2.5 V external reference			110 typical		
		0 V to 16 V range, 2.5 V external reference			90 typical		
		0 V to 5 V range, 2.5 V external reference			45 typical		
Total harmonic distortion 5/	THD	2.5 V external reference, 1 kHz tone	+25°C	01	-87 typical		dB
Signal to noise ratio	SNR	At ambient, 2.5 V external reference, bandwidth (BW) = 20 kHz, f_{OUT} = 1 kHz	+25°C	01	92 typical		dB
Peak harmonic or spurious noise	SFDR	At ambient, 2.5 V external reference, bandwidth (BW) = 20 kHz, f_{OUT} = 1 kHz	+25°C	01	92 typical		dB
Signal to noise and distortion (SINAD) ratio	SNR	At ambient, 2.5 V external reference, bandwidth (BW) = 20 kHz, f_{OUT} = 1 kHz	+25°C	01	85 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} 7/ = 4.75 V to 30 V, V_{SS} 7/ = -16.5 V to 0 V, AGND = DGND = 0 V, V_{REFIN}/V_{REFOUT} = 2.5 V external, DV_{CC} = 1.7 V to 5.5 V, R_{LOAD} = 1 kΩ for all ranges except 0 V to 16 V and 0 V to 20 V for which R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, and all specifications T_{MIN} to T_{MAX}. Temperature range: -55°C to +125°C.

3/ External reference is 2 V to 2.85 V with overrange and 2 V to 3 V without overange.

4/ Guaranteed by design and characterization, not production tested.

5/ Digitally generated sine wave at 1 kHz.

6/ Unless otherwise specified, V_{DD} 7/ = 4.75 V to 30 V, V_{SS} 7/ = -16.5 V to 0 V, AGND = DGND = 0 V, V_{REFIN}/V_{REFOUT} = 2.5 V external, DV_{CC} = 1.7 V to 5.5 V, R_{LOAD} = 1 kΩ for all ranges except 0 V to 16 V and 0 V to 20 V for which R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, and all specifications T_{MIN} to T_{MAX}. Temperature range: -55°C to +125°C. Guaranteed by design and characterization, not production tested.

7/ For specified performance, headroom requirements is 1 V. V_{DD} = 4.75 V to 30 V and V_{SS} = 0 V for single supply operation , and V_{DD} = 4.75 V to 16.5 V and V_{SS} = -16.5 V to 0 V for dual supply operation.

Case X

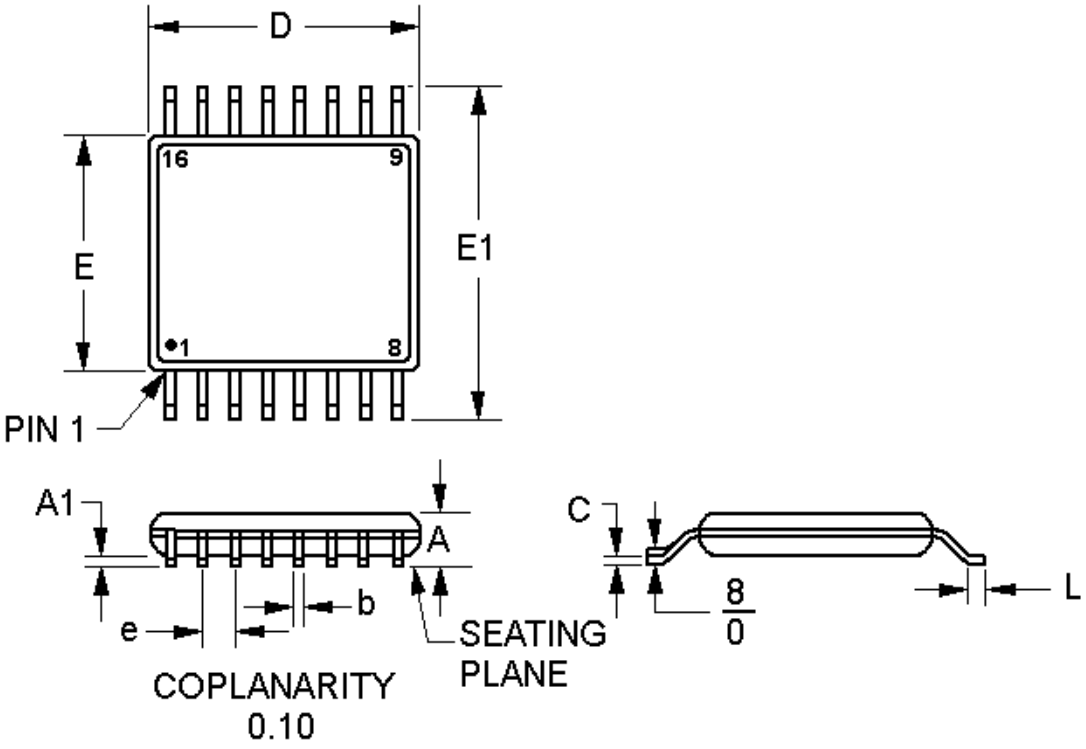

FIGURE 1. Case outline.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Medium	Maximum	Minimum	Medium	Maximum
A	---	---	.0472	---	---	1.20
A1	.0019	---	.0059	0.05	---	0.15
b	.0074	---	.0118	0.19		0.30
c	.0035	---	.0078	0.09	---	0.20
D	.1929	.1968	.2007	4.90	5.00	5.10
e	.0225 BSC			0.65 BSC		
E	.1692	.1733	.1771	4.30	4.40	4.50
E1	.2519 BSC			6.40 BSC		
L	.0177	.0236	.0295	0.45	0.60	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-153-AB.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	$\overline{\text{ALERT}}$	Active low alert. This pin is asserted low when the die temperature exceeds approximately 150°C, or when an output short circuit or a brownout occurs. This pin is also asserted low during power up, a full software reset, or a hardware rest for which a write to the control register asserts the pin high.
2	$\overline{\text{CLEAR}}$	Falling edge clear input. Asserting this pin sets the DAC register to zero scale, midscale, or full scale code (user selectable) and updates the DAC output. This pin can be left floating because there is an internal pull up resistor.
3	$\overline{\text{RESET}}$	Active low reset input. Asserting this pin returns the device to its default power on status where the output is clamped to ground, and the output buffer is powered down. This pin can be left floating because there is an internal pull up resistor.
4	V_{REFIN}/ V_{REFOUT}	Internal reference voltage output and external reference voltage input. For specified performance, V_{REFIN}/V_{REFOUT} = 2.5 V. Connect a 10 nF capacitor with the internal reference to minimize the noise.
5	AGND	Ground reference pin for analog circuitry.
6	V_{SS}	Negative analog supply connection. A voltage in the range of -16.5 V to 0 V can be connected to this pin. For unipolar output ranges, connect this pin to 0 V. V_{SS} must be decoupled to AGND.
7	V_{OUT}	Analog output voltage of the DAC. The output amplifier is capable of directly driving a 2 kΩ, 1 nF load.
8	V_{DD}	Positive analog supply connection. A voltage in the range of 4.75 V to 30 V can be connected to this pin for unipolar output ranges. Bipolar output ranges accept a voltage in the range of 4.75 V to 16.5 V V_{DD} must be decoupled to AGND.
9	DNC	Do not connect. Do not connect to this pin.
10	SDO	Serial data output. This pin clock data from the serial register in daisy chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
11	$\overline{\text{LDAC}}$	Load DAC. This logic input updates the DAC register and, consequently, the analog output. When tied permanently low, the DAC register is updated when the input register is updated. If $\overline{\text{LDAC}}$ is held high during the write to the input register, the DAC output register is not updated, and the DAC output update is held off until the falling edge of $\overline{\text{LDAC}}$. This pin can be left floating because there is an internal pull up resistor.

FIGURE 2. Terminal connections.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
12	SDI	Serial data input. Data must be valid on the falling edge of SCLK.
13	$\overline{\text{SYNC}}$	Active low synchronization input. This pin is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, is transferred in on the falling edge of SCLK. Data is latched on the rising edge of $\overline{\text{SYNC}}$.
14	SCLK	Serial clock input. Data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds of up to 50 MHz.
15	DV_{CC}	Digital supply. The voltage range is from 1.7 V to 5.5 V. The applied voltage sets the voltage at which the digital interface operates.
16	DGND	Digital ground.

FIGURE 2. Terminal connections - continued.

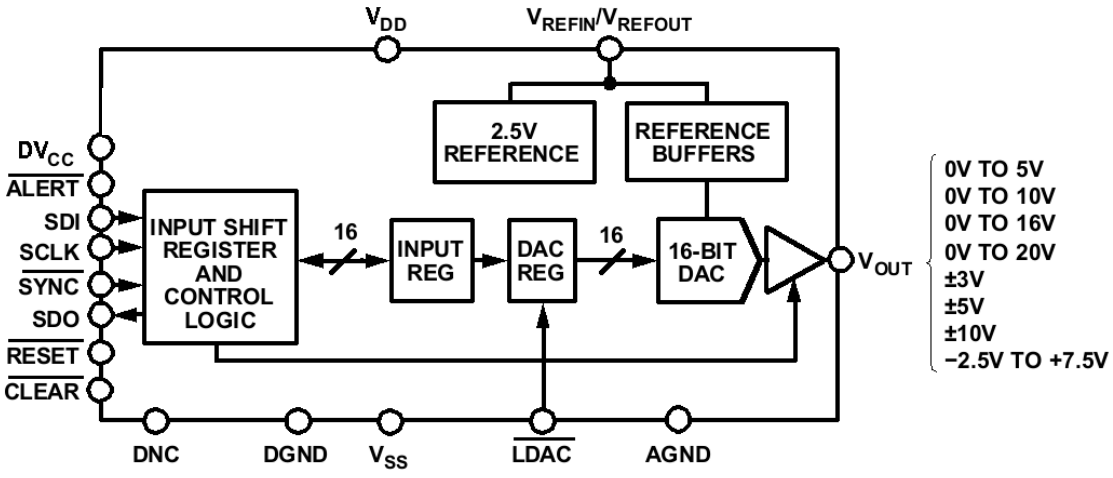

FIGURE 3. Block diagram.

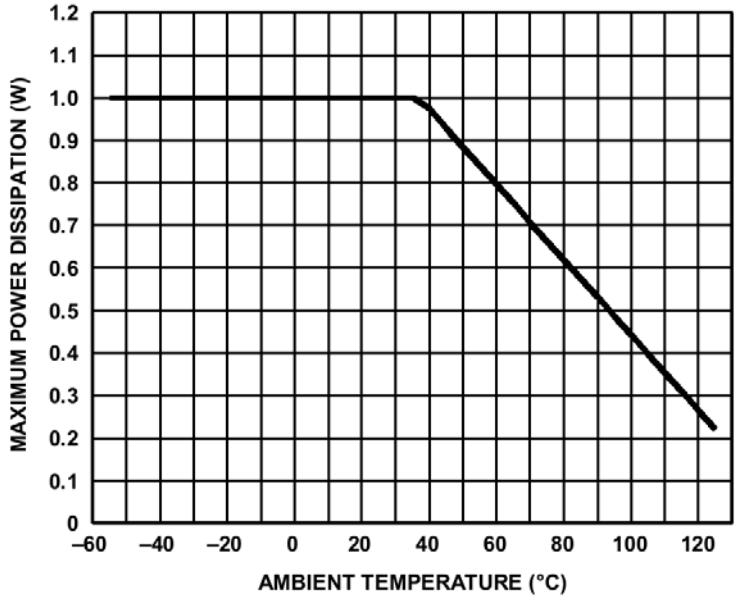

FIGURE 4. Maximum power dissipation.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/17605-01XE	24355	Tube, 96 units	AD5761RTRUZ-EP
V62/17605-01XE	24355	Reel, 1,000 units	AD5761RTRUZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland