REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 17-02-22	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	**TITLE** MICROCIRCUIT, LINEAR, HIGH STABILITY, ISOLATED ERROR AMPLIFIER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/17602**
	REV	**PAGE** 1 **OF** 15

AMSC N/A

5962-V030-17

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high stability, isolated error amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/17602	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADuM4190	High stability, isolated error amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-013-AC	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range: 2/
- V_{DD1}, V_{DD2} ..... -0.5 V to +24 V
- V_{REG1}, V_{REG2} ..... -0.5 V to +3.6 V

Input voltage range (+IN, -IN) ..... -0.5 V to +3.6 V
Output voltage range:
- REFOUT, REFOUT1, COMP, EAOUT ..... -0.5 V to +3.6 V
- EAOUT2 ..... -0.5 V to +5.5 V

Output current per output pin range ..... -11 mA to +11 mA
Common mode transients range ..... -100 kV/μs to +100 kV/μs 3/
Junction temperature range (T_J) ..... -55°C to +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 4/

Supply voltages (V_{DD1}, V_{DD2}) ..... 3.0 V to +20 V 2/
Input signal rise and fall times (t_R, t_F) ..... 1.0 ms maximum
Ambient operating temperature range (T_A) ..... -55°C to +125°C

1.5 Maximum continuous working voltage. 5/

AC voltage at a 50 year minimum lifetime:
- Bipolar waveform ..... 560 V peak maximum
- Unipolar waveform ..... 1131 V peak maximum

DC voltage at a 50 year minimum lifetime ..... 1131 V peak maximum

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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltages are relative to their respective grounds.

3/ Refers to common mode transients across the insulation barrier. Common mode transients exceeding the absolute maximum ratings may cause latch up or permanent damage.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

5/ Refers to the continuous voltage magnitude imposed across the isolation barrier.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Accuracy	(1.225 V – EA_{OUT}) / 1.225 V x 100%, see figure 4						
Initial error			25°C	01		0.5	%
					0.25 typical		
Total error			-55°C to +125°C	01		1	%
					0.5 typical		
Operational amplifier							
Offset error voltage			-55°C to +125°C	01	-5	+5	mV
			25°C		±2.5 typical		
Open loop gain			-55°C to +125°C	01	66		dB
			25°C		80 typical		
Input common mode range			-55°C to +125°C	01	0.35	1.5	V
Gain bandwidth product			25°C	01	10 typical		MHz
Common mode rejection			25°C	01	72 typical		dB
Input capacitance			25°C	01	2 typical		pF
Output voltage range		COMP pin	-55°C to +125°C	01	0.2	2.7	V
Input bias current			25°C	01	0.01 typical		µA
Reference							
Output voltage		0 mA to 1 mA load, C_{REFOUT} = 15 pF	25°C	01	1.215	1.235	V
					1.225 typical		
			-55°C to +125°C		1.213	1.237	
					1.225 typical		
Output current		C_{REFOUT} = 15 pF	-55°C to +125°C	01	2.0		mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Undervoltage lock out (UVLO)							
Positive going threshold			-55°C to +125°C	01		2.96	V
			25°C		2.8 typical		
Negative going threshold			-55°C to +125°C	01	2.4		V
			25°C		2.6 typical		
EAOUT impedance		V_{DD2} or V_{DD1} < UVLO threshold	25°C	01	High-Z typical		Ω
Output characteristics.		See figure 5					
Output gain 3/		From COMP to EA_{OUT},	-55°C to +125°C	01	0.83	1.17	V/V
		0.4 V to 2.1 V, ±3 mA	25°C		1.0 typical		
		From EA_{OUT} to EA_{OUT2},	-55°C to +125°C		2.5	2.7	
		0.4 V to 2.1 V, ±1 mA, V_{DD1} = 20 V	25°C		2.6 typical		
Output offset voltage		From COMP to EA_{OUT},	-55°C to +125°C	01	-0.4	+0.4	V
		0.4 V to 2.1 V, ±3 mA	25°C		+0.05 typical		
		From EA_{OUT} to EA_{OUT2},	-55°C to +125°C		-0.1	+0.1	
		0.4 V to 2.1 V, ±1 mA, V_{DD1} = 20 V	25°C		+0.01 typical		
Output linearity 4/		From COMP to EA_{OUT},	-55°C to +125°C	01	-1.0	+1.0	%
		0.4 V to 2.1 V, ±3 mA	25°C		+0.15 typical		
		From EA_{OUT} to EA_{OUT2},	-55°C to +125°C		-1.0	+1.0	
		0.4 V to 2.1 V, ±1 mA, V_{DD1} = 20 V	25°C		+0.1 typical		
Output -3 dB bandwidth		From COMP to EA_{OUT}, 0.4 V to 2.1 V, ±3 mA and from COMP to EA_{OUT2}, 0.4 V to 2.1 V, ±1 mA, V_{DD1} = 20 V	-55°C to +125°C	01	250		kHz
			25°C		400 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output characteristics – continued. See figure 5							
Output voltage							
EA_{OUT} low voltage		±3 mA output	-55°C to +125°C	01		0.4	V
EA_{OUT} high voltage		±3 mA output	-55°C to +125°C	01	2.4		V
			25°C		2.5 typical		
EA_{OUT2} low voltage		±1 mA output,	-55°C to +125°C	01		0.6	V
		V_{DD1} = 4.5 V to 5.5 V	25°C		0.3 typical		
		±1 mA output,	-55°C to +125°C			0.6	
		V_{DD1} = 10 V to 20 V	25°C		0.3 typical		
EA_{OUT2} high voltage		±1 mA output,	-55°C to +125°C	01	4.8		V
		V_{DD1} = 4.5 V to 5.5 V	25°C		4.9 typical		
		±1 mA output,	-55°C to +125°C		5.0		
		V_{DD1} = 10 V to 20 V	25°C		5.4 typical		
Noise		See figure 6					
EA_{OUT}			25°C	01	1.7 typical		mVrms
EA_{OUT2}			25°C	01	4.8 typical		mVrms

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply.							
Side 1 operating range		V_{DD1}	-55°C to +125°C	01	3.0	20	V
Side 2 operating range		V_{DD2}	-55°C to +125°C	01	3.0	20	V
Power supply rejection		DC, $V_{DD1} = V_{DD2}$ = 3.0 V to 20 V	-55°C to +125°C	01	60		dB
Supply current	I_{DD1}	See figure 7	-55°C to +125°C	01		2.0	mA
			25°C		1.4 typical		
	I_{DD2}	See figure 8	-55°C to +125°C			5.0	
			25°C		2.9 typical		
Package characteristics.							
Input to output resistance 5/	R_{I-O}		25°C	01	10^{13} typical		Ω
Input to output capacitance 5/	C_{I-O}	f = 1 MHz	25°C	01	2.2 typical		pF
Input capacitance 6/	C_I		25°C	01	4.0 typical		pF
Integrated circuit junction to ambient thermal resistance	θ_{JA}	Thermocouple located at center of package underside	25°C	01	45 typical		°C/W

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, $V_{DD1} = V_{DD2}$ = 3 V to 20 V for T_A = -55°C to +125°C and all typical specifications are at T_A = +25°C.

3/ Output gain defined as the slope of the best fit line of the output voltage versus the input voltage over the specified input range, with the offset error adjusted out.

4/ Output linearity is defined as the peak to peak output deviation from the best fit line of the output gain, expressed as a percentage of the full scale output voltage.

5/ The device is considered a 2 terminal device; pin1 through 8 are shorted together, and pin 9 through pin 16 are shorted together.

6/ Input capacitance is from any input pin to ground.

Case X

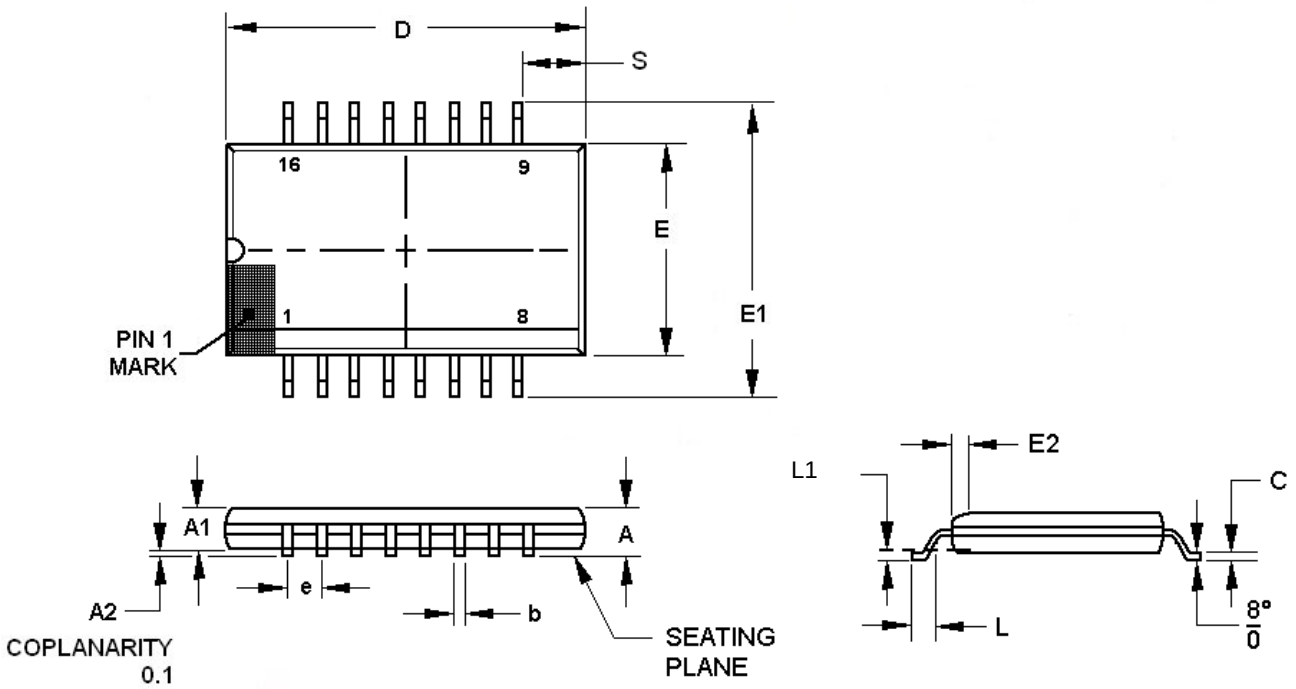

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/17602
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Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Medium	Maximum	Minimum	Medium	Maximum
A	.096	.099	.103	2.44	2.54	2.64
A1	.088	---	.096	2.24	---	2.44
A2	.003	.007	.011	0.10	0.20	0.30
b	.014	---	.018	0.36	---	0.46
c	.009	---	.012	0.23	---	0.32
D	.498	.501	.505	12.65	12.75	12.85
E	.291	.295	.299	7.40	7.50	7.60
E1	.398	.405	.413	10.11	10.31	10.51
E2	.012	.019	.027	0.31	0.50	0.71
e	.049 BSC			1.27 BSC		
L	.020	.029	.039	0.51	0.76	1.01
L1	.009 BSC			0.25 BSC		
S	.075 REF			1.93 REF		

NOTE:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{DD1}	Supply voltage for side 1 (3.0 V to 20 V). Connect a 1 μF capacitor between V_{DD1} and GND1.
2	GND1	Ground reference for side 1.
3	V_{REG1}	Internal supply voltage for side 1. Connect a 1 μF capacitor between V_{REG1} and GND1.
4	REF_{OUT1}	Reference output voltage for side 1. The maximum recommended capacitance for this pin ($C_{REFOUT1}$) is 15 pF.
5	NC	No connection. Connect pin 5 to GND1; do not leave this pin floating.
6	EA_{OUT2}	Isolated output voltage 2, open drain output. Connect a pull up resistor between EA_{OUT2} and V_{DD1} for current up to 1 mA.
7	EA_{OUT}	Isolated output voltage.
8	GND1	Ground reference for side 1.
9	GND2	Ground reference for side 2.
10	COMP	Output of the operational amplifier. A loop compensation network can be connected between the COMP pin and the –IN pin.
11	-IN	Inverting operational amplifier input. Pin 11 is the connection for the power supply setpoint and compensation network.
12	+IN	Noninverting operational amplifier input. Pin 12 can be used as a reference input.
13	REF_{OUT}	Reference output voltage for side 2. The maximum recommended capacitance for this pin (C_{REFOUT}) is 15 pF.
14	V_{REG2}	Internal supply voltage for side 2. Connect a 1 μF capacitor between V_{REG2} and GND2.
15	GND2	Ground reference for side 2.
16	V_{DD2}	Supply voltage for side 2 (3.0 V to 20 V). Connect a 1 μF capacitor between V_{DD2} and GND2.

NOTES.
1. NC = No connection
2. Connect pin 5 to GND1; do not leave this pin floating.

FIGURE 2. Terminal connections.

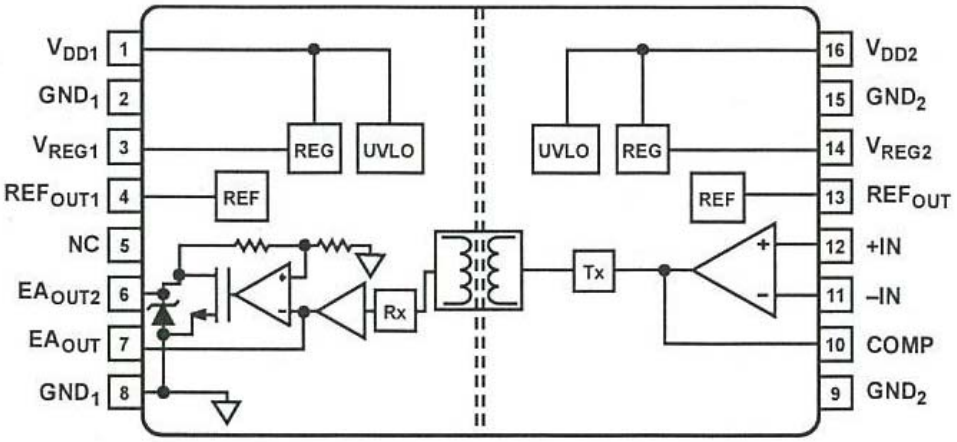

FIGURE 3. Logic diagram.

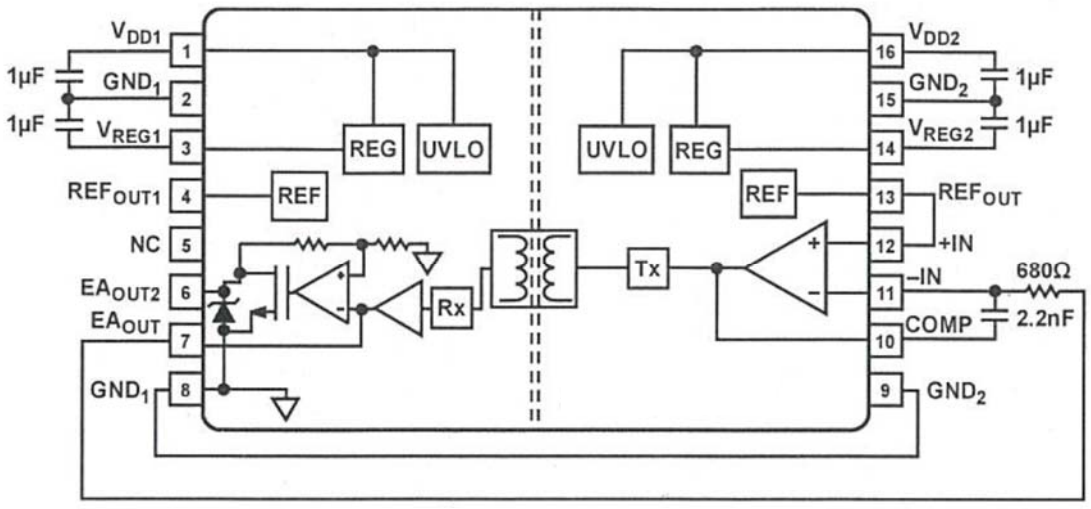

FIGURE 4. Accuracy circuit using EA_{OUT}.

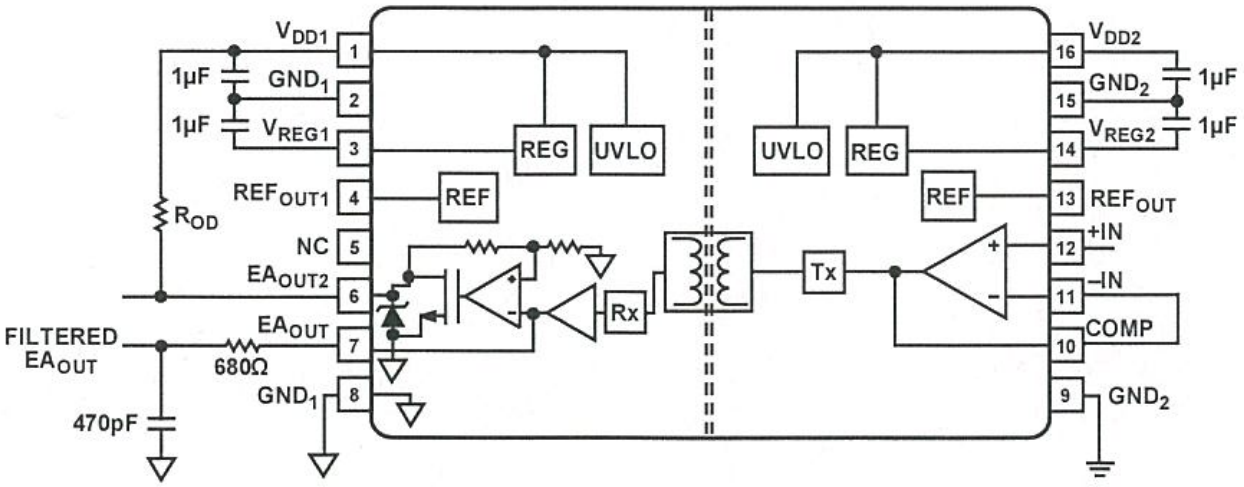

FIGURE 5. Isolated amplifier circuit.

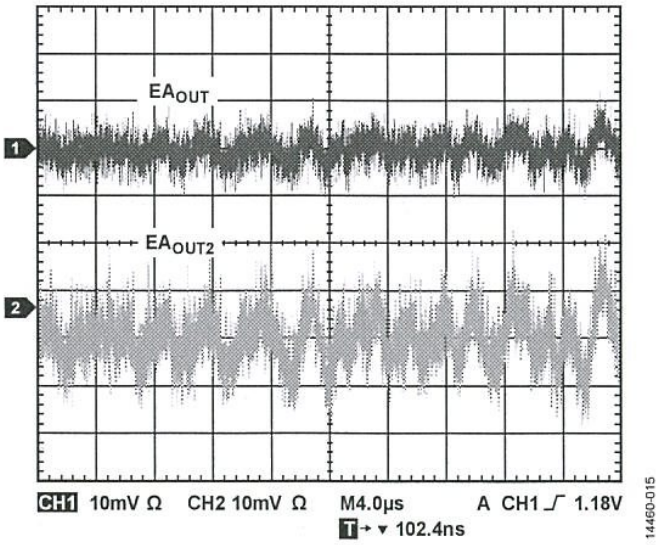

FIGURE 6. Output noise with test circuit 1 (10 mV/div), channel 1 = EAOUT, channel 2 = EAOUT.

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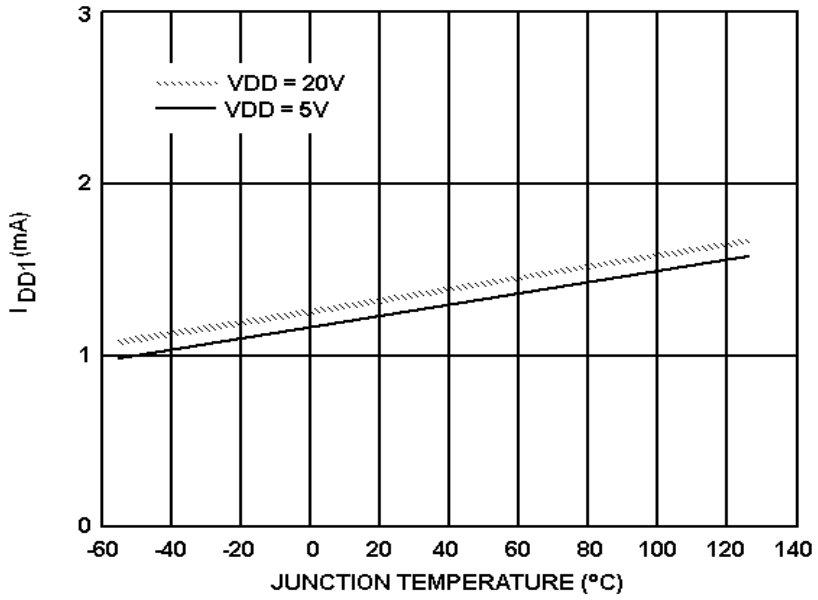

FIGURE 7. Typical I_{DD1} supply current versus junction temperature for V_{DD} = 20 V and V_{DD} = 5 V.

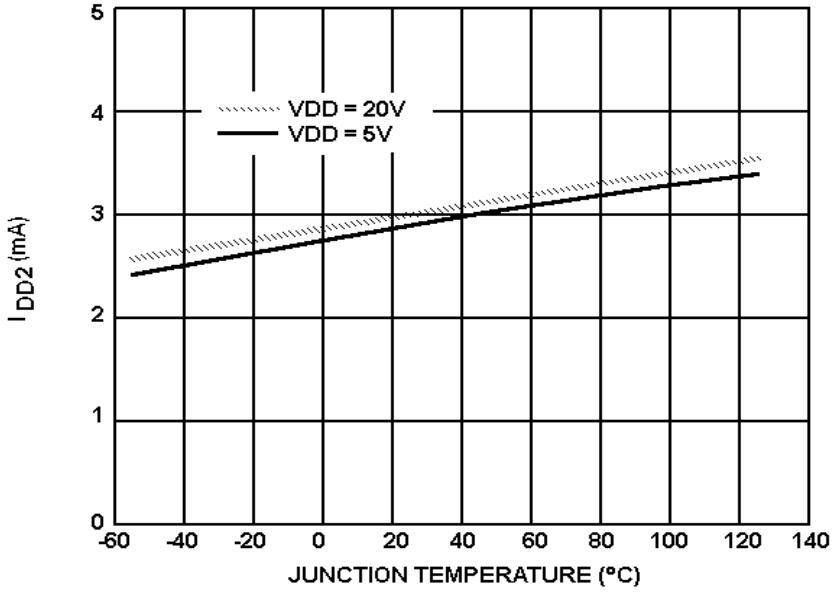

FIGURE 8. Typical I_{DD2} supply current versus junction temperature for V_{DD} = 20 V and V_{DD} = 5 V.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/17602-01XE	24355	Tube, 37 units	ADuM4190TRIZ-EP
V62/17602-01XE	24355	Reel, 1000 units	ADuM4190TRIZ-EP-RL

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland