REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 16-09-30	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, 16-BIT, ISOLATED SIGMA-DELTA MODULATOR, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/16625**
	REV	**PAGE** 1 **OF** 10

AMSC N/A

5962-V105-16

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16-Bit, Isolated Sigma-Delta Modulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16625	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7403–EP	16-Bit, Isolated Sigma-Delta Modulator

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-013-AC	Plastic, 16 Lead Standard Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD1} to GND_1	-0.3 V to +6.5 V
V_{DD2} to GND_2	-0.3 V to +6.5 V
Analog Input Voltage to GND_1	-1 V to V_{DD1} + 0.3 V
Digital Input Voltage to GND_2	-0.3 V to V_{DD2} + 0.5 V
Output Voltage to GND_2	-0.3 V to V_{DD2} + 0.3 V
Input Current to Any Pin Except Supplies	±10 mA 2/
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
Pb-Free Temperature, Soldering Reflow	260°C
ESD:	
FICDM	±1250 V 3/
HBM	±4000 V 4/

1.4 Maximum Continuous Working Voltage. 5/

AC Voltage:	
Maximum Bipolar waveform	1250 V_{PEAK} (20 year minimum lifetime (VDE approved working voltage))
Unipolar Waveform	1250 V_{PEAK} (20 year minimum lifetime)
DC Voltage	1250 V_{PEAK} (20 year minimum lifetime)

1.5 Package characteristics.

Resistance (Input to Output), R_{I-O}	10^{12} Ω TYP 6/
Capacitance (Input to Output) (f = 1 MHz)	2.2 pF TYP 6/
IC Junction to Ambient Thermal Resistance, θ_{JA}	45°C/W TYP 7/

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Transient currents of up to 100 mA do not cause SCR to latch up.
3/ JESD22-C101; RC network: 1 Ω, Cpkg; Class: IV.
4/ ESDA/JEDEC JS-001-2011; RC network: 1.5 kΩ, 100 pF; Class: 3A.
5/ Maximum continuous working voltage refers to continuous voltage magnitude imposed across the isolation barrier.
6/ The device is considered a 2-terminal device. For AD7403-EP, Pin 1 to Pin 8 are shorted together and Pin 9 to Pin 16 are shorted together.
7/ Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD22-C101	–	Field-Induced Charged-Device Model (FIDCM) Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
JEDEC JS-001	–	Joint JEDEC/ESDA standard for electrostatic discharge sensitivity test – Human Body Model (HBM)

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Data Timing. The Data Timing shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
STATIC PERFORMANCE						
Resolution		3/	16			Bits
Integral Nonlinearity 4/	INL			±2	±12	LSB
Differential Nonlinearity 4/	DNL	5/			±0.99	LSB
Offset Error 4/				±0.2	±0.9	mV
Offset Drift vs. Temperature 5/				1.6	3.8	µV/°C
		0°C to 85°C		1.3	3.1	µV/°C
Offset Drift vs V_{DD1}				50		µV/V
Gain Error				±0.2	±0.95	%FSR
Gain Error Drift vs. Temperature 5/				65	95	ppm/°C
				40	60	µV/°C
Gain Error Drift vs. V_{DD1} 5/				±0.6		mV/V
ANALOG INPUT						
Input Voltage Range		Full-scale range	-320		+320	mV
		For specified performance	-250		+250	mV
Input Common-Mode Voltage Range				−200 to +300		mV
Dynamic Input Current		V_{IN+} = ±250 mV, V_{IN-} = 0 V		±45	±50	µA
		V_{IN+} = 0 V, V_{IN-} = 0 V		0.05		µA
DC Leakage Current				±0.01	±0.6	µA
Input Capacitance				14		pF
DYNAMIC SPECIFICATIONS 4/ (V_{IN+} = 1 kHz)						
Signal-to-Noise-and-Distortion Ratio	SINAD		82	87		dB
Signal-to-Noise Ratio	SNR		86	88		dB
Total Harmonic Distortion	THD			-94		dB
Peak Harmonic or Spurious Noise	SFDR			-95		dB
Effective Number of Bits	ENOB		13.1	14.2		Bits
Noise Free Code Resolution			14			Bits
ISOLATION TRANSIENT IMMUNITY 4/			25	30		kV/µs
LOGIC INPUTS (CMOS with Schmitt trigger)						
Input Voltage High	V_{IH}		0.8 x V_{DD2}			V
Input Voltage Low	V_{IH}				0.2 x V_{DD2}	V
Input Current	I_{IN}				±0.6	µA
Input Capacitance	C_{IN}				10	pF
LOGIC OUTPUTS						
Output Voltage High	V_{OH}	I_O = −200 µA	V_{DD2} − 0.1			V
Output Voltage High	V_{OL}	I_O = 200 µA			0.4	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
POWER REQUIREMENTS						
V_{DD1}			4.5		5.5	V
V_{DD2}			4.5		5.5	V
I_{DD1}		V_{DD1} = 5.5 V		30	36	mA
I_{DD2}		V_{DD2} = 5.5 V		12	18	mA
Power Dissipation		V_{DD1} = V_{DD2} = 5.5 V		231	297	mW
TIMING SPECIFICATIONS (See Figure 5)						
Test	Symbol	Test conditions 6/	Limits			Unit
			Min	Typ	Max	
Master clock input frequency	f_{MCLKIN}		5		16	MHz
Data access time after MCLKIN rising edge 7/	t_1				45	ns
Data hold time after MCLKIN rising edge 7/	t_2		12			ns
Master clock low time	t_3		0.45 × t_{MCLKIN}			ns
Master clock high time	t_4		0.45 × t_{MCLKIN}			ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design. Refer to manufacturer data sheet.

2/ V_{DD1} = 4.5 V to 5.5 V, VIN+ = −250 mV to +250 mV, VIN− = 0 V, TA = −55°C to +125°C, f_{MCLKIN} = 5 MHz to 16 MHz, tested with sinc3 filter, 256 decimation rate, as defined by Verilog code, unless otherwise noted. All voltages are relative to their respective ground.

3/ Filter output truncated to 16 bits

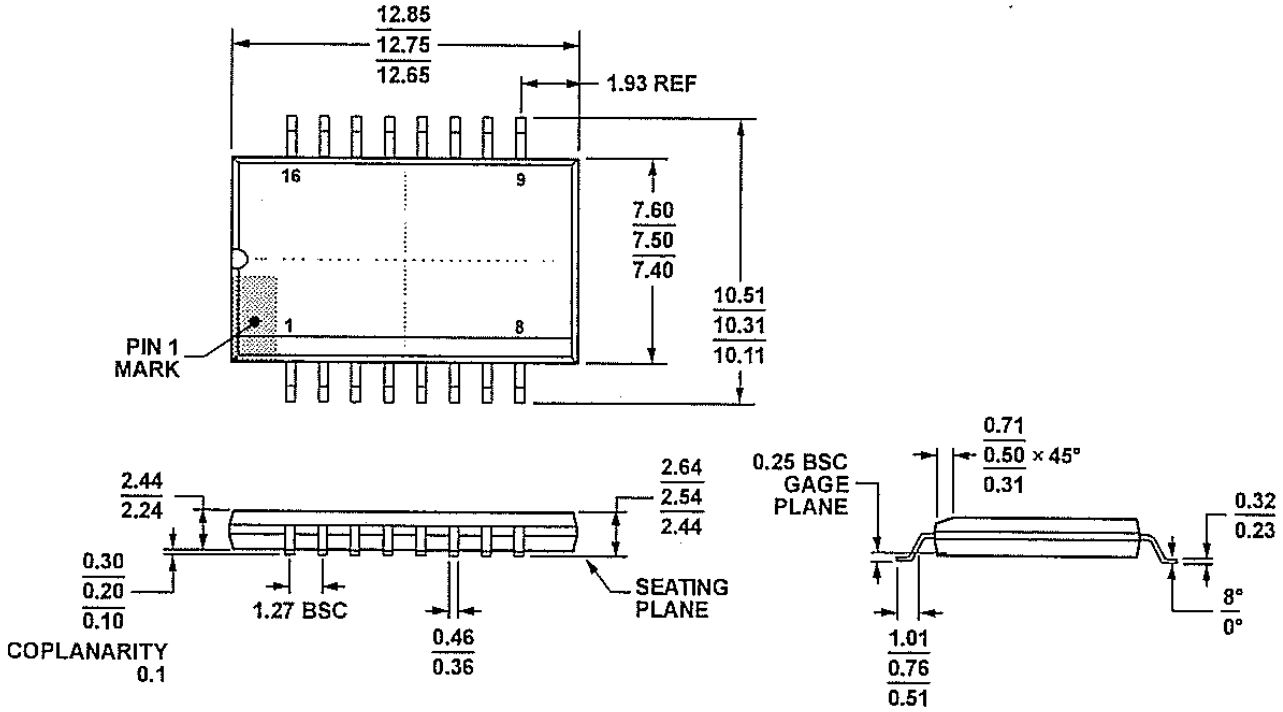
4/ See the Terminology section of the manufacturer AD7403 datasheet

5/ Not production tested. Sample tested during initial release to ensure compliance.

6/ V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 4.5 V to 5.5 V, T_A = −55°C to +125°C, unless otherwise noted. Sample tested during initial release to ensure compliance. It is recommended to read MDAT on the MCLKIN rising edge.

7/ Defined as the time required from an 80% MCLKIN input level to when the output crosses 0.8 V or 2.0 V for V_{DD2} = 3 V to 3.6 V or when the output crosses 0.8 V or 0.7 × V_{DD2} for V_{DD2} = 4.5 V to 5.5 V as outlined in Figure 2. Measured with a ±200 µA load and a 25 pF load capacitance

Case X



NOTES:

1. All linear dimensions are in millimeters.
2. Falls within JEDEC MS-013-AC.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{DD1}	16	GND_2
2	V_{IN+}	15	NIC 2/
3	V_{IN-}	14	V_{DD2}
4	GND_1	13	MCLKIN
5	NIC 1/	12	NIC 2/
6	NIC 1/	11	MDAT
7	V_{DD1}	10	NIC 2/
8	GND_1	9	GND_2

1/ Not Internally Connected. Connect to V_{DD1}, GND_1, or Leave Floating.
2/ Not Internally Connected. Connect to V_{DD2}, GND_2, or Leave Floating.

FIGURE 2. Terminal connections.

Terminal number	Terminal symbol	Description
1, 7	V_{DD1}	Supply Voltage, 4.5 V to 5.5 V. This is the supply voltage for the isolated side of the AD7403-EP and is relative to GND_1. For device operation, connect the supply voltage to both Pin 1 and Pin 7. Decouple each supply pin to GND_1 with a 10 µF capacitor in parallel with a 1 nF capacitor.
2	V_{IN+}	Positive Analog Input.
3	V_{IN-}	Negative Analog Input. Normally connected to GND_1.
4, 8	GND_1	Ground 1. This pin is the ground reference point for all circuitry on the isolated side.
5, 6	NIC	Not Internally Connected. These pins are not internally connected. Connect to V_{DD1}, GND_1, or leave floating.
9, 16	GND_2	Ground 2. This pin is the ground reference point for all circuitry on the nonisolated side.
10, 12, 15	NIC	Not Internally Connected. These pins are not internally connected. Connect to V_{DD2}, GND_2, or leave floating.
11	MDAT	Serial Data Output. The single bit modulator output is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the MCLKIN input and are valid on the following MCLKIN rising edge.
13	MCLKIN	Master Clock Logic Input. 5 MHz to 20 MHz frequency range. The bit stream from the modulator is propagated on the rising edge of the MCLKIN.
14	V_{DD2}	Supply Voltage, 3 V to 5.5 V. This is the supply voltage for the nonisolated side and is relative to GND_2. Decouple this supply to GND_2 with a 100 nF capacitor.

FIGURE 3. Terminal function.

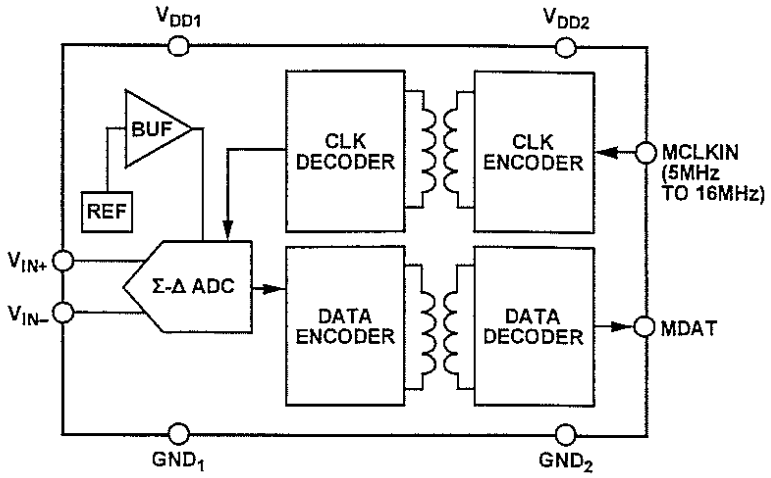


FIGURE 4. Functional block diagram.

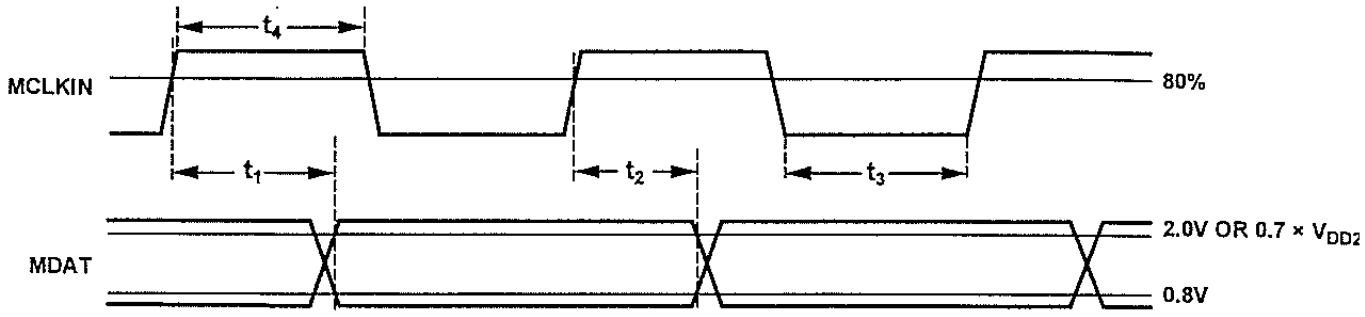


FIGURE 5. Data Timing.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 3 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Ordering Quantity	Vendor part number
V62/16625-01XE	24355	Tube 37 units	AD7403TRIZ-EP
		Reel 400 units	AD7403TRIZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106