REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Make corrections to both conditions columns under Logic low output voltages tests as specified in Table I. Make correction to dimension “b” and add dimension “e” as specified under Figure 1. Update document paragraphs to current requirements. - ro	21-10-06	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	A																				
PAGE	18																				

REV STATUS OF PAGES																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A

PREPARED BY
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DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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Original date of drawing
YY-MM-DD

16-09-07

CHECKED BY
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APPROVED BY
CHARLES F. SAFFLE

TITLE

MICROCIRCUIT, LINEAR, ISOLATED, 4 AMP, DUAL CHANNEL GATE DRIVER, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**	**DWG NO.**
A	**16236**	**V62/16622**

REV **A**

PAGE 1 **OF** 18

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V075-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance isolated, 4 amp dual channel gate driver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16622	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADuM3221	Isolated, 4 amp dual channel gate driver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage ranges (V_{DD}): 2/

V_{DD1} ..... -0.5 V to +7.0 V

V_{DD2} ..... -0.5 V to +20 V

Input voltage range (V_{IA}, V_{IB}) ..... -0.5 V to V_{DDI} + 0.5 V 2/ 3/

Output voltage range (V_{OA}, V_{OB}) ..... -0.5 V to V_{DDO} + 0.5 V 2/ 3/

Average output current per pin (I_O) ..... -23 mA to +23 mA 4/

Common mode transients (CM_H, CM_L) ..... -100 kV/μs to +100 kV/μs 5/

Storage temperature range ..... -55°C to +150°C

1.4 Recommended operating conditions. 6/

Operating junction temperature range (T_J) ..... -55°C to +125°C

Supply voltage ranges (V_{DD}): 2/

V_{DD1} ..... +3.0 V to +5.5 V

V_{DD2} ..... +7.6 V to +18 V

V_{DD1} rise time (tV_{DD1}) ..... 1 V/μs maximum

Common mode transient immunity, input to output ..... -25 kV/μs minimum, +25 kV/μs maximum

Input signal rise and fall times ..... 1 ms maximum

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltages are relative to their respective ground.

3/ V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.

4/ See figure 4 for information about maximum allowable current for various temperatures.

5/ Refers to common mode transients across the insulation barrier. Common mode transients exceeding the absolute maximum rating can cause latch up or permanent damage.

6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

1.5 Maximum continuous working voltage. 7/

Parameter	Maximum	Unit	Constraint
AC bipolar voltage	565	V peak	50 year minimum lifetime
AC unipolar voltage	1131	V peak	50 year minimum lifetime
DC voltage	1131	V peak	50 year minimum lifetime

1.6 Package characteristics.

Parameter	Symbol	Conditions	Limits	Unit
Resistance (input to output) 8/	R_{I-O}		10^{12} typical	Ω
Capacitance (input to output) 8/	C_{I-O}	f = 1 MHz	1.0 typical	pF
Input capacitance	C_I		4.0 typical	pF
Integrated circuit junction to case thermal resistance, side 1	θ_{JCI}	Thermocouple located at center of package underside.	46 typical	°C/W
Integrated circuit junction to case thermal resistance, side 2	θ_{JCO}	Thermocouple located at center of package underside.	41 typical	°C/W
Integrated circuit junction to ambient thermal resistance	θ_{JA}	Thermocouple located at center of package underside.	85 typical	°C/W

_____

7/ Refers to the continuous voltage magnitude imposed across the isolation barrier.

8/ The device is considered a 2 terminal device; pin 1 through pin 4 are shorted together, and pin 5 through pin 8 are shorted together.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Thermal derating curve. The thermal derating curve shall be as shown in figure 4.

3.5.5 Supply current for isolator side 1 versus frequency graph. The supply current for isolator side 1 versus frequency graph shall be as shown in figure 5.

3.5.6 Supply current for isolator side 2 versus frequency with 2 nF load graph. The supply current for isolator side 2 versus frequency with 2 nF load graph shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 5 V operation	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
DC specifications.							
Input supply current, two channels, quiescent	$I_{DDI(Q)}$		25°C	01	1.2 typical		mA
			-55°C to +125°C			1.5	
Output supply current, two channels, quiescent	$I_{DDO(Q)}$		25°C	01	4.7 typical		mA
			-55°C to +125°C			10	
Total supply current, 3/ two channels, V_{DD1} supply current	$I_{DD1(Q)}$	DC to 1 MHz logic signal frequency	25°C	01	1.4 typical		mA
			-55°C to +125°C			1.7	
Total supply current, 3/ two channels, V_{DD2} supply current	$I_{DD2(Q)}$	DC to 1 MHz logic signal frequency	25°C	01	1.1 typical		mA
			-55°C to +125°C			17	
Input currents	I_{IA}, I_{IB}	0 V ≤ V_{IA}, V_{IB} ≤ V_{DD1}	25°C	01	+0.01 typical		µA
			-55°C to +125°C		-10	+10	
Logic high input threshold	V_{IH}		-55°C to +125°C	01	0.7 x V_{DD1}		V
Logic low input threshold	V_{IL}		-55°C to +125°C	01		0.3 x V_{DD1}	V
Logic high output voltages	V_{OAH}, V_{OBH}	I_{OX} = -20 mA, 4/ V_{IX} = V_{IXH} 5/	25°C	01	V_{DD2} typical		V
			-55°C to +125°C		V_{DD2} – 0.1		
Logic low output voltages	V_{OAL}, V_{OBL}	I_{OX} = +20 mA, 4/ V_{IX} = V_{IXL} 6/	25°C	01	0 typical		V
			-55°C to +125°C			0.15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 5 V operation – continued.	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
DC specifications - continued.							
Undervoltage lockout V_{DD2} supply.							
Positive going threshold	V_{DD2UV+}		25°C	01	7.0 typical		V
			-55°C to +125°C			7.5	
Negative going threshold	V_{DD2UV-}		25°C	01	6.5 typical		V
			-55°C to +125°C		6.0		
Hysteresis	V_{DD2UVH}		25°C	01	0.5 typical		V
Output short circuit 7/ pulsed current	$I_{OA(SC)}$, $I_{OB(SC)}$	V_{DD2} = 10 V	25°C	01	4.0 typical		A
			-55°C to +125°C		2.0		
Output pulsed source resistance	R_{OA}, R_{OB}	V_{DD2} = 10 V	25°C	01	1.3 typical		Ω
			-55°C to +125°C		0.3	3.0	
Output pulsed sink resistance	R_{OA}, R_{OB}	V_{DD2} = 10 V	25°C	01	0.9 typical		Ω
			-55°C to +125°C		0.3	3.0	
Switching specifications.							
Pulse width 8/	PW	C_L = 2 nF, V_{DD2} = 10 V	-55°C to +125°C	01	50		ns
Data rate 9/		C_L = 2 nF, V_{DD2} = 10 V	-55°C to +125°C	01		1	MHz
Propagation delay 10/	t_{DLH}, t_{DHL}	C_L = 2 nF, V_{DD2} = 10 V	25°C	01	45 typical		ns
			-55°C to +125°C		35	60	
		C_L = 2 nF, V_{DD2} = 7.6 V	25°C		50 typical		
			-55°C to +125°C		36	68	
Propagation delay 11/ skew	t_{PSK}	C_L = 2 nF, V_{DD2} = 10 V	-55°C to +125°C	01		12	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 5 V operation – continued.	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Switching specifications - continued.							
Channel to channel matching 12/	t_{PSKCD}	C_L = 2 nF, V_{DD2} = 10 V	25°C	01	1 typical		ns
			-55°C to +125°C			5	
		C_L = 2 nF, V_{DD2} = 7.6 V	25°C		1 typical		
			-55°C to +125°C			7	
Output rise/fall time (10% to 90%)	t_R / t_F	C_L = 2 nF, V_{DD2} = 10 V	25°C	01	20 typical		ns
			-55°C to +125°C		14	25	
Dynamic input supply current per channel	$I_{DDI(D)}$	V_{DD2} = 10 V	25°C	01	0.05 typical		mA/Mbps
Dynamic output supply current per channel	$I_{DDO(D)}$	V_{DD2} = 10 V	25°C	01	1.5 typical		mA/Mbps
Refresh rate	f_r		25°C	01	1.2 typical		Mbps

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 13/ 3.3 V operation	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
DC specifications.							
Input supply current, two channels, quiescent	$I_{DDI(Q)}$		25°C	01	0.7 typical		mA
			-55°C to +125°C			1.0	
Output supply current, two channels, quiescent	$I_{DDO(Q)}$		25°C	01	4.7 typical		mA
			-55°C to +125°C			10	
Total supply current, 3/ two channels, V_{DD1} supply current	$I_{DD1(Q)}$	DC to 1 MHz logic signal frequency	25°C	01	0.8 typical		mA
			-55°C to +125°C			1.0	
Total supply current, 3/ two channels, V_{DD2} supply current	$I_{DD2(Q)}$	DC to 1 MHz logic signal frequency	25°C	01	11 typical		mA
			-55°C to +125°C			17	
Input currents	I_{IA}, I_{IB}	0 V ≤ V_{IA}, V_{IB} ≤ V_{DD1}	25°C	01	+0.01 typical		µA
			-55°C to +125°C		-10	+10	
Logic high input threshold	V_{IH}		-55°C to +125°C	01	0.7 x V_{DD1}		V
Logic low input threshold	V_{IL}		-55°C to +125°C	01		0.3 x V_{DD1}	V
Logic high output voltages	V_{OAH}, V_{OBH}	I_{OX} = -20 mA, 4/ V_{IX} = V_{IXH} 5/	25°C	01	V_{DD2} typical		V
			-55°C to +125°C		V_{DD2} – 0.1		
Logic low output voltages	V_{OAL}, V_{OBL}	I_{OX} = +20 mA, 4/ V_{IX} = V_{IXL} 6/	25°C	01	0 typical		V
			-55°C to +125°C			0.15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 13/ 3.3 V operation – continued.	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
DC specifications - continued.							
Undervoltage lockout V_{DD2} supply.							
Positive going threshold	V_{DD2UV+}		25°C	01	7.0 typical		V
			-55°C to +125°C			7.5	
Negative going threshold	V_{DD2UV-}		25°C	01	6.5 typical		V
			-55°C to +125°C		6.0		
Hysteresis	V_{DD2UVH}		25°C	01	0.5 typical		V
Output short circuit 7/ pulsed current	$I_{OA(SC)}$, $I_{OB(SC)}$	V_{DD2} = 10 V	25°C	01	4.0 typical		A
			-55°C to +125°C		2.0		
Output pulsed source resistance	R_{OA}, R_{OB}	V_{DD2} = 10 V	25°C	01	1.3 typical		Ω
			-55°C to +125°C		0.3	3.0	
Output pulsed sink resistance	R_{OA}, R_{OB}	V_{DD2} = 10 V	25°C	01	0.9 typical		Ω
			-55°C to +125°C		0.3	3.0	
Switching specifications.							
Pulse width 8/	PW	C_L = 2 nF, V_{DD2} = 10 V	-55°C to +125°C	01	50		ns
Data rate 9/		C_L = 2 nF, V_{DD2} = 10 V	-55°C to +125°C	01		1	MHz
Propagation delay 10/	t_{DLH}, t_{DHL}	C_L = 2 nF, V_{DD2} = 10 V	25°C	01	48 typical		ns
			-55°C to +125°C		36	62	
		C_L = 2 nF, V_{DD2} = 7.6 V	25°C		53 typical		
			-55°C to +125°C		37	72	
Propagation delay 11/ skew	t_{PSK}	C_L = 2 nF, V_{DD2} = 10 V	-55°C to +125°C	01		12	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 13/ 3.3 V operation – continued.	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Switching specifications - continued.							
Channel to channel matching 12/	t_{PSKCD}	C_L = 2 nF, V_{DD2} = 10 V	25°C	01	1 typical		ns
			-55°C to +125°C			5	
Output rise/fall time (10% to 90%)	t_R / t_F	C_L = 2 nF, V_{DD2} = 10 V	25°C	01	20 typical		ns
			-55°C to +125°C		14	25	
		C_L = 2 nF, V_{DD2} = 7.6 V	25°C		22 typical		
			-55°C to +125°C		14	28	
Dynamic input supply current per channel	$I_{DDI(D)}$	V_{DD2} = 10 V	25°C	01	0.025 typical		mA/Mbps
Dynamic output supply current per channel	$I_{DDO(D)}$	V_{DD2} = 10 V	25°C	01	1.5 typical		mA/Mbps
Refresh rate	f_r		25°C	01	1.1 typical		Mbps

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ 5 V operation. All voltages are relative to their respective ground. Unless otherwise specified, 4.5 V ≤ V_{DD1} ≤ 5.5 V and 7.6 V ≤ V_{DD2} ≤ 18 V. All minimum/maximum specifications apply over T_J = -55°C to +125°C. All typical specifications are at T_J = 25°C, V_{DD1} = 5 V and V_{DD2} = 10 V. Switching specifications are tested with CMOS signal levels.

3/ The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. See figure 5 and figure 6 for total V_{DD1} and V_{DD2} supply currents as function of frequency.

4/ I_{OX} is the channel x output current, where x = A or B.

5/ V_{IxH} is the input side logic high.

6/ V_{IxL} is the input side logic low.

7/ Short circuit duration less than 1 μs. Average power must conform to the limit shown in the absolute maximum ratings section.

8/ The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.

9/ The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.

10/ t_{DLH} propagation delay is measured from the time of the input rising logic high threshold (V_{IH}), to the output rising 10% threshold of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold (V_{IL}), to the output falling 90% threshold of the V_{Ox} signal.

11/ t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

12/ Channel to channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

13/ 3.3 V operation. All voltages are relative to their respective ground. Unless otherwise specified, 3.0 V ≤ V_{DD1} ≤ 3.6 V and 7.6 V ≤ V_{DD2} ≤ 18 V. All minimum/maximum specifications apply over T_J = -55°C to +125°C. All typical specifications are at T_J = 25°C, V_{DD1} = 3.3 V and V_{DD2} = 10 V. Switching specifications are tested with CMOS signal levels.

Case X

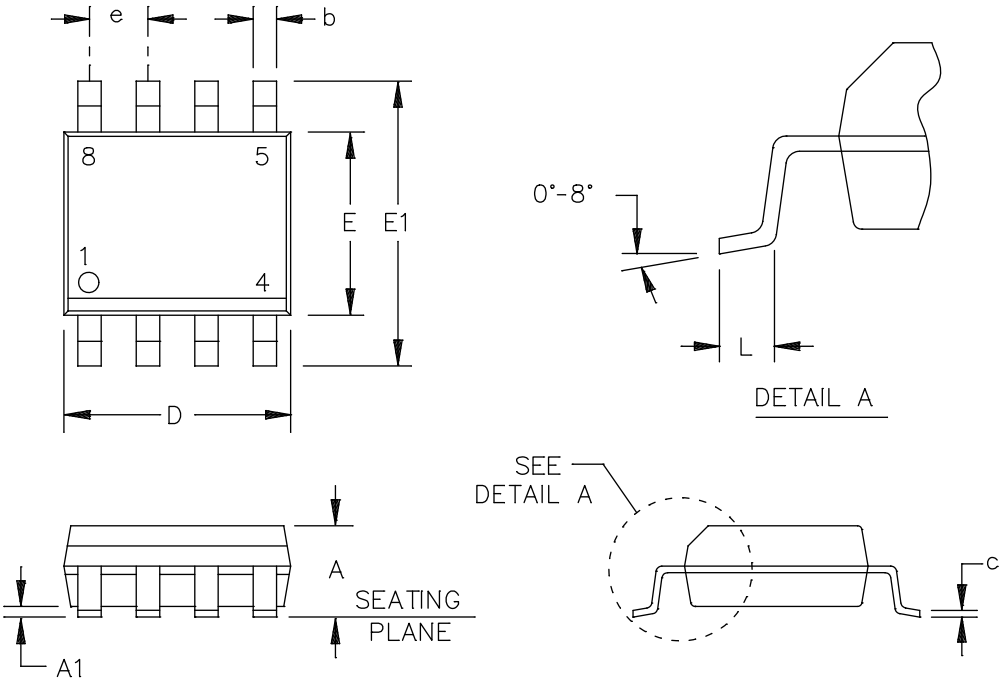

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/16622
		REV A	PAGE 13

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.0532	.0688	1.35	1.75
A1	.0039	.0098	0.10	0.25
b	.0122	.0201	0.31	0.51
c	.0067	.0098	0.17	0.25
D	.1890	.1968	4.80	5.00
e	.0500 BSC		1.27 BSC	
E	.1497	.1574	3.80	4.00
E1	.2284	.2441	5.80	6.20
L	.0157	.05000	0.40	1.27

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{DD1}	Supply voltage for isolator side 1, 3.0 V to 5.5 V.
2	V_{IA}	Logic input A.
3	V_{IB}	Logic input B.
4	GND 1	Ground 1. GND 1 is the ground reference for isolator side 1.
5	GND 2	Ground 2. GND 2 is the ground reference for isolator side 2.
6	V_{OB}	Logic output B.
7	V_{OA}	Logic output A.
8	V_{DD2}	Supply voltage for isolator side 2, 7.6 V to 18 V.

FIGURE 2. Terminal connections.

Positive logic

V_{IA} input	V_{IB} input	V_{DD1} state	V_{DD2} state	V_{OA} output	V_{OB} output	Notes
Low	Low	Powered	Powered	Low	Low	
Low	High	Powered	Powered	Low	High	
High	Low	Powered	Powered	High	Low	
High	High	Powered	Powered	High	High	
Don't care	Don't care	Unpowered	Powered	Low	Low	Outputs return to the input state within 1 μs of V_{DD1} power restoration.
Don't care	Don't care	Powered	Unpowered	Low	Low	Outputs return to the input state within 1 μs of V_{DD2} power restoration.

FIGURE 3. Truth table.

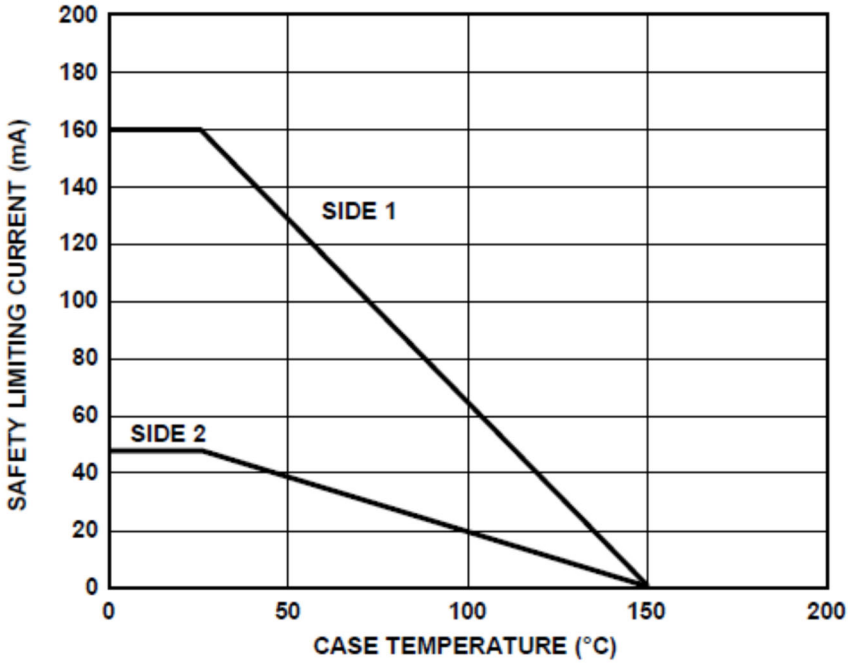

FIGURE 4. Thermal derating curve.

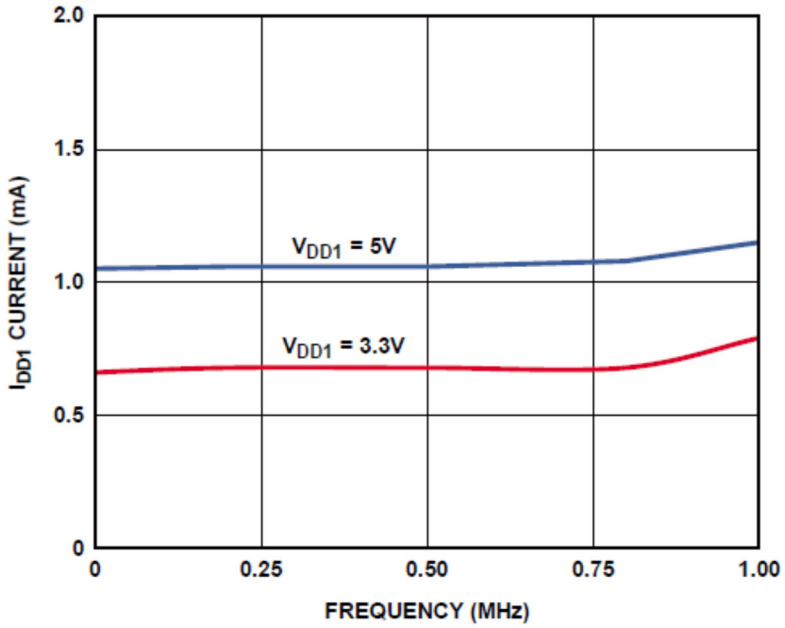

FIGURE 5. Supply current for isolator side 1 versus frequency.

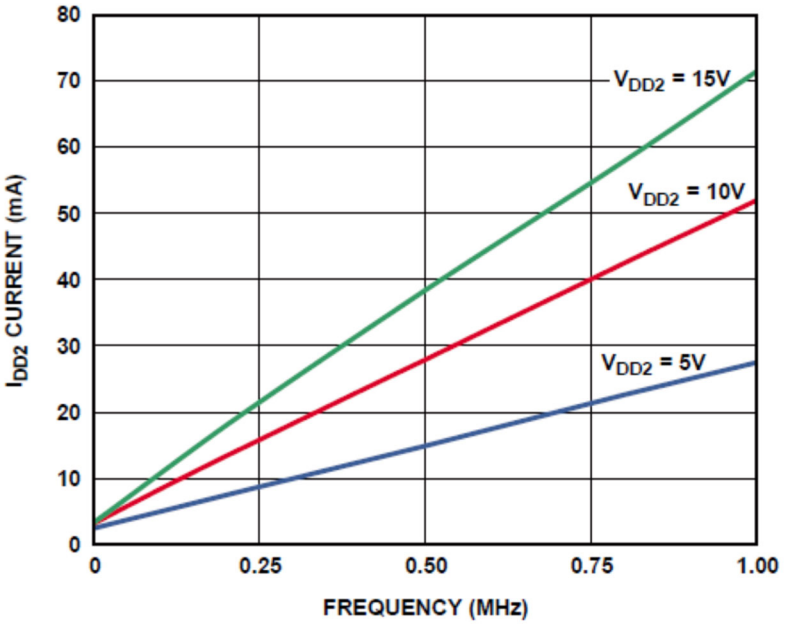

FIGURE 6. Supply current for isolator side 2 versus frequency with 2 nF load.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/16622-01XE	24355	Tube, 98 units	ADuM3221TRZ-EP
V62/16622-01XE	24355	Reel, 1000 units	ADuM3221TRZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123