REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14						

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 16-08-25	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, LINEAR, 1 pC CHARGE INJECTION, 100 pA LEAKAGE, CMOS, ±5 V/5 V/3 V, QUAD SPST SWITCHES, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/16617**
	REV	**PAGE** 1 **OF** 14

AMSC N/A

5962-V104-16

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 1 pC Charge Injection, 100 Pa Leakage, CMOS, ±5 V/5 V/3, Quad SPST Switches microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16617	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG613–EP	1 pC Charge Injection, 100 Pa Leakage, CMOS ±5 V/5 V/3, Quad SPST Switches

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153-AB	16-Lead Thin Shrink Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to V_{SS}	13 V 2/
V_{DD} to GND	-0.3 V to +6.5 V 2/
V_{SS} to GND	+0.3 V to -6.5 V 2/
Analog Inputs	V_{SS} -0.3 V to V_{DD} + 0.3 V 3/
Digital Inputs	GND – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first 3/
Peak Current, Sx or Dx	20 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx	10 mA
3 V Operation, 85°C to 125°C	7.5 mA
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
θ_{JA} Thermal Impedance – Case outline X	150.4°C/W
Lead Soldering:	
Lead temperature. Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	220°C
Pb-Free Soldering:	
Reflow, Peak Temperature	260 (+0/-5)°C
Time at Peak Temperature	20 sec to 40 sec

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Tested at −55°C to +125°C.
3/ Over voltages at INx, Sx, or Dx are clamped by internal diodes. Limit the current to the maximum ratings given. Tested at −55°C to +125°C.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 On Resistance. The on resistance shall be as shown in figure 6.

3.5.7 Off leakage. The off leakage shall be as shown in figure 7.

3.5.8 On leakage. The on leakage shall be as shown in figure 8.

3.5.9 Switching times. The switching times shall be as shown in figure 9.

3.5.10 Break Before Make Time Delay. The Break Before Make Time Delay shall be as shown in figure 10.

3.5.11 Charge Injection. The charge Injection shall be as shown in figure 11.

3.5.12 Off Isolation. The Off isolation shall be as shown in figure 12.

3.5.13 Channel-to-Channel Crosstalk. The Channel-to-Channel Crosstalk shall be as shown in figure 13.

3.5.14 Bandwidth. The bandwidth shall be as shown in figure 14.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/ V_{DD} = 5 V ±10% V_{SS} = 5 V ±10%	Limits						Unit
			25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
ANALOG SWITCH									
Analog Signal Range						V_{SS}		V_{DD}	V
On Resistance,	R_{ON}	V_S = ±3 V, I_S = −1 mA; see Figure 6		85	115			160	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_S = ±3 V, I_S = −1 mA		2	4			6.5	Ω
On-Resistance Flatness	$R_{RFLAT(ON)}$			25	40			60	Ω
LEAKAGE CURRENTS (V_{DD} = +5.5 V, V_{SS} = −5.5 V)									
Source Off Leakage	$I_{S(OFF)}$	V_D = ±4.5 V, V_S = ∓4.5 V, see Figure 7		±0.01	±0.1			±2	nA
Drain Off Leakage,	$I_{D(OFF)}$	V_D = ±4.5 V, V_S = ∓4.5 V, see Figure 7		±0.01	±0.1			±2	nA
Channel On Leakage	$I_{D(ON)}$, $I_{S(ON)}$	V_D = V_S = ±4.5 V; see Figure 8		±0.01	±0.1			±6	nA
DIGITAL INPUTS									
Input High Voltage	V_{INH}					2.4			V
Input Low Voltage	V_{INL}							0.8	V
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{INL} or V_{INH}		0.005				±0.1	µA
Digital Input Capacitance	C_{IN}			2					pF
DYNAMIC CHARACTERISTICS 3/									
Delay from Digital Control Input and Output Switching On	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_S = 3.0 V; see Figure 9		45	65			90	ns
Delay from Digital Control Input and Output Switching Off,	t_{OFF}	R_L = 300 Ω, C_L = 35 pF, V_S = 3.0 V; see Figure 9		25	40			50	ns
Break-Before-Make Time Delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 3.0 V; see Figure 10		15		10			ns
Charge Injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 11		-0.5					pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; see Figure 12		-65					dB
Channel to Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; see Figure 13		-90					dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF; see Figure 14		680					MHz
Off Switch Source Capacitance	$C_{S(OFF)}$	f = 1 MHz		5					pF
Off Switch Drain Capacitance	$C_{D(OFF)}$	f = 1 MHz		5					pF
On Switch Capacitance	$C_{D(ON)}$,$C_{S(ON)}$	f = 1 MHz		5					pF
POWER REQUIREMENTS (V_{DD} = +5.5 V, V_{SS} = -5.5 V)									
Positive Supply Current	I_{DD}	Digital inputs = 0 V or 5.5 V		0.001				1.0	µA
Negative Supply Current	I_{SS}	Digital inputs = 0 V or 5.5 V		0.001				1.0	µA
V_{DD}/V_{SS}						±2.7		±5.5	V
Power Consumption				11					nW
					11				µW

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/ V_{DD} = 5 V ±10% V_{SS} = 0 V	Limits						Unit
			25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
ANALOG SWITCH									
Analog Signal Range						0		V_{DD}	V
On Resistance,	R_{ON}	V_S = 3.5 V, I_S = −1 mA; see Figure 6		210	290			380	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_S = 3.5 V, I_S = −1 mA		3	10			13	Ω
LEAKAGE CURRENTS (V_{DD} = 5.5 V)									
Source Off Leakage	$I_{S(OFF)}$	V_S = 1 V or 4.5 V, V_D = 4.5 V or 1 V; see Figure 7		±0.01	±0.1			±2	nA
Drain Off Leakage,	$I_{D(OFF)}$	V_S = 1 V or 4.5 V, V_D = 4.5 V or 1 V; see Figure 7		±0.01	±0.1			±2	nA
Channel On Leakage	$I_{D(ON)}$, $I_{S(ON)}$	V_S = V_D = 1 V or 4.5 V; see Figure 8		±0.01	±0.1			±6	nA
DIGITAL INPUTS									
Input High Voltage	V_{INH}					2.4			V
Input Low Voltage	V_{INL}							0.8	V
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{INL} or V_{INH}		0.005				±0.1	µA
Digital Input Capacitance	C_{IN}			2					pF
DYNAMIC CHARACTERISTICS 3/									
	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_S = 3.0 V; see Figure 9		70	100			150	ns
	t_{OFF}	R_L = 300 Ω, C_L = 35 pF, V_S = 3.0 V; see Figure 9		25	40			50	ns
Break-Before-Make Time Delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 3.0 V; see Figure 10		25		10			ns
Charge Injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 11		1					pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; see Figure 12		-62					dB
Channel to Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; see Figure 13		-90					dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF; see Figure 14		680					MHz
Off Switch Source Capacitance	$C_{S(OFF)}$	f = 1 MHz		5					pF
Off Switch Drain Capacitance	$C_{D(OFF)}$	f = 1 MHz		5					pF
On Switch Capacitance	$C_{D(ON)}$,$C_{S(ON)}$	f = 1 MHz		5					pF
POWER REQUIREMENTS (V_{DD} = 5.5 V)									
	I_{DD}	Digital inputs = 0 V or 5.5 V		0.001				1.0	µA
	V_{DD}	Digital inputs = 0 V or 5.5 V				2.7		5.5	V
Power Consumption				5.5					nW
					5.5				µW

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

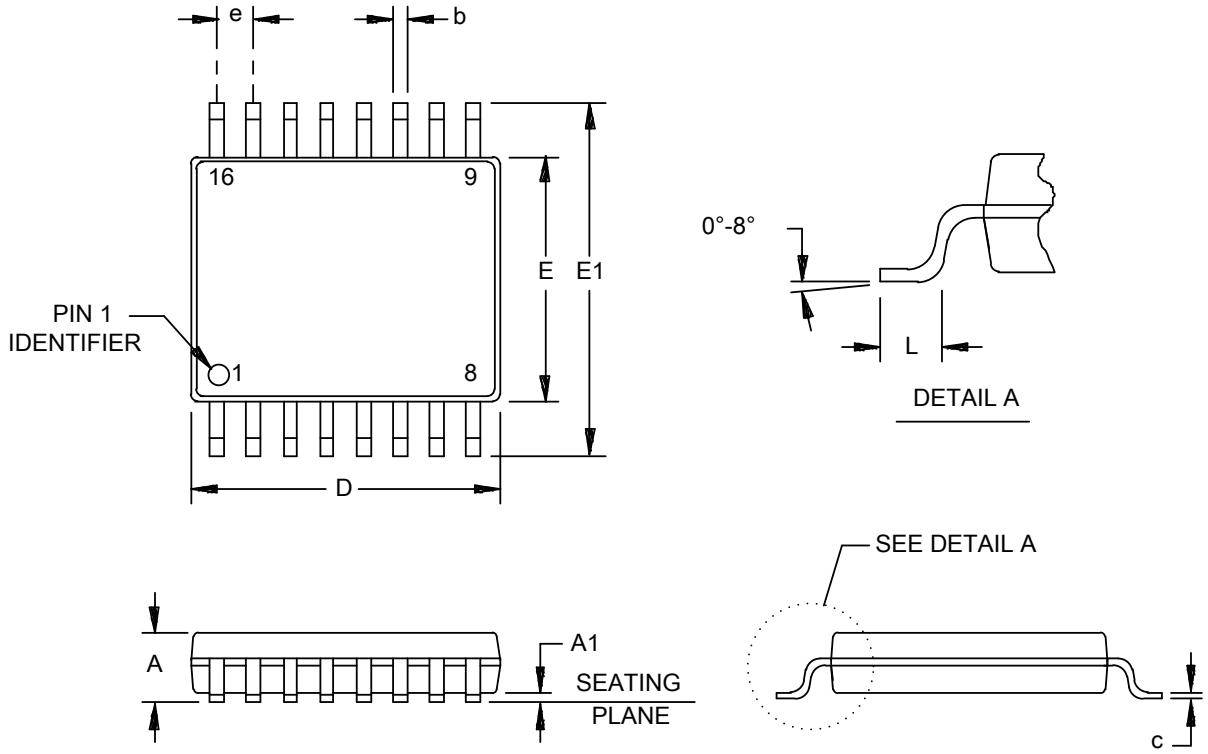
Test	Symbol	Test conditions 2/ V_{DD} = 3 V ±10% V_{SS} = 0 V	Limits						Unit
			25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
ANALOG SWITCH									
Analog Signal Range						0		V_{DD}	V
On Resistance,	R_{ON}	V_S = 1.5 V, I_S = −1 mA; see Figure 6		380			460		Ω
LEAKAGE CURRENTS (V_{DD} = 3.3 V)									
Source Off Leakage	$I_{S(OFF)}$	V_S = 1 V or 3 V, V_D = 3 V or 1 V; see Figure 7		±0.01	±0.1			±2	nA
Drain Off Leakage,	$I_{D(OFF)}$	V_S = 1 V or 3 V, V_D = 3 V or 1 V; see Figure 7		±0.01	±0.1			±2	nA
Channel On Leakage	$I_{D(ON)}$, $I_{S(ON)}$	V_S = V_D = 1 V or 4.5 V; see Figure 8		±0.01	±0.1			±6	nA
DIGITAL INPUTS									
Input High Voltage	V_{INH}					2.0			V
Input Low Voltage	V_{INL}							0.8	V
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{INL} or V_{INH}		0.005				±0.1	µA
Digital Input Capacitance	C_{IN}			2					pF
DYNAMIC CHARACTERISTICS 3/									
	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_S = 2 V; see Figure 9		130	185			260	ns
	t_{OFF}	R_L = 300 Ω, C_L = 35 pF, V_S = 2 V; see Figure 9		40	55			65	ns
Break-Before-Make Time Delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 2 V; see Figure 10		50		10			ns
Charge Injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 11		1.5					pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; see Figure 12		-62					dB
Channel to Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; see Figure 13		-90					dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF; see Figure 14		680					MHz
	$C_{S(OFF)}$	f = 1 MHz		5					pF
	$C_{D(OFF)}$	f = 1 MHz		5					pF
	$C_{D(ON)}$,$C_{S(ON)}$	f = 1 MHz		5					pF
POWER REQUIREMENTS (V_{DD} = 3.3 V)									
	I_{DD}	Digital inputs = 0 V or 3.3 V		0.001				1.0	µA
	V_{DD}	Digital inputs = 0 V or 3.3 V				2.7		5.5	V
Power Consumption				3.3					nW
					3.3				µW

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ GND = 0 V, unless otherwise noted. V_S is the source voltage. V_D is the drain voltage.

3/ Guaranteed by design; not subject to production test.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 BSC	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-153-AB.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	IN1	16	IN2
2	D1	15	D2
3	S1	14	S2
4	V_{SS}	13	V_{DD}
5	GND	12	NC
6	S4	11	S3
7	D4	10	D3
8	IN4	9	IN3

NOTES:

1. NC = Not Internally connected.

FIGURE 2. Terminal connections.

Case outline X		
Terminal		Description
Number	Mnemonic	
1	IN1	Switch 1 Digital Control Input.
2	D1	Drain Terminal of Switch 1. This pin can be an input or output.
3	S1	Source Terminal of Switch 1. This pin can be an input or output
4	V_{SS}	Most Negative Power Supply Terminal. Tie this pin to GND when using the device with single-supply voltages.
5	GND	Ground (0 V) Reference.
6	S4	Source Terminal of Switch 4. This pin can be an input or output.
7	D4	Drain Terminal of Switch 4. This pin can be an input or output.
8	IN4	Switch 4 Digital Control Input.
9	IN3	Switch 3 Digital Control Input.
10	D3	Drain Terminal of Switch 3. This pin can be an input or output.
11	S3	Source Terminal of Switch 3. This pin can be an input or output.
12	NC	Not Internally Connected.
13	V_{DD}	Most Positive Power Supply Terminal.
14	S2	Source Terminal of Switch 2. This pin can be an input or output.
15	D2	Drain Terminal of Switch 2. This pin can be an input or output.
16	IN2	Switch 2 Digital Control Input.

FIGURE 3. Terminal function.

Logic	S1 and S4	S2 and S3
0	Off	On
1	On	Off

FIGURE 4. Truth table.

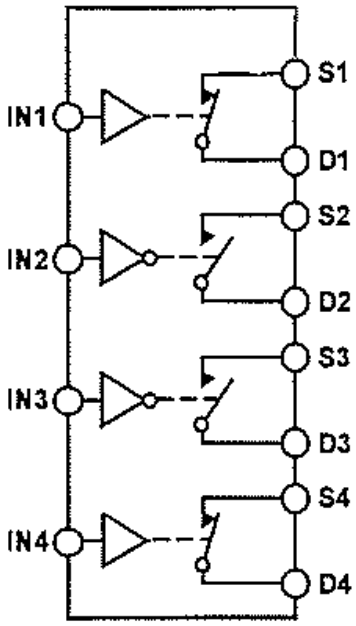


FIGURE 5. Functional block diagram.

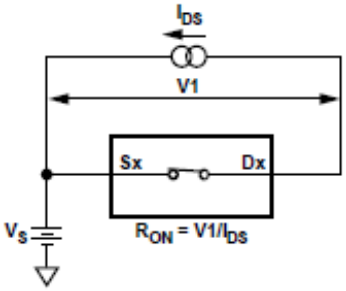


FIGURE 6. . On Resistance.

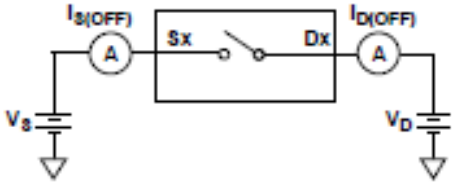


FIGURE 7 Off Leakage.

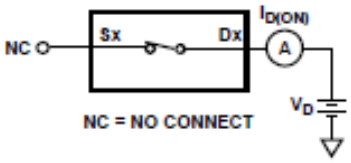


FIGURE 8. On Leakage.

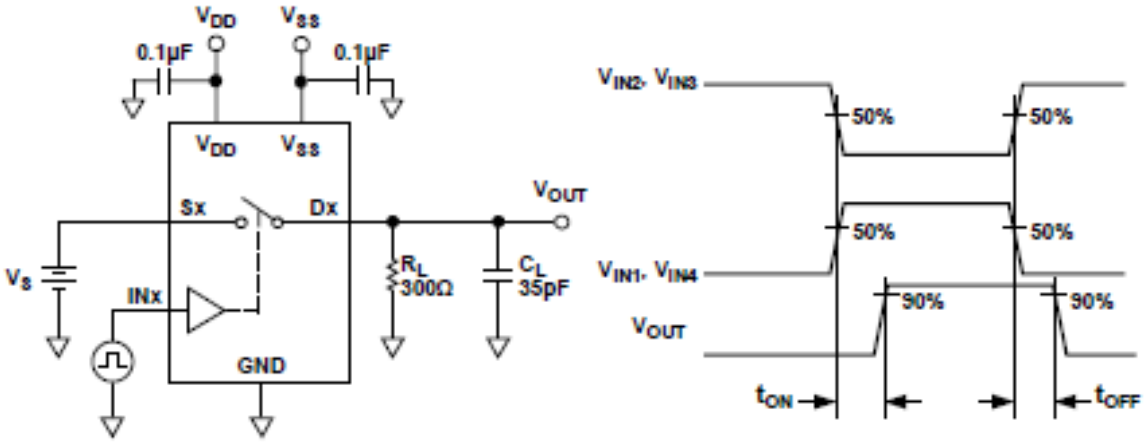


FIGURE 9. Switching times.

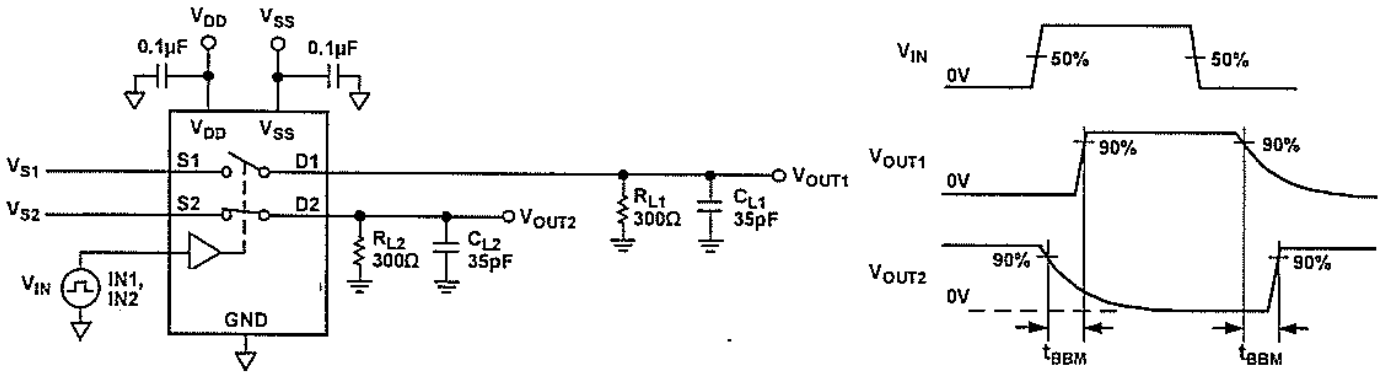


FIGURE 10. Break Before Make Time Delay.

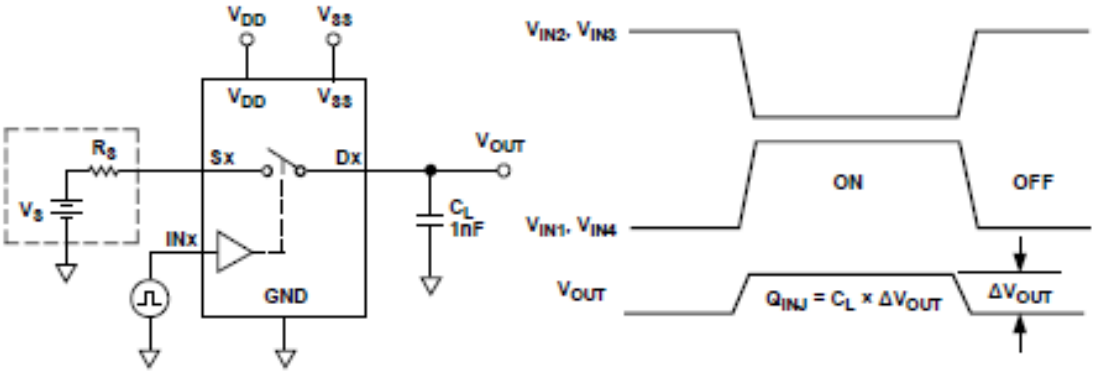


FIGURE 11. Charge Injection.

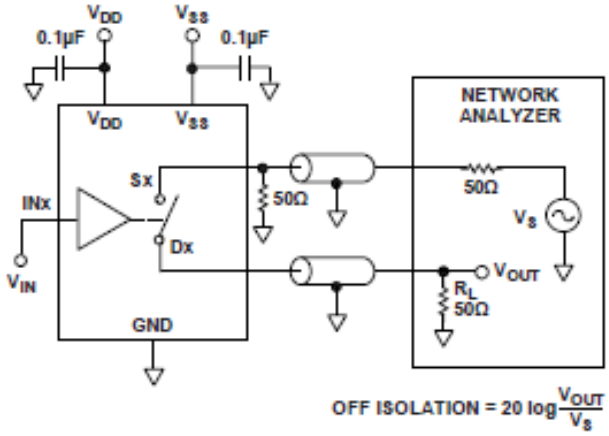


FIGURE 12. Off Isolation.

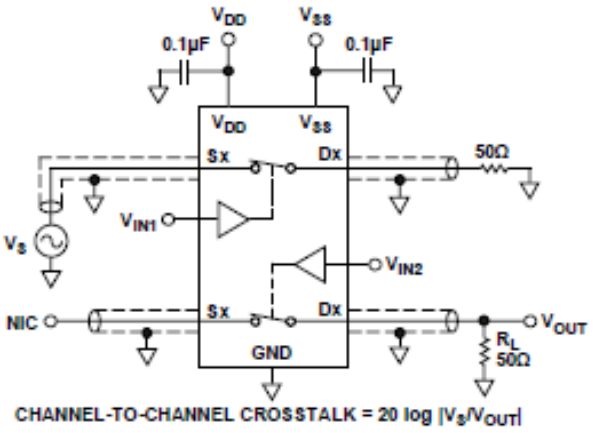


FIGURE 13. Channel to Channel Crosstalk.

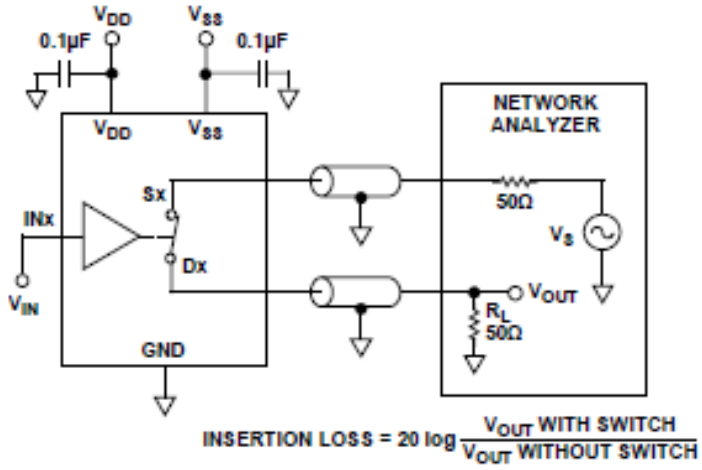


FIGURE 14. Bandwidth. (Fig 22)

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Ordering Quantity	Vendor part number
V62/16617-01XE	24355	Tube 96 units	ADG613SRUZ-EP
		Reel 1000 units	ADG613SRUZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106