REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update document paragraphs to current requirements. - ro	21-08-19	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A	A							
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 16-09-14	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, LOW DISTORTION DIFFERENTIAL RF/IF AMPLIFIER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/16616**
	REV **A**	**PAGE** 1 **OF** 12

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V066-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low distortion differential radio frequency (RF) / intermediate frequency (IF) amplifier microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16616	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD8351-EP	Low distortion differential RF / IF amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-220-WEED-4	Lead frame quad chip scale package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (VPOS)	6 V
PWUP voltage	VPOS
Internal power dissipation (P_D)	320 mW
Maximum junction temperature (T_J)	125°C
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature range (soldering, 60 seconds)	+300°C
Thermal resistance, junction to ambient (θ_{JA})	79.1°C/W

1.4 Recommended operating conditions. 2/

Supply voltage (VPOS)	5 V
Operating free-air temperature range (T_A)	-55°C to +105°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance.							
-3 dB bandwidth		A_V = 6 dB, $V_{OUT} \leq$ 1.0 Vp-p	25°C	01	3000 typical		MHz
		A_V = 12 dB, $V_{OUT} \leq$ 1.0 Vp-p			2200 typical		
		A_V = 18 dB, $V_{OUT} \leq$ 1.0 Vp-p			600 typical		
Bandwidth for 0.1 dB flatness		0 dB $\leq A_V \leq$ 20 dB, $V_{OUT} \leq$ 1.0 Vp-p	25°C	01	200 typical		MHz
Bandwidth for 0.2 dB flatness		0 dB $\leq A_V \leq$ 20 dB, $V_{OUT} \leq$ 1.0 Vp-p	25°C	01	400 typical		MHz
Gain accuracy		Using 1% resistor for R_G, 0 dB $\leq A_V \leq$ 20 dB	25°C	01	$\pm$1 typical		dB
Gain supply sensitivity		V_S $\pm$5%	25°C	01	0.08 typical		dB/V
Gain temperature sensitivity			-55°C to +105°C	01	3.9 typical		mdB/°C
Slew rate		R_L = 1 kΩ, V_{OUT} = 2 V step	25°C	01	13000 typical		V/μs
		R_L = 150 Ω, V_S = 2 V step			7500 typical		
Settling time		1 V step to 1%	25°C	01	< 3 typical		ns
Overdrive recovery time		V_{IN} = 4 V to 0 V step, $V_{OUT} \leq \pm$10 mV	25°C	01	< 2 typical		ns
Reverse isolation (S12)			25°C	01	-67 typical		dB
Input/output characteristics.							
Input common mode voltage adjustment range			25°C	01	1.2 to 3.8 typical		V
Maximum output voltage swing		1 dB compressed	25°C	01	4.75 typical		Vp-p
Output common mode offset			25°C	01	40 typical		mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input/output characteristics – continued.							
Output common mode drift			-55°C to +105°C	01	0.24 typical		mV/°C
Output differential offset voltage			25°C	01	20 typical		mV
Output differential offset drift			-55°C to +105°C	01	0.13 typical		mV/°C
Input bias current			25°C	01	±15 typical		µA
Input resistance 3/			25°C	01	5 typical		kΩ
Input capacitance 3/			25°C	01	0.8 typical		pF
Common mode rejection ratio	CMRR		25°C	01	43 typical		dB
Output resistance 3/			25°C	01	150 typical		Ω
Output capacitance 3/			25°C	01	0.8 typical		pF
Power interface.							
Supply voltage			25°C	01	3	5.5	V
PWUP threshold			25°C	01	1.3 typical		V
PWUP input bias current		PWUP at 5 V	25°C	01	100 typical		µA
		PWUP at 0 V			25 typical		
Quiescent current			-55°C to +105°C	01	28 typical		mA
						35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Noise/distortion at 10 MHz.							
Second/third 4/ harmonic distortion		R_L = 1 kΩ, V_{OUT} = 2 Vp-p	25°C	01	-95/-93 typical		dBc
		R_L = 150 Ω, V_{OUT} = 2 Vp-p			-80/-69 typical		
Third order intermodulation distortion	IMD	R_L = 1 kΩ, f1 = 9.5 MHz, f2 = 10.5 MHz, V_{OUT} = 2 Vp-p composite	25°C	01	-90 typical		dBc
		R_L = 150 Ω, f1 = 9.5 MHz, f2 = 10.5 MHz, V_{OUT} = 2 Vp-p composite			-70 typical		
Output third order intercept		f1 = 9.5 MHz, f2 = 10.5 MHz	25°C	01	33 typical		dBm
Noise spectral density (referred to input, RTI)			25°C	01	2.65 typical		nV/$\sqrt{Hz}$
1 dB compression point			25°C	01	13.5 typical		dBm
Noise/distortion at 70 MHz							
Second/third 4/ harmonic distortion		R_L = 1 kΩ, V_{OUT} = 2 Vp-p	25°C	01	-79/-81 typical		dBc
		R_L = 150 Ω, V_{OUT} = 2 Vp-p			-65/-66 typical		
Third order intermodulation distortion	IMD	R_L = 1 kΩ, f1 = 69.5 MHz, f2 = 70.5 MHz, V_{OUT} = 2 Vp-p composite	25°C	01	-85 typical		dBc
		R_L = 150 Ω, f1 = 69.5 MHz, f2 = 70.5 MHz, V_{OUT} = 2 Vp-p composite			-69 typical		
Output third order intercept		f1 = 69.5 MHz, f2 = 70.5 MHz	25°C	01	31 typical		dBm
Noise spectral density (referred to input, RTI)			25°C	01	2.70 typical		nV/$\sqrt{Hz}$
1 dB compression point			25°C	01	13.3 typical		dBm

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Noise/distortion at 140 MHz							
Second/third 4/ harmonic distortion		R_L = 1 kΩ, V_{OUT} = 2 Vp-p	25°C	01	-69/-69 typical		dBc
		R_L = 150 Ω, V_{OUT} = 2 Vp-p			-54/-53 typical		
Third order intermodulation distortion	IMD	R_L = 1 kΩ, f1 = 139.5 MHz, f2 = 140.5 MHz, V_{OUT} = 2 Vp-p composite	25°C	01	-79 typical		dBc
		R_L = 150 Ω, f1 = 139.5 MHz, f2 = 140.5 MHz, V_{OUT} = 2 Vp-p composite			-67 typical		
Output third order intercept		f1 = 139.5 MHz, f2 = 140.5 MHz	25°C	01	29 typical		dBm
Noise spectral density (referred to input, RTI)			25°C	01	2.75 typical		$nV/\sqrt{Hz}$
1 dB compression point			25°C	01	13 typical		dBm
Noise/distortion at 240 MHz							
Second/third 4/ harmonic distortion		R_L = 1 kΩ, V_{OUT} = 2 Vp-p	25°C	01	-60/-66 typical		dBc
		R_L = 150 Ω, V_{OUT} = 2 Vp-p			-46/-50 typical		
Third order intermodulation distortion	IMD	R_L = 1 kΩ, f1 = 239.5 MHz, f2 = 240.5 MHz, V_{OUT} = 2 Vp-p composite	25°C	01	-76 typical		dBc
		R_L = 150 Ω, f1 = 239.5 MHz, f2 = 240.5 MHz, V_{OUT} = 2 Vp-p composite			-62 typical		
Output third order intercept		f1 = 239.5 MHz, f2 = 240.5 MHz	25°C	01	27 typical		dBm
Noise spectral density (referred to input, RTI)			25°C	01	2.90 typical		$nV/\sqrt{Hz}$
1 dB compression point			25°C	01	13 typical		dBm

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_S = 5 V, R_L = 150 Ω, R_G = 110 Ω, A_V = 10 dB, f = 70 MHz, T_A = +25°C and some parameters may be specified differentially. The gain (A_V) can be set to any value between 0 dB and 26 dB.

3/ Values are specified differentially.

4/ See the manufacturer's datasheet for information about single ended to differential operation.

Case X

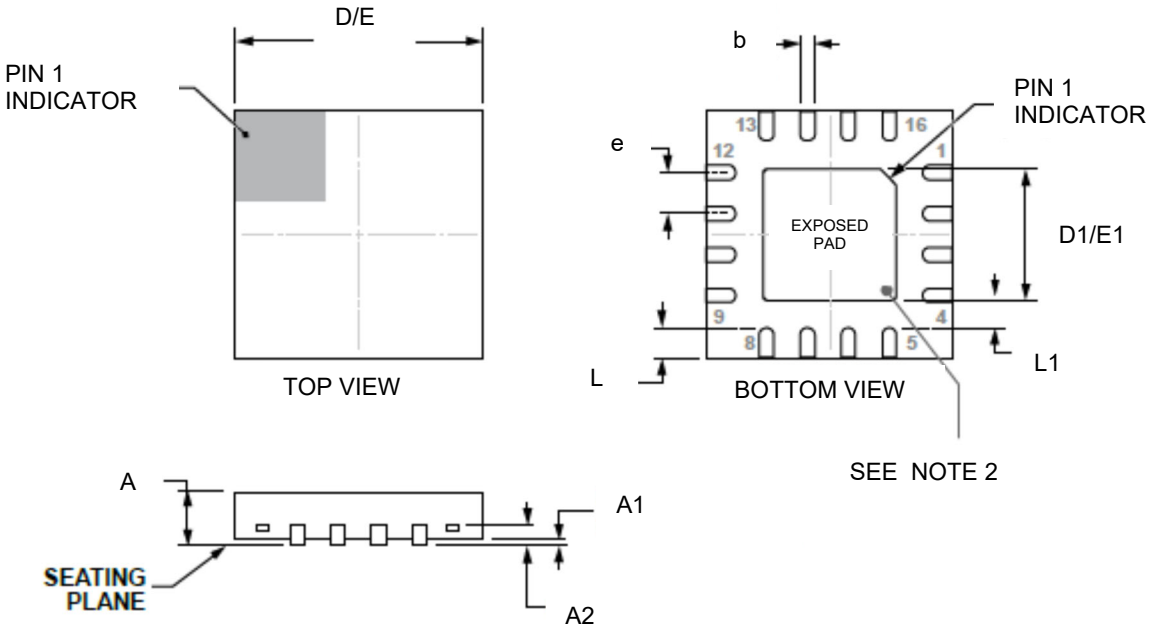

FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Max
A	.0275	.0295	.0314	0.70	0.75	0.80
A1	.0031 COPLANARITY	.0007 NOM	.0019	0.08 COPLANARITY	0.02 NOM	0.05
A2	.0079 REF			0.203 REF		
b	.0070	.0098	.0118	0.18	0.25	0.30
D/E	.1141	.1181	.1220	2.90	3.00	3.10
D1/E1	.0629	.0669 SQ	.0708	1.60	1.70 SQ	1.80
e	.0196 BSC			0.50 BSC		
L	.0118	.0157	.0177	0.30	0.40	0.45
L1	.0078	---	---	0.20	---	---

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
3. Falls within reference to JEDEC MO-220-WEED-4.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	RGP1	Gain resistor input 1.
2	INHI	Balanced differential input, high. Biased to midsupply, typically ac-coupled.
3	INLO	Balanced differential input, low. Biased to midsupply, typically ac-coupled.
4	RGP2	Gain resistor input 2.
5	NC	No connect. Do not connect to this pin.
6	NC	No connect. Do not connect to this pin.
7	NC	No connect. Do not connect to this pin.
8	NC	No connect. Do not connect to this pin.
9	COMM	Device common. Connect this pin to a low impedance ground.
10	OPLO	Balanced differential output, low. Biased to VOCM, typically ac-coupled.
11	OPHI	Balanced differential output, high. Biased to VOCM, typically ac-coupled.
12	VPOS	Positive supply voltage. 3 V to 5.5 V.
13	VOCM	Input/output common mode voltage. The voltage applied to this pin sets the common mode voltage at both the input and output. This pin is typically decoupled to ground with 0.1 μF capacitor.
14	NC	No connect. Do not connect to this pin.
15	NC	No connect. Do not connect to this pin.
16	PWUP	Apply a positive voltage ($1.3\ V \leq V_{PWUP} \leq VPOS$) to activate the device.
	EXPOSED PAD	Exposed pad. The exposed pad is internally connected to GND and must be soldered to a low impedance ground plane.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/16616-01XE	24355	Tube, 50 units	AD8351SCPZ-EP
V62/16616-01XE	24355	Reel, 1500 units	AD8351SCPZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123