REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update document paragraphs to current requirements. - ro	22-04-14	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16						

PMIC N/A

Original date of drawing

YY-MM-DD
17-01-25

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TITLE
MICROCIRCUIT, LINEAR, PRECISION, ULTRALOW NOISE, RRIO, ZERO DRIFT OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/16615
REV	A	PAGE 1 OF 16

AMSC N/A

5962-V039-22

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance precision, ultralow noise, rail to rail input and output (RRIO), zero drift operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16615	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADA4528-2	Precision, ultralow noise, (RRIO), zero drift operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	See figure 1	Square lead frame chip scale package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_S)	6 V
Input voltage (VIN)	$\pm V_S$ ±0.3 V
Input current	±10 mA 2/
Differential input voltage	$\pm V_S$
Output short circuit duration to GND	Indefinite
Power dissipation (P_D) with T_J under +150°C	400 mW
Lead temperature (soldering, 60 seconds)	+300°C
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature range (T_J)	-65°C to +150°C
Thermal resistance, junction to case (θ_{JC})	3.9°C/W
Thermal resistance, junction to ambient (θ_{JA})	52°C/W

1.4 Recommended operating conditions. 3/

Operating temperature range (T_A)	-55°C to +125°C

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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input pins have clamp diodes to the power supply pins. Limits the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https:/www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_S = 2.5 V, V_{CM} = V_S/2 unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input characteristics							
Offset voltage	V_{OS}	V_{CM} = 0 V to 2.5 V	+25°C	01		2.5	µV
					0.3 typical		
			-55°C to +125°C			4.3	
Offset voltage drift	$\Delta V_{OS}/\Delta T$		-55°C to +125°C	01		0.018	µV/°C
					0.002 typical		
Input bias current	I_B		+25°C	01		400	pA
					220 typical		
			-55°C to +125°C			600	
Input offset current	I_{OS}		+25°C	01		800	pA
					440 typical		
			-55°C to +125°C			1	nA
Input voltage range			+25°C	01	0	2.5	V
Common mode rejection ratio	CMRR	V_{CM} = 0 V to 2.5 V	+25°C	01	135		dB
					158 typical		
			-55°C to +125°C		116		
Open loop gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 2.4 V	+25°C	01	130		dB
					140 typical		
			-55°C to +125°C		126		
		R_L = 2 kΩ, V_O = 0.1 V to 2.4 V	+25°C		122		
					132 typical		
			-55°C to +125°C		119		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = 2.5 V, V_{CM} = V_S/2 unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input characteristics – continued.							
Input resistance, differential mode	R_{INDM}		+25°C	01	225 typical		kΩ
Input resistance, common mode	R_{INCM}		+25°C	01	1 typical		GΩ
Input capacitance, differential mode	C_{INDM}		+25°C	01	15 typical		pF
Input capacitance, common mode	C_{INCM}		+25°C	01	30 typical		pF
Output characteristics							
Output voltage high	V_{OH}	R_L = 10 kΩ to V_{CM}	+25°C	01	2.49		V
					2.495 typical		
			-55°C to +125°C		2.485		
		R_L = 2 kΩ to V_{CM}	+25°C		2.46		
					2.48 typical		
			-55°C to +125°C		2.44		
Output voltage low	V_{OL}	R_L = 10 kΩ to V_{CM}	+25°C	01		10	mV
					5 typical		
			-55°C to +125°C			15	
		R_L = 2 kΩ to V_{CM}	+25°C			40	
					20 typical		
			-55°C to +125°C			60	
Short circuit current	I_{SC}		+25°C	01	±30 typical		mA
Closed loop output impedance	Z_{OUT}	f = 1 kHz, A_V = +10	+25°C	01	0.1 typical		Ω

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = 2.5 V, V_{CM} = V_S/2 unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply							
Power supply rejection ratio	PSRR	V_S = 2.2 V to 5.5 V	+25°C	01	130		dB
					150 typical		
			-55°C to +125°C		127		
Supply current per amplifier	I_{SY}	I_O = 0 mA	+25°C	01		1.7	mA
					1.4 typical		
			-55°C to +125°C			2.1	
Dynamic performance							
Slew rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = +1	+25°C	01	0.45 typical		V/μs
Settling time to 0.1%	t_S	V_{IN} = 1.5 V step, R_L = 10 kΩ, C_L = 100 pF, A_V = -1	+25°C	01	7 typical		μs
Unity gain crossover	UGC	V_{IN} = 10 mVp-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1	+25°C	01	4 typical		MHz
Phase margin	ΦM	V_{IN} = 10 mVp-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1	+25°C	01	57 typical		Degrees
Gain bandwidth product	GBP	V_{IN} = 10 mVp-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +100	+25°C	01	3 typical		MHz
-3 dB closed loop bandwidth	f_{-3dB}	V_{IN} = 10 mVp-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1	+25°C	01	6.2 typical		MHz
Overload recovery time		R_L = 10 kΩ, C_L = 100 pF, A_V = -10	+25°C	01	50 typical		μs

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = 2.5 V, V_{CM} = V_S/2 unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Noise performance							
Voltage noise	e_{np-p}	f = 0.1 Hz to 10 Hz, A_V = +100	+25°C	01	97 typical		nVp-p
Voltage noise density	e_n	f = 1 kHz, A_V = +100	+25°C	01	5.6 typical		nV / $\sqrt{Hz}$
		f = 1 kHz, A_V = +100, V_{CM} = 2.0 V			5.5 typical		
Current noise	i_{np-p}	f = 0.1 Hz to 10 Hz, A_V = +100	+25°C	01	10 typical		pAp-p
Current noise density	i_n	f = 1 kHz, A_V = +100	+25°C	01	0.7 typical		pA / $\sqrt{Hz}$

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = 5 V, V_{CM} = V_S/2 unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input characteristics							
Offset voltage	V_{OS}	V_{CM} = 0 V to 5 V	+25°C	01		2.5	µV
					0.3 typical		
			-55°C to +125°C			4	
Offset voltage drift	$\Delta V_{OS}/\Delta T$		-55°C to +125°C	01		0.015	µV/°C
					0.002 typical		
Input bias current	I_B		+25°C	01		250	pA
					125 typical		
			-55°C to +125°C			400	
Input offset current	I_{OS}		+25°C	01		500	pA
					250 typical		
			-55°C to +125°C			650	
Input voltage range			+25°C	01	0	5	V
Common mode rejection ratio	CMRR	V_{CM} = 0 V to 5 V	+25°C	01	137		dB
					160 typical		
			-55°C to +125°C		122		
Open loop gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 4.9 V	+25°C	01	127		dB
					139 typical		
			-55°C to +125°C		125		
		R_L = 2 kΩ, V_O = 0.1 V to 4.9 V	+25°C		121		
					131 typical		
			-55°C to +125°C		120		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = 5 V, V_{CM} = V_S/2 unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input characteristics – continued.							
Input resistance, differential mode	R_{INDM}		+25°C	01	190 typical		kΩ
Input resistance, common mode	R_{INCM}		+25°C	01	1 typical		GΩ
Input capacitance, differential mode	C_{INDM}		+25°C	01	16.5 typical		pF
Input capacitance, common mode	C_{INCM}		+25°C	01	33 typical		pF
Output characteristics							
Output voltage high	V_{OH}	R_L = 10 kΩ to V_{CM}	+25°C	01	4.99		V
					4.995 typical		
			-55°C to +125°C		4.98		
		R_L = 2 kΩ to V_{CM}	+25°C		4.96		
					4.98 typical		
			-55°C to +125°C		4.94		
Output voltage low	V_{OL}	R_L = 10 kΩ to V_{CM}	+25°C	01		10	mV
					5 typical		
			-55°C to +125°C			20	
		R_L = 2 kΩ to V_{CM}	+25°C			40	
					20 typical		
			-55°C to +125°C			60	
Short circuit current	I_{SC}		+25°C	01	±40 typical		mA
Closed loop output impedance	Z_{OUT}	f = 1 kHz, A_V = +10	+25°C	01	0.1 typical		Ω

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = 5 V, V_{CM} = V_S/2 unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply							
Power supply rejection ratio	PSRR	V_S = 2.2 V to 5.5 V	+25°C	01	130		dB
					150 typical		
			-55°C to +125°C		127		
Supply current per amplifier	ISY	I_O = 0 mA	+25°C	01		1.8	mA
					1.5 typical		
			-55°C to +125°C			2.2	
Dynamic performance							
Slew rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = +1	+25°C	01	0.5 typical		V/μs
Settling time to 0.1%	t_S	V_{IN} = 4 V step, R_L = 10 kΩ, C_L = 100 pF, A_V = -1	+25°C	01	10 typical		μs
Unity gain crossover	UGC	V_{IN} = 10 mVp-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1	+25°C	01	4 typical		MHz
Phase margin	ΦM	V_{IN} = 10 mVp-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1	+25°C	01	57 typical		Degrees
Gain bandwidth product	GBP	V_{IN} = 10 mVp-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +100	+25°C	01	3.4 typical		MHz
-3 dB closed loop bandwidth	f_{-3dB}	V_{IN} = 10 mVp-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1	+25°C	01	6.5 typical		MHz
Overload recovery time		R_L = 10 kΩ, C_L = 100 pF, A_V = -10	+25°C	01	50 typical		μs

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = 5 V, V_{CM} = V_S/2 unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Noise performance							
Voltage noise	e_{np-p}	f = 0.1 Hz to 10 Hz, A_V = +100	+25°C	01	99 typical		nVp-p
Voltage noise density	e_n	f = 1 kHz, A_V = +100	+25°C	01	5.9 typical		nV / $\sqrt{Hz}$
		f = 1 kHz, A_V = +100, V_{CM} = 4.5 V			5.3 typical		
Current noise	i_{np-p}	f = 0.1 Hz to 10 Hz, A_V = +100	+25°C	01	10 typical		pAp-p
Current noise density	i_n	f = 1 kHz, A_V = +100	+25°C	01	0.5 typical		pA / $\sqrt{Hz}$

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X

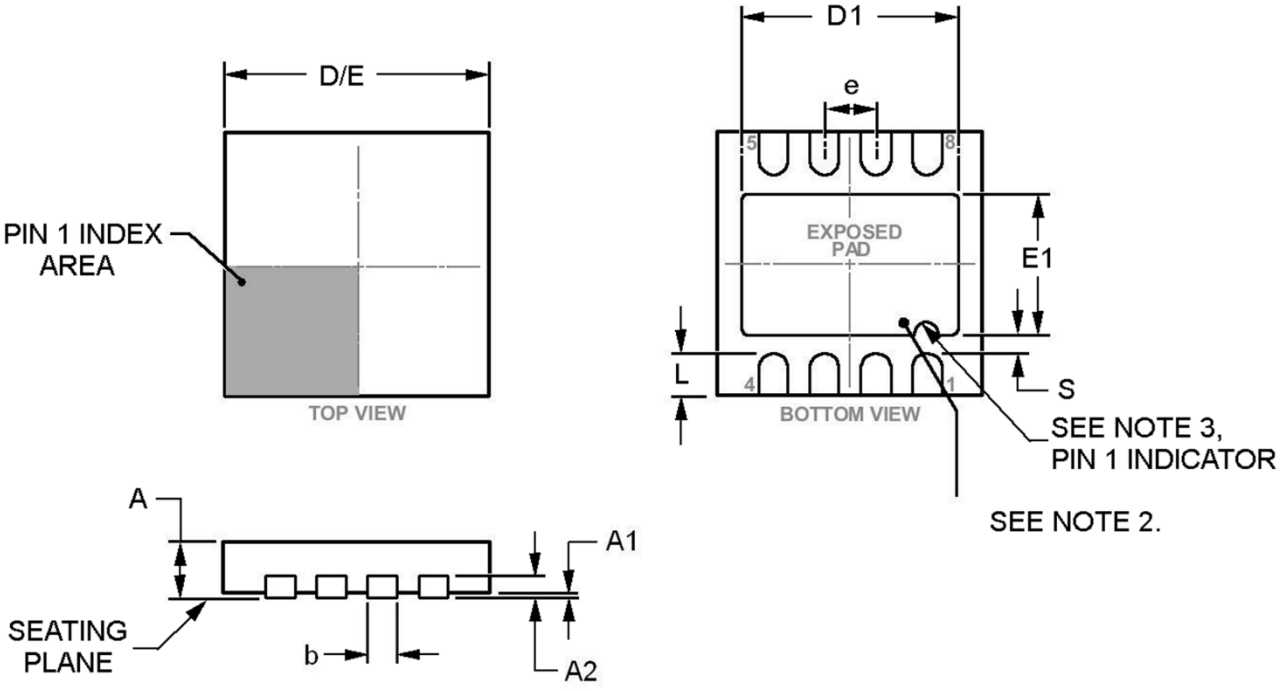

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/16615
		REV A	PAGE 13

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.0275	.0295	.0314	0.70	0.75	0.80
A1	.0007 NOM	---	.0019	0.02 NOM	---	0.05
A2	.0079 REF			0.203 REF		
b	.0078	.0118	.0137	0.20	0.30	0.35
D	.1141	.1181	.1220	2.90	3.00	3.10
D1	.0921	.0960	.0999	2.34	2.44	2.54
E	.1141	.1181	.1220	2.90	3.00	3.10
E1	.0590	.0629	.0669	1.50	1.60	1.70
e	.0255 BSC			0.65 BSC		
L	.0137	.0157	.0177	0.35	0.40	0.45
S	.0078	---	---	0.20	---	---

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
3. The pin 1 indicator's radius is 0.20 mm (.0078 inch).

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	OUT A	Output, channel A.
2	-IN A	Inverting input, channel A.
3	+IN A	Noninverting input, channel A.
4	$-V_S$	Negative supply voltage.
5	+IN B	Noninverting input, channel B.
6	-IN B	Inverting input, channel B.
7	OUT B	Output, channel B.
8	$+V_S$	Positive supply voltage
	EPAD	Exposed pad. Connect the exposed pad to $-V_S$ or leave it unconnected.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/16615-01XE	24355	Tray, 714 units	ADA4528-2TCPZ-EP
V62/16615-01XE	24355	Reel, 1500 units	ADA4528-2TCPZ-EPR7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123