REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A

PREPARED BY

Phu H. Nguyen

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil/

Original date of drawing
YY MM DD

16-07-12

CHECKED BY

Phu H. Nguyen

APPROVED BY

Thomas M. Hess

TITLE

MICROCIRCUIT, LINEAR-DIGITAL, WIDEBAND 2.5 GHz, 37 dB ISOLATION AT 1 GHz, CMOS, 1.65 V TO 2.75 V, 4:1 MUX/SP4T, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**	**DWG NO.**
A	**16236**	**V62/16614**

REV

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AMSC N/A

5962-V082-16

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Wideband 2.5 GHz, 37 dB Isolation at 1 GHz, CMOS, 1.65 V to 2.75 V, 4:1 Mux/SP4T microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16614	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG904 –EP	Wideband 2.5 GHz, 37 dB Isolation at 1 GHz, CMOS, 1.65 V to 2.75 V, 4:1 Mux/SP4T

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-220	Lead Frame Chip Scale Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to GND	-0.5 V to +4 V 2/
Inputs to GND	−0.5 V to V_{DD} + 0.3 V 2/ 3/
Continuous Current	Data 4/ + 15%
Input Power	18 dBm 5/
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
Lead temperature (Soldering, 10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C
Electrostatic Discharge (ESD)	1 kV

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA}	θ_{JC}	Unit
Case X	30.4	2.83	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Tested at −55°C to +125°C.
3/ RFx off port inputs to ground = −0.5 V to VDD − 0.5 V.
4/ See Table I.
5/ Input power is tested with switch in both open and close position. Power is applied on RFx, while RFC is terminated to a 50 Ω resistor to GND.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 Switching Timing, $t_{ON(EN)}$ and $t_{OFF(EN)}$. The Switching Timing, $t_{ON(EN)}$ and $t_{OFF(EN)}$ shall be as shown in figure 6.

3.5.7 Switching Timing, t_{RISE} and t_{FALL}. The Switching Timing, t_{RISE} and t_{FALL} shall be as shown in figure 7.

3.5.8 Off Isolation. The Off Isolation shall be as shown in figure 8.

3.5.9 Insertion Loss. The Insertion Loss shall be as shown in figure 9.

3.5.10 Crosstalk. The Crosstalk shall be as shown in figure 10.

3.5.11 Video Feedthrough. The Video Feedthrough shall be as shown in figure 11.

3.5.12 Third-Order Intermodulation Intercept (IP3). The Third-Order Intermodulation Intercept (IP3) shall be as shown in figure 12.

3.5.13 1 dB Input Compression (P1 dB). The 1 dB Input Compression (P1 dB) shall be as shown in figure 13.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ 3/	Max	
AC Electrical Characteristics						
−3 dB Frequency 4/				2.5		GHz
Insertion Loss	S12, S21	DC to 100 MHz; VDD = 2.5 V ±10%; see Figure 9		0.5	1	dB
		500 MHz; VDD = 2.5 V ±10%		0.7	1.2	
		1000 MHz; VDD = 2.5 V ±10%		1.1	1.8	
Isolation—RFC to RF1x	S12, S21	100 MHz; see Figure 8	51	60		dB
		500 MHz; see Figure 8	35	45		
		1000 MHz; see Figure 8	30	37		
Crosstalk	S12, S21	100 MHz; see Figure 10	50	58		dB
		500 MHz; see Figure 10	32	35		
		1000 MHz; see Figure 10	30	35		
Return Loss 4/	S11, S21					dB
On Channel		DC to 100 MHz	19	27		
		500 MHz		26		
		1000 MHz		18		
Off Channel		DC to 100 MHz	14	22		
		500 MHz		19		
		1000 MHz		18		
Timing						ns
On Switching Time 4/	$t_{ON\ (\overline{EN})}$	50% $\overline{EN}$ to 90% RF; see Figure 6		8.5	10	
Off Switching Time 4/	$t_{OFF\ (\overline{EN})}$	50% $\overline{EN}$ to 10% RF; see Figure 6		13	16	
Transition Time	t_{TRANS}	50% A0/A1 to 10% RF		12	15	
Rise Time 4/	t_{RISE}	10% to 90% RF; see Figure 7		3	5	
Fall Time 4/	t_{FALL}	90% to 10% RF; see Figure 7		7.5	11	
Third-Order Intermodulation Intercept	IP3	900 MHz/901 MHz, 4 dBm; see Figure 12	25	31		dBm
Video Feedthrough 5/		See Figure 11		3		mV p-p
Input Power						
1 dB Input Compression	P1dB	1000 MHz 6/; see Figure 13		16		dBm
DC Electrical Characteristics						
Input High Voltage	V_{INH}	V_{DD} = 2.25 V to 2.75 V	1.7			V
		V_{DD} = 1.65 V to 1.95 V	0.65 V_{DD}			V
Input Low Voltage	V_{INL}	V_{DD} = 2.25 V to 2.75 V			0.7	V
		V_{DD} = 1.65 V to 1.95 V			0.35 V_{DD}	V
Input Leakage Current	I_I	0 V ≤ VIN ≤ 2.75 V		±0.1	±1	µA
Capacitance 4/						
RF Port On Capacitance	$C_{RF\ ON}$			3		pF
Digital Input Capacitance	C			2		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/		Limits			Unit
				Min	Typ	Max	
Power Requirements							
V_{DD}				1.65		2.75	V_{DD}
Quiescent Power Supply Current	I_{DD}	Digital inputs = 0 V or V_{DD}			0.1	2.5	µA
Continuous Current per Channel							
V_{DD} = 2.75 V, V_{SS} = 0 V		Case outline X, θ_{JA} = 30.4 °C/W, dc bias = 0.5 V	25°C			93.1	mA
			85°C			10.8	
			105°C			5.9	
			125°C			3.3	
V_{DD} = 1.65 V, V_{SS} = 0 V			25°C			82.6	
			85°C			10.8	
			105°C			5.9	
			125°C			3.3	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 1.65 V to 2.75 V, GND = 0 V, input power = 0 dBm, temperature range = −55°C to +125°C, unless otherwise noted.

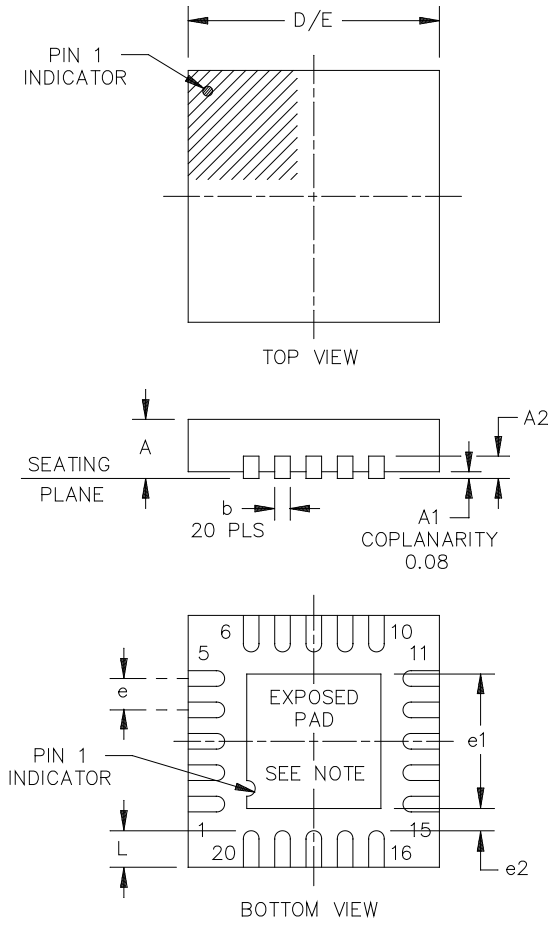
3/ Typical values are at VDD = 2.5 V and 25°C, unless otherwise stated.

4/ Guaranteed by design, not subject to production test.

5/ Video feedthrough is the dc transience at the output of any port of the switch when the control voltage is switched from high to low or low to high in a 50 Ω test setup, measured with 1 ns rise time pulses and 500 MHz bandwidth.

6/ Lest than 100 MHz, refer to the AN-952 Application Note for more information about power handling.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.70	0.80	e	0.50 BSC	
A1		0.05	e1	2.00	2.30
A2	0.20 REF		e2	0.20	
b	0.18	0.30	L	0.55	0.65
D/E	3.90	4.10			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-220-WGGD-1.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	20	GND
2	RF1	19	V_{DD}
3	GND	18	$\overline{EN}$
4	GND	17	A0
5	FR3	16	A1
6	GND	15	GND
7	GND	14	RF2
8	RFC	13	GND
9	GND	12	GND
10	GND	11	RF4

FIGURE 2. Terminal connections.

Terminal number	Mnemonic	Function
0	EPAD	Exposed Pad. The exposed pad is tied to the substrate, GND.
1, 3, 4, 6. 7. 9, 10, 12, 13, 15, 20	GND	Ground Reference Points for All Circuitry on the Device.
2	RF1	RF 1 Port.
5	RF3	RF 3 Port.
8	RFC	Common RF Port for Switch.
11	RF4	RF 4 Port.
14	RF2	RF 2 Port.
16	A1	Logic Control Input 1.
17	A0	Logic Control Input 0.
18	$\overline{EN}$	Active Low Digital Input. When high, the device is disabled and all switches are off. When low, Ax logic inputs determine on switches.
19	V_{DD}	Power Supply Input. This device operates from 1.65 V to 2.75 V. VDD must be decoupled to GND.

FIGURE 3. Terminal function.

A1	A0	$\overline{EN}$	On Switch 1/
X 2/	X 2/	1	None
0	0	0	RF1
0	1	0	RF2
1	0	0	RF3
1	1	0	RF4

1/ Off switches have 50 Ω termination to GND.
2/ X = Don't care

FIGURE 4. Truth table.

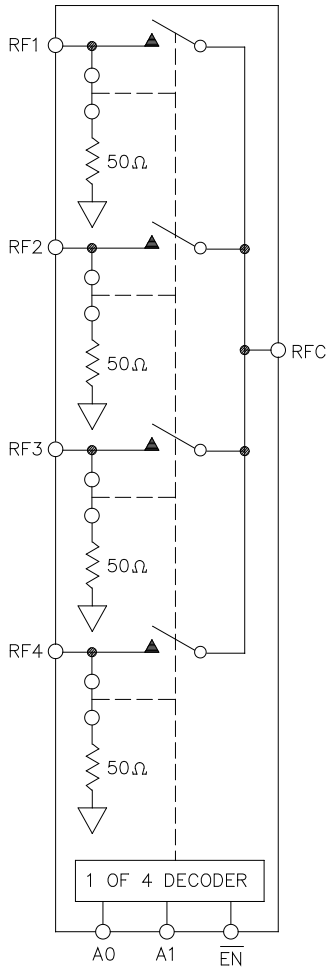


FIGURE 5. Functional block diagram.

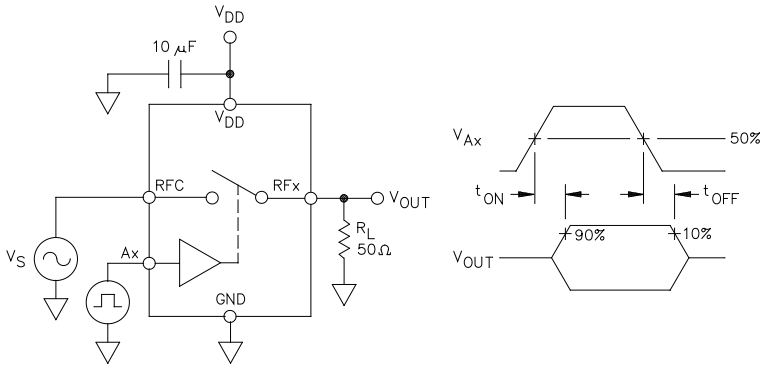


FIGURE 6. Switching Timing, $t_{ON(\overline{EN})}$ and $t_{OFF(\overline{EN})}$

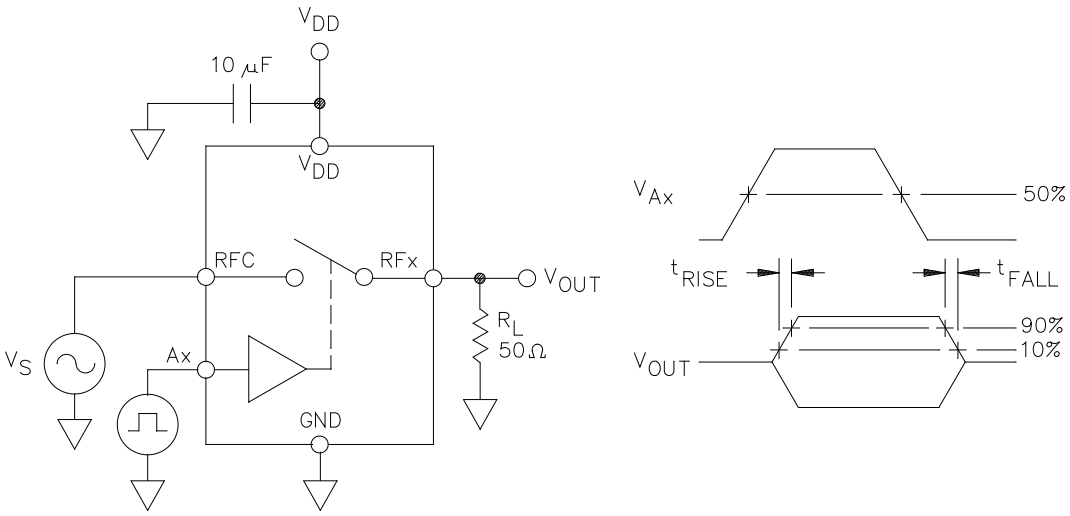


FIGURE 7. Switching Timing, t_{RISE} and t_{FALL}.

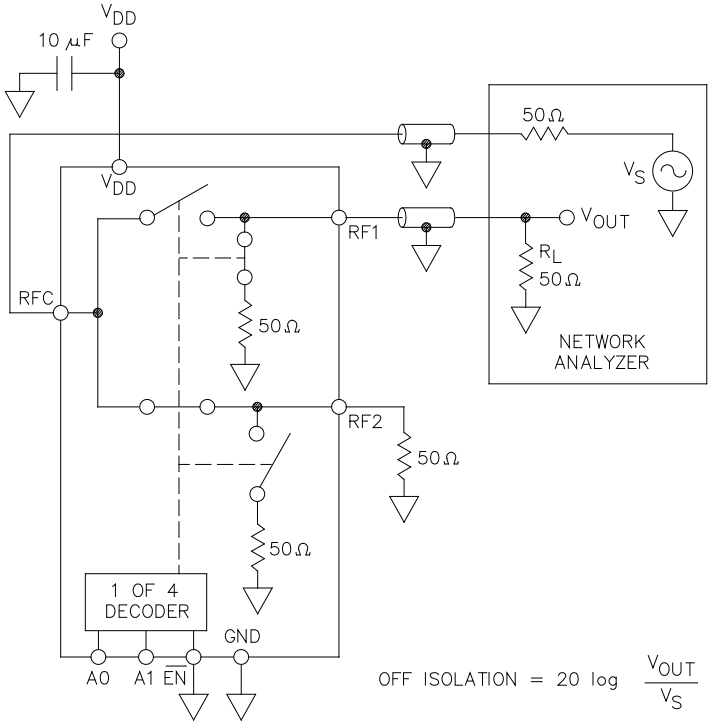


FIGURE 8. Off Isolation.

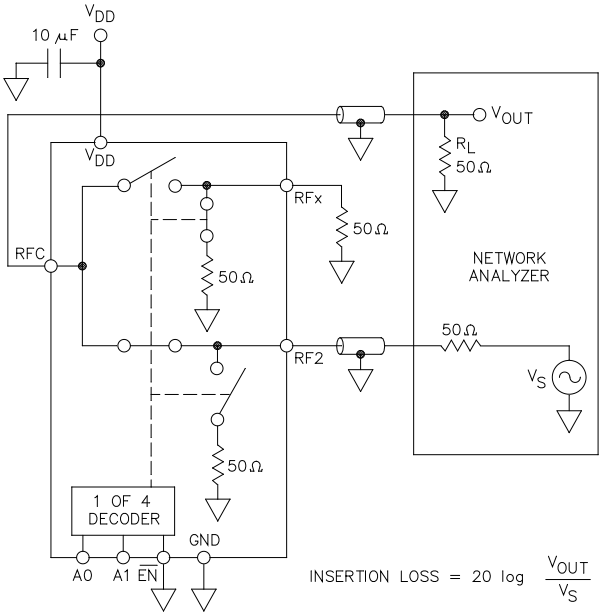


FIGURE 9. Isertion Loss.

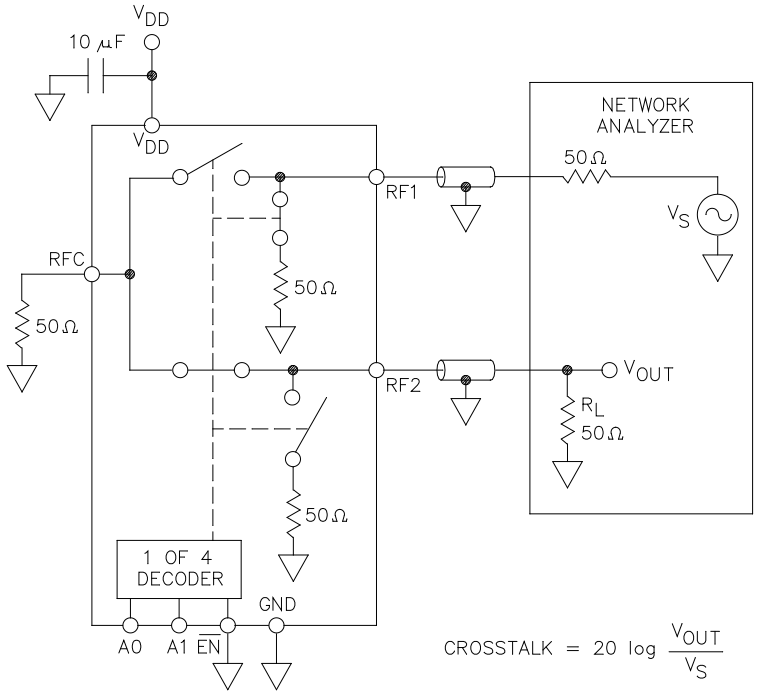


FIGURE 10. Crosstalk.

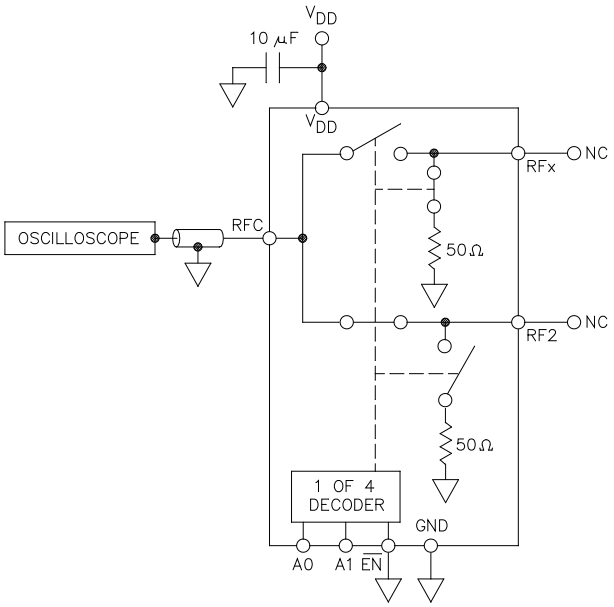


FIGURE 11. Video Feedthrough.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/16614
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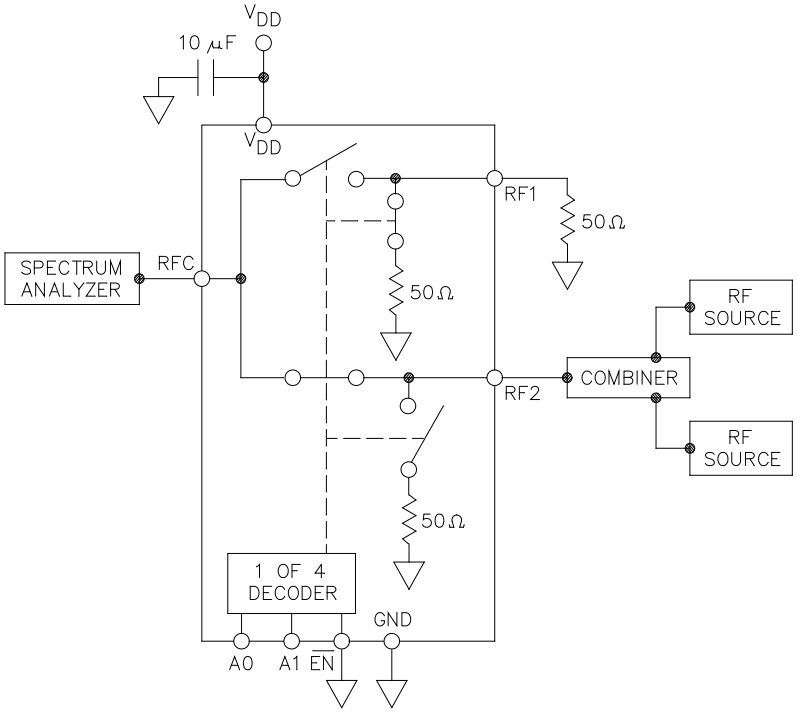

FIGURE 12. Third-Order Intermodulation Intercept (IP3).

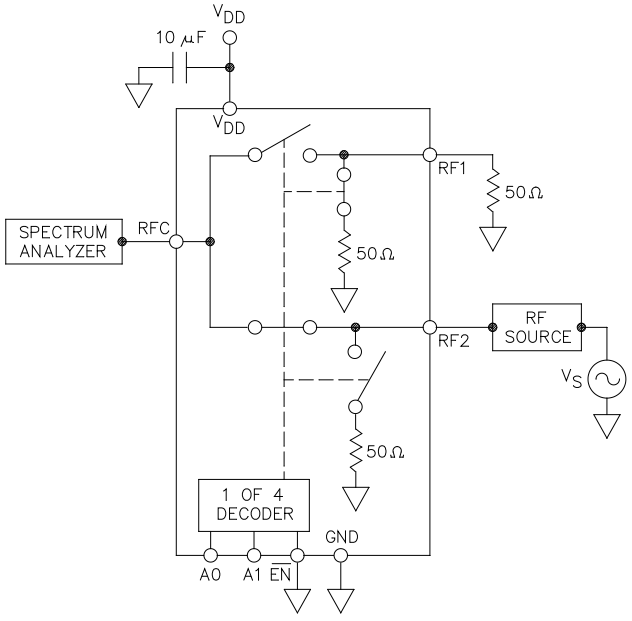

FIGURE 13. 1 dB Input Compression (P1dB).

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Transport media	Vendor part number
V62/16614-01XE	24355	Tube	ADG904SCPZ-EP
		Tape and reel	ADG904SCPZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106