REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil/

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CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

TITLE

MICROCIRCUIT, LINEAR, LOW DISTORTION, WIDE BANDWIDTH VOLTAGE FEEDBACK CLAMP AMPLIFIER, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	16236	V62/16612

REV

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AMSC N/A

5962-V107-16

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low distortion, wide bandwidth voltage feedback clamp amplifier microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16612	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD8037-EP	Low distortion, wide bandwidth voltage feedback clamp amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_S)	12.6 V
Power dissipation (P_D)	See figure 3
Voltage swing x bandwidth product	350 V- MHz
Common mode input voltage	$\pm V_S$
|High clamping voltage (V_H) – Input voltage (V_{IN})|	$\leq$ 6.3 V
|Low clamping voltage (V_L) – V_{IN}|	$\leq$ 6.3 V
Differential input voltage	$\pm$1.2 V
Storage temperature range (T_{STG})	-65°C to +125°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature range (T_J)	+150°C 2/
Thermal resistance, junction to ambient (θ_{JA})	155°C/W

1.4 Recommended operating conditions. 3/

Supply voltage range (V_S)	$\pm$5 V
Operating free-air temperature range (T_A)	-55°C to +105°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Exceeding a junction temperature of +175°C for an extended period can result in device failure.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Power dissipation graph. The power dissipation graph shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance.							
Small signal bandwidth at -3 dB		$V_{OUT} \leq 0.4$ Vp-p	+25°C	01	200		MHz
					270 typical		
Large signal 3/ bandwidth at -3 dB		V_{OUT} = 3.5 Vp-p	+25°C	01	160		MHz
					190 typical		
Bandwidth for 0.1 dB flatness		$V_{OUT} \leq 0.4$ Vp-p, R_F = 274 Ω	+25°C	01	130 typical		MHz
Slew rate, average ±		V_{OUT} = 4 V step, 10% to 90%	+25°C	01	1100		V/μs
					1500 typical		
Rise/fall time		V_{OUT} = 0.5 V step, 10% to 90%	+25°C	01	1.2 typical		ns
		V_{OUT} = 4 V step, 10% to 90%			2.2 typical		
Settling time to 0.1%		V_{OUT} = 2 V step	+25°C	01	10 typical		ns
Settling time to 0.01%		V_{OUT} = 2 V step	+25°C	01	16 typical		ns
Noise/harmonic performance.							
Second harmonic distortion		2 Vpp, 20 MHz, R_L = 100 Ω	+25°C	01		-45	dBc
					-52 typical		
		2 Vpp, 20 MHz, R_L = 500 Ω	+25°C			-65	
					-72 typical		
Third harmonic distortion		2 Vpp, 20 MHz, R_L = 100 Ω	+25°C	01		-63	dBc
					-70 typical		
		2 Vpp, 20 MHz, R_L = 500 Ω	+25°C			-73	
					-80 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Noise/harmonic performance – continued.							
Third order intercept		25 MHz	+25°C	01	41 typical		dBm
Noise figure		R_S = 50 Ω	+25°C	01	14 typical		dB
Input voltage noise		1 MHz to 200 MHz	+25°C	01	4.5 typical		$nV/\sqrt{Hz}$
Input current noise		1 MHz to 200 MHz	+25°C	01	2.1 typical		$pA/\sqrt{Hz}$
Average equivalent integrated input noise voltage		0.1 MHz to 200 MHz	+25°C	01	60 typical		μVrms
Differential gain error (3.58 MHz)		R_L = 150 Ω	+25°C	01		0.04	%
					0.02 typical		
Differential phase error (3.58 MHz)		R_L = 150 Ω	+25°C	01		0.04	Degree
					0.02 typical		
Phase nonlinearity		DC to 100 MHz	+25°C	01	1.1 typical		Degrees
Clamp performance							
Clamp voltage 3/ range		V_{CH} or V_{CL}	+25°C	01	±3.3		V
					±3.9 typical		
Clamp accuracy		2x overdrive, V_{CH} = 2 V, V_{CL} = -2 V	+25°C	01		±10	mV
					±3 typical		
			-55°C to 105°C			±20	
Clamp nonlinearity 4/ range			+25°C	01	100 typical		mV
Clamp input bias current (V_H or V_L)		V_H, V_L = ±0.5 V	+25°C	01		±70	μA
					±50 typical		
			-55°C to 105°C			±90	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Clamp performance – continued.							
Clamp input bandwidth (-3 dB)		V_{CH} or V_{CL} = 2 Vpp	+25°C	01	180		MHz
					270 typical		
Clamp overshoot		2x overdrive, V_{CH} or V_{CL} = 2 V_{PP}	+25°C	01		5	%
					1 typical		
Overdrive recovery		2x overdrive	+25°C	01	1.3 typical		ns
DC performance		R_L = 150 Ω, measured at A_V = 50					
Input offset voltage 5/	V_{IO}		+25°C	01		7	mV
					2 typical		
			-55°C to 105°C			10	
Offset voltage drift			+25°C	01	±10 typical		µV/°C
Input bias current	I_{IB}		+25°C	01		9	µA
					3 typical		
			-55°C to 105°C			15	
Input offset current	I_{IO}		+25°C	01		3	µA
					0.1 typical		
			-55°C to 105°C			5	
Common mode rejection ratio	CMRR	V_{CM} = ±2 V	+25°C	01	70		dB
					90 typical		
Open loop gain		V_{OUT} = ±2.5 V	+25°C	01	54		dB
					60 typical		
			-55°C to 105°C		46		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input characteristics.							
Input resistance	R_{IN}		+25°C	01	500 typical		kΩ
Input capacitance	C_{IN}		+25°C	01	1.2 typical		pF
Input common mode voltage range			+25°C	01	±2.5 typical		V
Output characteristics.							
Output voltage range		R_L = 150 Ω	+25°C	01	±3.2		V
					±3.9 typical		
Output current	C_{OUT}		+25°C	01	70 typical		mA
Output resistance	R_{OUT}		+25°C	01	0.3 typical		Ω
Short circuit current	I_{OS}		+25°C	01	240 typical		mA
Power supply							
Operating range			+25°C	01	±3.0	±6.0	V
					±5.0 typical		
Quiescent current			+25°C	01		19.5	mA
					18.5 typical		
			-55°C to 105°C			24	
Power supply rejection ratio	PSRR		+25°C	01	66 typical		dB
			-55°C to 105°C		56		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_S = ±5 V, resistance load (R_L) = 100 Ω, gain = +2, and V_H, V_L open.

3/ See the absolute maximum ratings section.

4/ Nonlinearity is defined as the voltage delta between the set input clamp voltage (V_H or V_L) and the voltage at which V_{OUT} starts deviating from V_{IN}.

5/ Measured with respect to the inverting input.

Case X

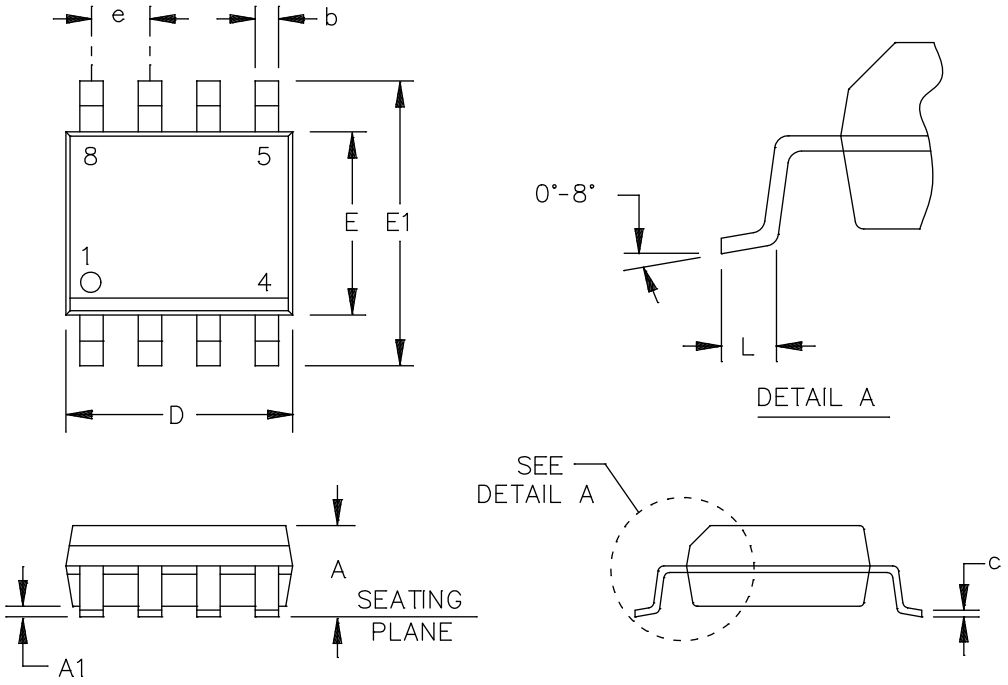

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/16612
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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.0500 BSC		1.27 BSC	
c	.0067	.0098	0.17	0.25
D	.1890	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
E1	.2284	.2441	5.80	6.20
L	.0157	.5000	0.40	1.27

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	NC	No connect.
2	-INPUT	Inverting input.
3	+INPUT	Noninverting input.
4	$-V_S$	Negative supply.
5	V_L	Low clamping voltage.
6	OUTPUT	Output.
7	$+V_S$	Positive supply.
8	V_H	High clamping voltage.

FIGURE 2. Terminal connections.

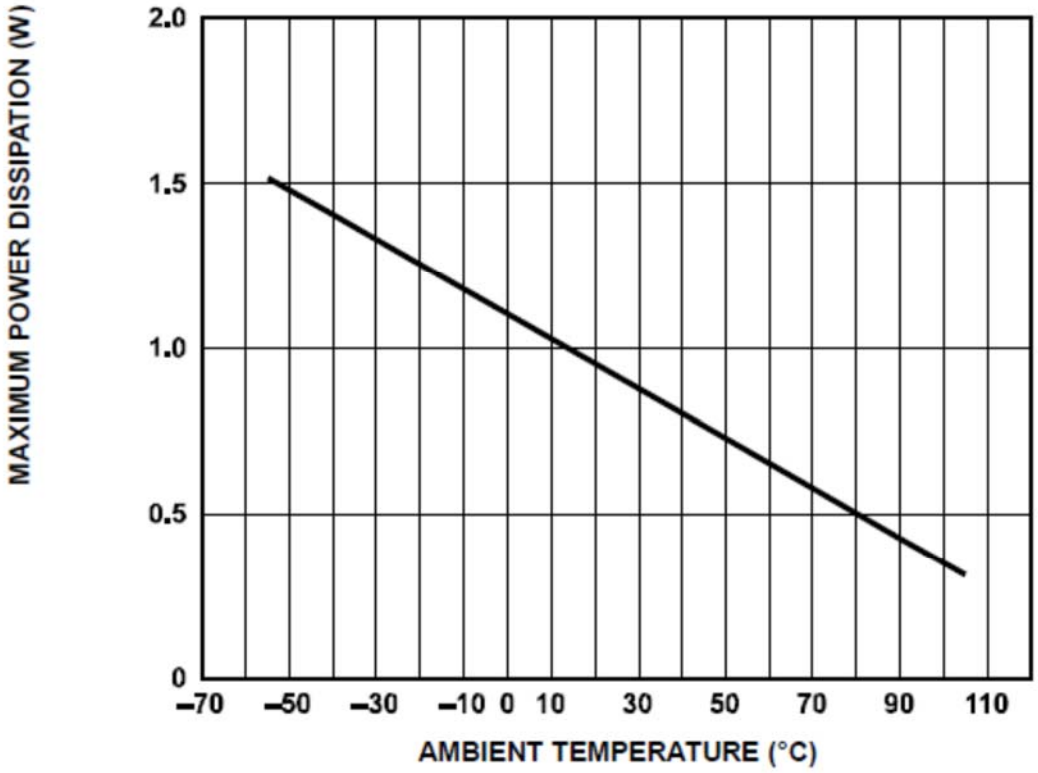

FIGURE 3. Power dissipation graph.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/16612-01XE	24355	Tube, 98 units	AD8037SRZ-EP
V62/16612-01XE	24355	Reel, 1000 units	AD8037SRZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland