REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Under figure 1 dimension table, delete the COPLANARITY limit entirely. Updated document paragraphs to current requirements. - ro	22-02-08	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets																						
REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19			

PMIC N/A

Original date of drawing
YY-MM-DD
16-10-14

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TITLE
MICROCIRCUIT, DIGITAL-LINEAR, 16 BIT, 250 MSPS, ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

SIZE	Cage Code	DWG No.
A	16236	V62/16611

REV	A	PAGE	1 of 19

AMSC N/A

5962-V097-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16 bit, 250 million samples per second (MSPS) analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16611	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD9467-EP	16 bit, 250 MSPS analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	72	MO-220-VNND-4	Lead frame chip scale package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Electrical section.
AVDD1, AVDD3 with respect to AGND ..... -0.3 V to +2.0 V
AVDD2, SPIVDD with respect to AGND ..... -0.3 V to +3.9 V
DRVDD with respect to DRGND ..... -0.3 V to +2.0 V
AGND with respect to DRGND ..... -0.3 V to +0.3 V
AVDD2, SPIVDD with respect to AVDD1, AVDD3 ..... -2.0 V to +3.9 V
AVDD1, AVDD3 with respect to DRVDD ..... -2.0 V to +2.0 V
AVDD2, SPIVDD with respect to DRVDD ..... -2.0 V to +3.9 V
Digital outputs with respect to DRGND:
(Dx+, Dx-, OR+, OR-, DCO+, DCO-) ..... -0.3 V to DRVDD + 0.2 V
CLK+, CLK- with respect to AGND ..... -0.3 V to AVDD1 + 0.2 V
VIN+, VIN- with respect to AGND ..... -0.3 V to +3.6 V
XVREF with respect to AGND ..... -0.3 V to AVDD1 + 0.2 V
SCLK, CSB, SDIO with respect to AGND ..... -0.3 V to SPIVDD + 0.2 V
Environmental section.
Junction temperature range (T_J) ..... +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Storage temperature range (T_{STG}) ambient ..... -65°C to +150°C

1.4 Recommended operating conditions. 2/

Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal impedance.

Air flow velocity (m/sec)	Thermal resistance, junction to ambient (θJA) 3/ 4/	Thermal resistance, junction to board (θJB) 3/ 5/ 6/	Thermal resistance, junction to case (θJC) 3/ 7/	Unit
0.0	15.7°C/W	7.5°C/W	0.5°	°C/W
1.0	13.7°C/W	N/A	N/A	°C/W
2.5	12.3°C/W	N/A	N/A	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
3/ Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
4/ Per JEDEC JESD 51-2 (still air) or JEDEC JESD 51-6 (moving air).
5/ Per JEDEC JESD 51-8 (still air).
6/ N/A means not applicable.
7/ Per MIL-STD883, method 1012.

2. APPLICABLE DOCUMENTS

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

Method 1012 - Thermal Characteristics.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

JEDEC Solid State Technology Association

EIA/JESD 51-2a - Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
EIA/JEDEC 51-5 - Extension of Thermal Conductivity Test Board Standards for Packages with Direct Thermal Attachment Mechanisms
EIA/JEDEC 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
EIA/JESD 51-8 - Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https:/www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 16 bit output data timing waveform. The 16 bit output data timing waveform and test circuit shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Specifications section.							
Resolution			+25°C	01	16		Bits
Accuracy							
No missing codes			-55°C to +125°C	01	Guaranteed typical		
Offset error			-55°C to +125°C	01	0 typical		LSB
					-200	+200	
Gain error			-55°C to +125°C	01	-0.1 typical		LSB
					-3.9	+2.6	
Differential 3/ nonlinearity	DNL		-55°C to +125°C	01	±0.5 typical		LSB
					-0.9	+1.5	
Integral 3/ nonlinearity	INL		-55°C to +125°C	01	±3.5 typical		LSB
					-12	+12	
Temperature drift							
Offset error			-55°C to +125°C	01	±0.023 typical		%FSR/°C
Gain error			-55°C to +125°C	01	±0.036 typical		%FSR/°C
Analog inputs							
Differential input voltage range		Internal VREF = 1 V to 1.25 V	-55°C to +125°C	01	2.5 typical		Vp-p
					2	2.5	
Common mode voltage			+25°C	01	2.15 typical		V
Differential input resistance			+25°C	01	530 typical		Ω
Differential input capacitance			+25°C	01	3.5 typical		pF
Full power bandwidth			+25°C	01	900 typical		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Specifications section - continued.							
XVREF input							
Input voltage			-55°C to +125°C	01	1	1.25	V
Input capacitance			-55°C to +125°C	01	3 typical		pF
Power supply							
1.8 V analog supply voltage	AVDD1		-55°C to +125°C	01	1.8 typical		V
					1.75	1.85	
3.3 V analog supply voltage	AVDD2		-55°C to +125°C	01	3.3 typical		V
					3.0	3.6	
1.8 V analog supply voltage	AVDD3		-55°C to +125°C	01	1.8 typical		V
					1.7	1.9	
1.8 V digital output driver supply voltage	DRVDD		-55°C to +125°C	01	1.8 typical		V
					1.7	1.9	
1.8 V analog supply current	IAVDD1		-55°C to +125°C	01	567 typical		mA
						620	
3.3 V analog supply current	IAVDD2		-55°C to +125°C	01	55 typical		mA
						61	
1.8 V analog supply current	IAVDD3		-55°C to +125°C	01	31 typical		mA
						35	
1.8 V digital output driver supply current	IDRVDD		-55°C to +125°C	01	40 typical		mA
						43	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Specifications section - continued.							
Power supply – continued.							
Total power dissipation (including output drivers)			-55°C to +125°C	01	1.33 typical		W
						1.5	
Power down dissipation			-55°C to +125°C	01	4.4 typical		mW
						90	
AC specification section							
Analog input full scale			-55°C to +125°C	01	2/2.5 typical		Vp-p
					2.5		
Signal to noise ratio	SNR	f_{IN} = 5 MHz	+25°C	01	74.7/76.4 typical		dBFS
		f_{IN} = 97 MHz	+25°C		74.5/76.1 typical		
		f_{IN} = 140 MHz	+25°C		74.4/76.0 typical		
		f_{IN} = 170 MHz	+25°C		74.3/75.8 typical		
					73.7		
			-55°C to +125°C		71.5		
		f_{IN} = 210 MHz	+25°C		74.0/75.5 typical		
		f_{IN} = 300 MHz	+25°C		73.3/74.6 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC specification section - continued.							
Signal to noise and distortion ratio	SINAD	f_{IN} = 5 MHz	+25°C	01	74.6/76.3 typical		dBFS
		f_{IN} = 97 MHz	+25°C		74.4/76.0 typical		
		f_{IN} = 140 MHz	+25°C		74.4/76.0 typical		
		f_{IN} = 170 MHz	+25°C		74.2/75.8 typical		
					72.4		
			-55°C to +125°C		71.0		
		f_{IN} = 210 MHz	+25°C		73.9/75.4 typical		
		f_{IN} = 300 MHz	+25°C		73.1/74.4 typical		
Effective number of bits	ENOB	f_{IN} = 5 MHz	+25°C	01	12.1/12.4 typical		dBFS
		f_{IN} = 97 MHz	+25°C		12.1/12.3 typical		
		f_{IN} = 140 MHz	+25°C		12.1/12.3 typical		
		f_{IN} = 170 MHz	+25°C		12.0/12.3 typical		
			-55°C to +125°C		11.5		
		f_{IN} = 210 MHz	+25°C		12.0/12.2 typical		
		f_{IN} = 300 MHz	+25°C		11.9/12.1 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC specification section – continued.							
Spurious free dynamic range (including second and third harmonic distortion	SFDR	f_{IN} = 5 MHz	+25°C	01	98/97 typical		dBFS
		f_{IN} = 97 MHz	+25°C		95/93 typical		
		f_{IN} = 140 MHz	+25°C		94/95 typical		
		f_{IN} = 170 MHz	+25°C		93/92 typical		
					82		
			-55°C to +125°C		82		
		f_{IN} = 210 MHz	+25°C		93/92 typical		
		f_{IN} = 300 MHz	+25°C		93/90 typical		
		f_{IN} = 5 MHz at -2 dB full scale	+25°C		100/100 typical		
		f_{IN} = 97 MHz at -2 dB full scale	+25°C		97/97 typical		
		f_{IN} = 140 MHz at -2 dB full scale	+25°C		100/95 typical		
		f_{IN} = 170 MHz at -2 dB full scale	+25°C		100/100 typical		
		f_{IN} = 210 MHz at -2 dB full scale	+25°C		93/93 typical		
		f_{IN} = 300 MHz at -2 dB full scale	+25°C		90/90 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC specification section – continued.							
Worst other (excluding second and third harmonic distortion	SFDR	f_{IN} = 5 MHz	+25°C	01	98/97 typical		dBFS
		f_{IN} = 97 MHz	+25°C		97/93 typical		
		f_{IN} = 140 MHz	+25°C		97/95 typical		
		f_{IN} = 170 MHz	+25°C		97/93 typical		
					88		
			-55°C to +125°C		82		
		f_{IN} = 210 MHz	+25°C		97/95 typical		
		f_{IN} = 300 MHz	+25°C		97/95 typical		
Two tone intermodulation distortion	IMD	AIN1 and AIN2 = -7.0 dBFS at 2.5 V p-p FS, f_{IN1} = 70 MHz, f_{IN2} = 72 MHz	+25°C	01	97 typical		dBFS
		AIN1 and AIN2 = -7.0 dBFS at 2.5 V p-p FS, f_{IN1} = 170 MHz, f_{IN2} = 172 MHz			91 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital specification section							
Clock inputs (CLK+, CLK-)							
Logic compliance				01	CMOS/LVDS/ LVPECL		
Differential input 4/ voltage			-55°C to +125°C	01	250		mVp-p
Input common mode voltage			-55°C to +125°C	01	0.8 typical		V
Input resistance (differential)			+25°C	01	20 typical		kΩ
Input capacitance			+25°C	01	2.5 typical		pF
Logic inputs (SCLK, CSB, SDIO)							
Logic 1 voltage			-55°C to +125°C	01	1.2	3.6	V
Logic 0 voltage			-55°C to +125°C	01		0.3	V
Input resistance			+25°C	01	30 typical		kΩ
Input capacitance			+25°C	01	0.5 typical		pF
Logic output (SDIO) 5/							
Logic 1 voltage		I_{OH} = 800 μA	-55°C to +125°C	01	1.7/3.1 typical		V
Logic 0 voltage		I_{OL} = 50 μA	-55°C to +125°C	01		0.3	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital specification section – continued.							
Digital outputs (D0+ to D15, D0- to D15-, DCO + DCO-, OR+, OR-)							
Logic compliance				01	LVDS		
Differential output voltage	V_{OD}		-55°C to +125°C	01	247	545	mV
Output offset voltage	V_{OS}		-55°C to +125°C	01	1.125	1.375	V
Output coding (default)				01	Offset binary		
Switching specifications section							
Clock 6/							
Clock rate			-55°C to +125°C	01	50	250	MSPS
Clock pulse width high	t_{CH}		+25°C	01	2 typical		ns
Clock pulse width low	t_{CL}		+25°C	01	2 typical		ns
Output parameters. 6/ 7/							
Propagation delay	t_{PD}		+25°C	01	3 typical		ns
Rise time	t_R	20% to 80%	+25°C	01	200 typical		ps
Fall time	t_F	20% to 80%	+25°C	01	200 typical		ps
DCO propagation delay	t_{CPD}		+25°C	01	3 typical		ns
DCO to data delay	t_{SKEW}		-55°C to +125°C	01	-200	+200	ps
Wake up time (power down)			-55°C to +125°C	01	100 typical		ms
Pipeline latency			-55°C to +125°C	01	16 typical		Clock cycles

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching specifications section - continued.							
Aperture							
Aperture delay	t_A		+25°C	01	1.2 typical		ns
Aperture uncertainty (jitter)			+25°C	01	60 typical		fs rms
Out of range recovery time			+25°C	01	1 typical		Clock cycles

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 Vp-p differential input, 1.25 V internal reference, AIN = -1.0 dBFS, DCS on, default SPI settings.

3/ Measured with a low input frequency, full scale sine wave, with approximately 5 pF loading on each output bit.

4/ This is specified for LVDS and LVPECL only.

5/ This depends on if SPIVDD is tied to a 1.8 V or 3.3 V supply.

6/ Can be adjusted via the SPI interface.

7/ Measurements were made using a part soldered to FR-4 material.

Case X

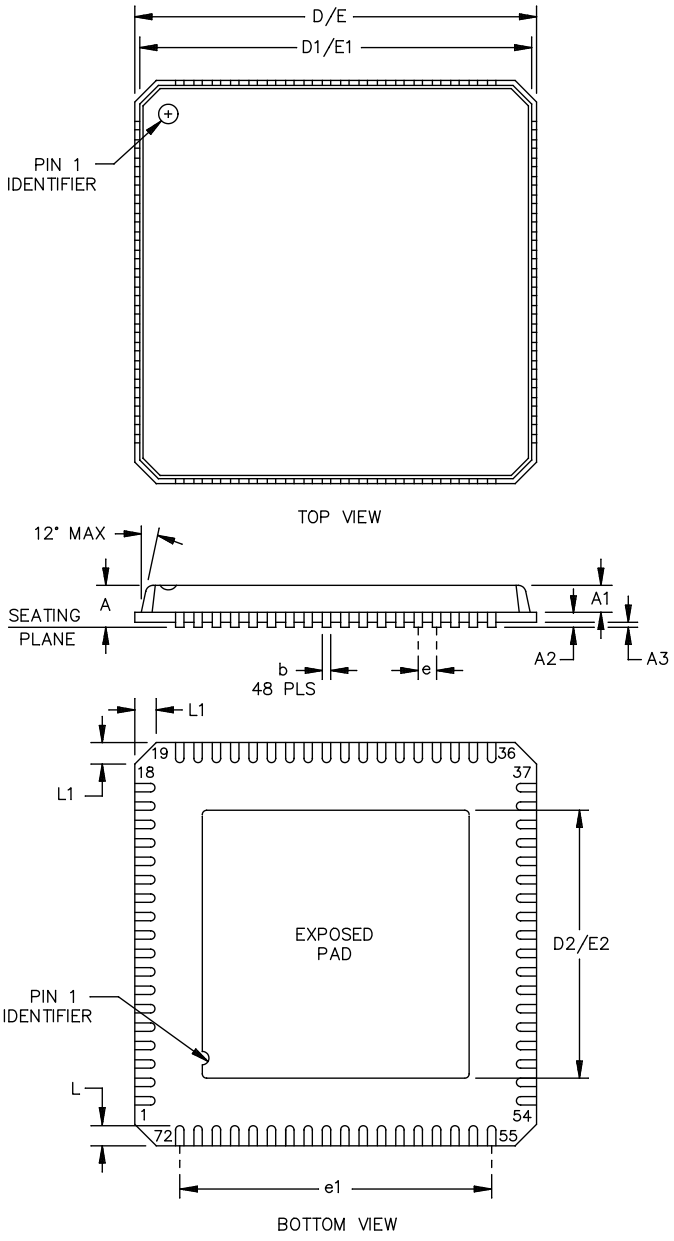

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/16611
		REV A	PAGE 14

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Max
A	.031	.033	.035	0.80	0.85	0.90
A1	.023	.025	.027	0.60	0.65	0.70
A2		.007 REF			0.20 REF	
A3	---	.0004	.002	---	0.01	0.05
b	.007	.009	.011	0.18	0.23	0.30
D/E	.389	.393 SQ	.397	9.90	10.00 SQ	10.10
D1/E1	.379	.383 SQ	.387	9.65	9.75 SQ	9.85
D2/E2	.330	.334	.338	8.40	8.50 SQ	8.60
e		.019 BSC			0.50 BSC	
e1		.344 BSC			8.50 BSC	
L	.011	.015	.019	0.30	0.40	0.50
L1	.009	.016	.023	0.24	0.42	0.60

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of manufacturer's data sheet.
3. Falls within reference to JEDEC MO-220-VNND-4.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal numbers	Terminal symbol	Description
0	EPAD	Exposed paddle. The exposed paddle must be connected to AGND.
10, 14, 16, 41, 43, 45	AGND	Analog ground.
1, 2, 3, 4, 7, 8, 9, 11, 12, 13, 15, 46, 52, 53, 54, 55, 56, 58, 59, 60, 61, 62, 63, 70, 71, 72	AVDD1	1.8 V analog supply.
64, 65, 68, 69	AVDD2	3.3 V analog supply.
42, 44	AVDD3	1.8 V analog supply.
51	SPIVDD	1.8 V or 3.3 V SPI supply.
17, 38	DRGND	Digital output driver ground.
18, 37	DRVDD	1.8 V digital output driver supply.
67	VIN-	Analog input complement.
66	VIN+	Analog input true.
6	CLK-	Clock input complement.
5	CLK+	Clock input true.
19	D1-/D0-	D1 and D0 (LSB) digital output complement.
20	D1+/DO+	D1 and D0 (LSB) digital output true.
21	D3-/D2-	D3 and D2 digital output complement.
22	D3+/D2+	D3 and D2 digital output true.
23	D5-/D4-	D5 and D4 digital output complement.
24	D5+/D4+	D5 and D4 digital output true.
25	D7-/D6-	D7 and D6 digital output complement.
26	D7+/D6+	D7 and D6 digital output true.

FIGURE 2. Terminal connections.

Device type	01	
Case outline	X	
Terminal numbers	Terminal symbol	Description
29	D9-/D8-	D9 and D8 digital output complement.
30	D9+/D8+	D9 and D8 digital output true.
31	D11-/D10-	D11 and D10 digital output complement.
32	D11+/D10+	D11 and D10 digital output true.
33	D13-/D12-	D13 and D12 digital output complement.
34	D13+/D12+	D13 and D12 digital output true.
35	D15-/D14-	D15 and D14 digital output complement.
36	D15+/D14+	D15 and D14 digital output true.
27	DCO-	Data clock digital output complement.
28	DCO+	Data clock output true.
39	OR-	Output of range digital output complement.
40	OR+	Out of range digital output true.
47	DNC	Do not connect (leave pin floating).
48	SDIO	Serial data input/output.
49	SCLK	Serial clock.
50	CSB	Chip select bar.
57	XVREF	External VREF option.

FIGURE 2. Terminal connections - continued.

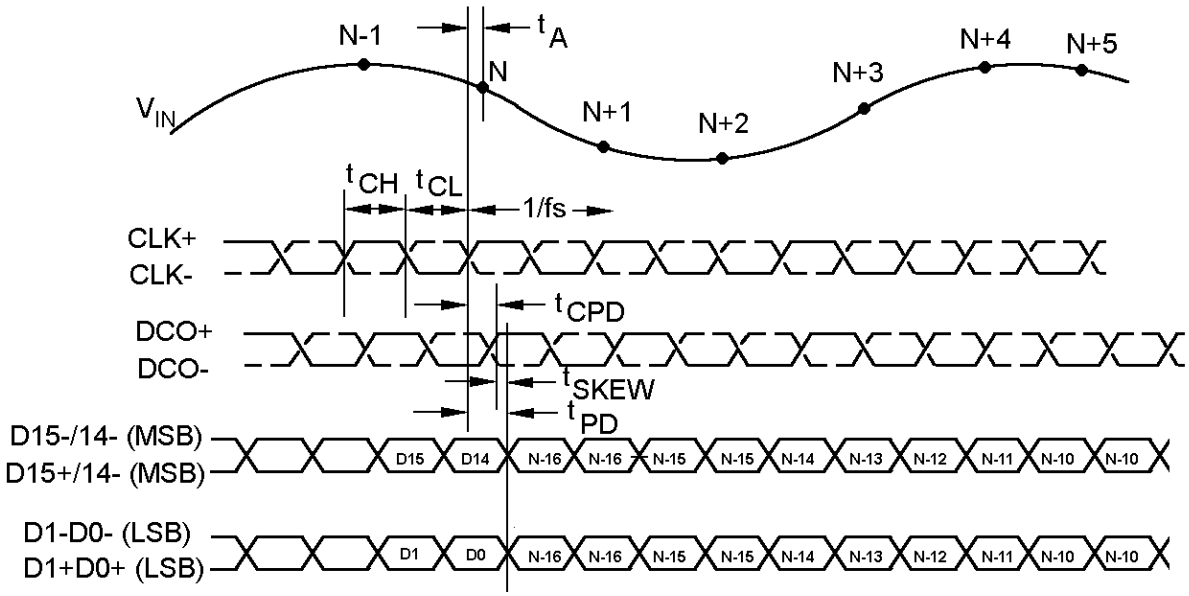

FIGURE 3. 16 bit output data timing waveform.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/16611-01XE	24355	Tray, 168 units	AD9467SCPZ-250-EP
		Reel, 400 units	AD9467SCPZ250EPRL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123