REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make correction to the vendor part number by deleting TPS51200-EP and replacing with TPS51200MDRCTEP as specified under paragraph 6.3. - ro	16-12-06	C. SAFFLE
B	Add JEDEC references to paragraphs 1.3 and 2. Add Top side marking column to paragraph 6.3. Update document paragraphs to current requirements. - ro	22-05-04	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B									
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13									

PMIC N/A

Original date of drawing
YY-MM-DD
16-07-14

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TITLE
MICROCIRCUIT, LINEAR, SINK AND SOURCE DDR TERMINATION REGULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/16610
REV B		PAGE 1 OF 13

AMSC N/A

5962-V050-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance sink and source double data rate (DDR) termination regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16610	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS51200-EP	Sink and source DDR termination regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	10	See figure 1	Plastic quad leadless small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage (V_{IN}): 2/
- REFIN, VIN, VLDOIN, VOSNS ..... -0.3 V minimum, 3.6 V maximum
- EN ..... -0.3 V minimum, 6.5 V maximum
- PGND to GND ..... -0.3 V minimum, 0.3 V maximum

Output voltage (VOUT): 2/
- REFOUT, VO ..... -0.3 V minimum, 3.6 V maximum
- PGOOD ..... -0.3 V minimum, 6.5 V maximum

Operating junction temperature range (T_J) ..... -55°C to +150°C

Storage temperature range (T_{STG}) ..... -55°C to +150°C

Electrostatic discharge (ESD):
- Human body model (HBM), per JEDEC JS-001 ..... ±2000 V 3/
- Charged device model (CDM), per JEDEC JESD22-C101 ..... ±500 V 4/

1.4 Recommended operating conditions. 5/

Supply voltages (V_{IN}) ..... 2.375 V minimum, 3.500 V maximum

Voltage:
- EN, VLDOIN, VOSNS ..... -0.1 V minimum, 3.5 V maximum
- REFIN ..... 0.5 V minimum, 1.8 V maximum
- PGOOD, VO ..... -0.1 V minimum, 3.5 V maximum
- REFOUT ..... -0.1 V minimum, 1.8 V maximum
- PGND ..... -0.1 V minimum, 0.1 V maximum

Operating junction temperature range (T_J) ..... -55°C to +125°C

1.5 Thermal characteristics.

Thermal metric 6/	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	55.6	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	84.6	°C/W
Thermal resistance, junction-to-board	θ_{JB}	30.0	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	5.5	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	30.1	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	10.9	°C/W

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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Unless otherwise specified, all voltages are with respect to the network ground terminal.
3/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
4/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
6/ Contact manufacturer for more information about traditional and new thermal metrics.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Supply current							
Supply current	I_{IN}	V_{EN} = 3.3 V, no load	25°C	01		1	mA
					0.7 typical		
Shutdown current	$I_{IN(SDN)}$	V_{EN} = 0 V, V_{REFIN} = 0 V, no load	25°C	01		80	µA
					65 typical		
		V_{EN} = 0 V, V_{REFIN} > 0.4 V, no load				400	
					200 typical		
Supply current of VLDOIN	I_{LDOIN}	V_{EN} = 3.3 V, no load	25°C	01		50	µA
					1 typical		
Shutdown current of VLDOIN	$I_{LDOIN(SDN)}$	V_{EN} = 0 V, no load	25°C	01		50	µA
					0.1 typical		
Input current							
Input current, REFIN	I_{REFIN}	V_{EN} = 3.3 V	-55°C to +125°C	01		1	µA
VO output							
Output dc voltage, VO	V_{VOSNS}	V_{REFOUT} = 1.25 V (DDR1), I_O = 0 A	-55°C to +125°C	01	-15	15	V
			25°C		1.25 typical		mV
		V_{REFOUT} = 0.9 V (DDR2), I_O = 0 A	-55°C to +125°C		-15	15	V
			25°C		0.9 typical		mV
		V_{REFOUT} = 0.75 V (DDR3), V_{LDOIN} = 1.5 V, I_O = 0 A	-55°C to +125°C		-15	15	V
			25°C		0.75 typical		mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
VO output – continued.							
Output voltage tolerance to REFOUT	V_{VOTOL}	-2 A < I_{VO} < 2 A	-55°C to +125°C	01	-25	25	mV
VO source current limit	I_{VOSRCL}	With reference to REFOUT, V_{OSNS} = 90% x V_{REFOUT}	-55°C to +125°C	01	3	4.5	A
VO sink current limit	I_{VOSNCL}	With reference to REFOUT, V_{OSNS} = 110% x V_{REFOUT}	-55°C to +125°C	01	3.5	5.5	A
Discharge current, VO	I_{DSCHRG}	V_{REFIN} = V, V_{VO} = 0.3 V, V_{EN} = 0 V	25°C	01		25	Ω
					18 typical		
Powergood comparator							
VO PGOOD threshold	$V_{TH(PG)}$	PGOOD window lower threshold with respect to REFOUT	-55°C to +125°C	01	-23.5	-17.5	%
			25°C		-20 typical		
		PGOOD window upper threshold with respect to REFOUT	-55°C to +125°C		17.5	23.5	
			25°C		20 typical		
		PGOOD hysteresis	25°C		5 typical		
PGOOD start up delay	$t_{PGSTUPDLY}$	Start up rising edge, VOSNS within 15% of REFOUT	25°C	01	2 typical		ms
Output low voltage	$V_{PGOODLOW}$	I_{SINK} = 4 mA	-55°C to +125°C	01		0.4	V
PGOOD bad delay	$t_{PBADDLY}$	VOSNS is outside of the ±20% PGOOD window	25°C	01	10 typical		µs
Leakage current 3/	$I_{PGOODLK}$	V_{OSNS} = V_{REFIN} (PGOOD high impedance), V_{PGOOD} = V_{VIN} + 0.2 V	-55°C to +125°C	01		1	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
REFIN and REFOUT							
REFIN voltage range	V_{REFIN}		-55°C to +125°C	01	0.5	1.8	V
REFIN undervoltage lockout	$V_{REFINUVLO}$	REFIN rising	-55°C to +125°C	01	360	420	mV
			25°C		390 typical		
REFIN undervoltage lockout hysteresis	$V_{REFINUVHYS}$		25°C	01	20 typical		mV
REFOUT voltage	V_{REFOUT}		25°C	01	REFIN typical		V
REFOUT voltage tolerance to V_{REFIN}	$V_{REFOUTTOL}$	-10 mA < I_{REFOUT} < 10 mA, V_{REFIN} = 1.25 V	-55°C to +125°C	01	-15	15	mV
		-10 mA < I_{REFOUT} < 10 mA, V_{REFIN} = 0.9 V			-15	15	
		-10 mA < I_{REFOUT} < 10 mA, V_{REFIN} = 0.75 V			-15	15	
		-10 mA < I_{REFOUT} < 10 mA, V_{REFIN} = 0.6 V			-15	15	
REFOUT source current limit	$I_{REFOUTSRCL}$	V_{REFOUT} = 0 V	-55°C to +125°C	01	10		mA
			25°C		40 typical		
REFOUT sink current limit	$I_{REFOUTSNCL}$	V_{REFOUT} = 0 V	-55°C to +125°C	01	10		mA
			25°C		40 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
UVLO and EN logic threshold.							
UVLO threshold	$V_{VINUVVIN}$	Wake up	25°C	01	2.2	2.375	V
					2.3 typical		
		Hysteresis			50 typical		mV
High level input voltage	V_{ENIH}	Enable	-55°C to +125°C	01	1.7		V
Low level input voltage	V_{ENIL}	Enable	-55°C to +125°C	01		0.3	V
Hysteresis voltage	V_{ENYST}	Enable	25°C	01	0.5 typical		V
Logic input leakage current	I_{ENLEAK}	EN	25°C	01	-1	1	µA
Thermal shutdown							
Thermal shutdown threshold	T_{SON}	Shutdown temperature	25°C	01	150 typical		°C
		Hysteresis			25 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{VIN} = 3.3 V, V_{VLDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{VOSNS} = 0.9 V, V_{EN} = V_{VIN}, C_{OUT} = 3 x 10 µF and figure 3.

3/ Ensured by design. Not production tested.

Case X

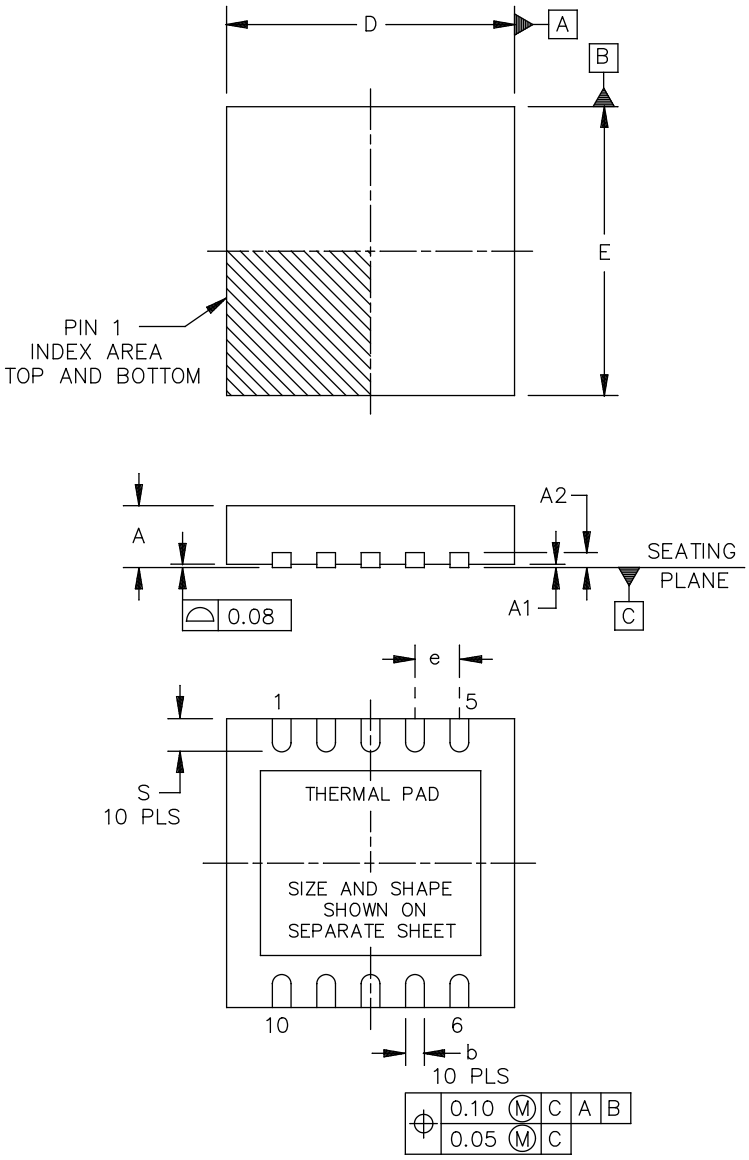

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/16610
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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.031	.039	0.80	1.00
A1	.000	.002	0.00	0.05
A2	.008 REF		0.20 REF	
b	.007	.012	0.18	0.30
D	.114	.122	2.90	3.10
E	.114	.122	2.90	3.10
e	.020 BSC		0.50 BSC	
s	.012	.020	0.30	0.50

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present
3. See the additional figure in the manufacturer's datasheet for details regarding the exposed thermal pad features and dimensions, if present.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O SEE NOTE 1	Description
1	REFIN	I	Reference input.
2	VLDOIN	I	Supply voltage for the LDO.
3	VO	O	Power output for the LDO.
4	PGND SEE NOTE 2	G	Power ground output for the LDO.
5	VOSNS	I	Voltage sense input for the LDO. Connect to positive terminal of the output capacitor or the load.
6	REFOUT	O	Reference output. Connect to GND through 0.1 μF ceramic capacitor.
7	EN	I	For DDT VTT application, connect EN to SLP_S3. For any other application, use the EN pin as the ON/OFF function.
8	GND	G	Signal ground. Connect to negative terminal of the output capacitor.
9	PGOOD	O	PGOOD output. Indicates regulation.
10	VIN	I	2.5 V or 3.3 V power supply. A ceramic decoupling capacitor with a value between 1 μF and 4.7 μF is required.

NOTES:
1. I = Input, O = Output, and G = Ground.
2. Thermal pad connection.

FIGURE 2. Terminal connections.

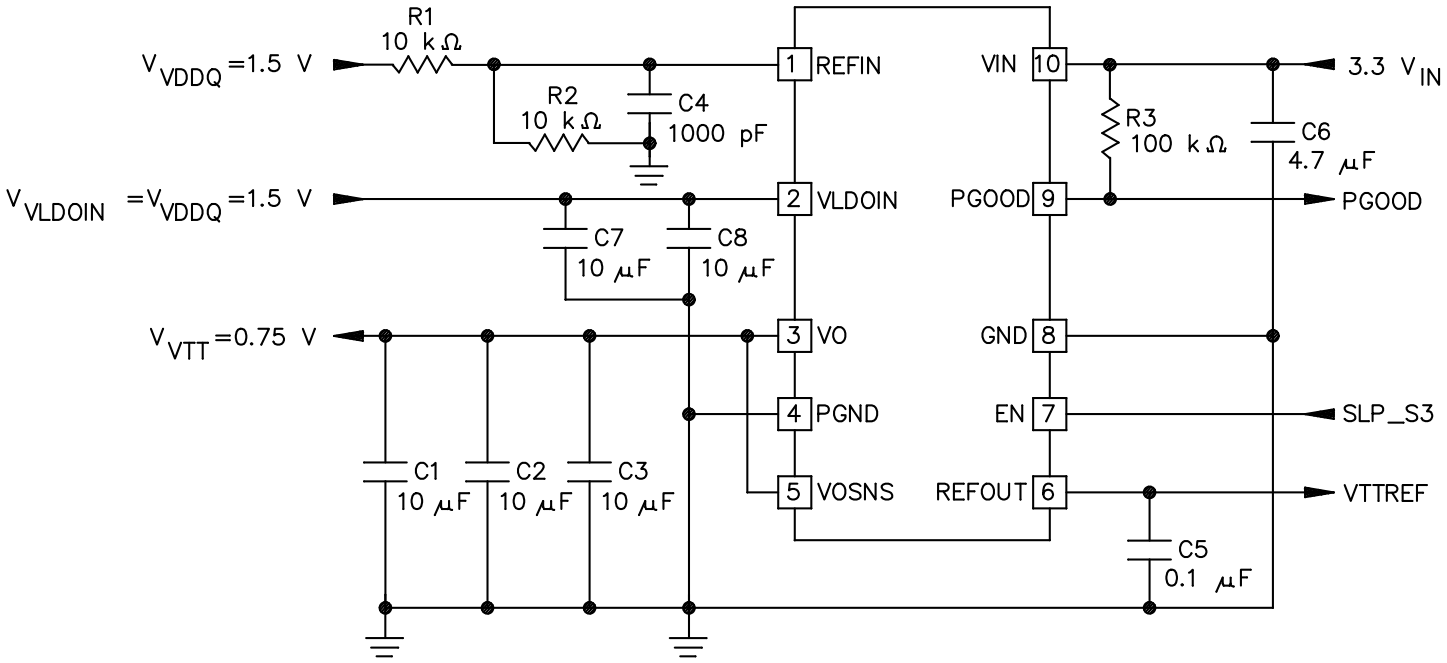

FIGURE 3. 3.3 V VIN, DDR3 configuration.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number 2/
V62/16610-01XE	01295	1200M	TPS51200MDRCTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For all available packages, see the orderable addendum at the end of the manufacturer's data sheet.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243