REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Under Table I, 36 V single supply, Dynamics characteristics section, Source and drain capacitance test, delete V_S = 6 V and replace with V_S = 18 V. Update document paragraphs to current requirements. - ro	21-06-16	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A					
PAGE	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33					
REV STATUS OF PAGES	**REV**					A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	PAGE					1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 16-04-06	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, HIGH VOLTAGE, LATCH UP PROOF, 4-/8- CHANNEL CMOS MULTIPLEXERS, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/16607**
	REV **A**	**PAGE** 1 **OF** 33

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high voltage, latch-up proof, 4-/8- channel CMOS multiplexers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16607	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG5408-EP	High voltage, latch-up proof, 4-/8 channel CMOS multiplexers
02	ADG5409-EP	High voltage, latch-up proof, 4-/8 channel CMOS multiplexers

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-220-WGGC	Quad flat pack thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Positive power supply voltage (V_{DD}) to Negative power supply voltage (V_{SS})	48 V
V_{DD} to Ground (GND)	-0.3 V to +48 V
V_{SS} to GND	+0.3 V to -48 V
Analog inputs	V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first 2/
Digital inputs	V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first 2/
Peak current, Sx, D, or Dx pins:	
Device type 01	435 mA (pulsed at 1 ms, 10% duty cycle maximum)
Device type 02	300 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous current, Sx, D, or Dx pins	Data + 15% 3/
Temperature range operating	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Junction temperature	150°C
Thermal impedance, (θ_{JA})	30.4°C/W
Reflow soldering peak temperature, lead (Pb) free	As per JEDEC J-STD 020

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC J STD-020 - Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices
JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Over voltages at the Ax, EN, Sx, D, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
3/ See table I in Continuous current, Sx or D section.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 On resistance. The On resistance shall be as shown in figure 5.

3.5.6 Off leakage. The Off leakage shall be as shown in figure 6.

3.5.7 On leakage. The On leakage shall be as shown in figure 7.

3.5.8 Address to output switching times. The address to output switching times shall be as shown in figure 8.

3.5.9 Enable delay, t_{ON}(EN), t_{OFF}(EN). The enable delay, t_{ON}(EN), t_{OFF}(EN) shall be as shown in figure 9.

3.5.10 Break before make time delay, t_D. The Break before make time delay, t_D shall be as shown in figure 10.

3.5.11 Charge injection. The charge injection shall be as shown in figure 11.

3.5.12 Off isolation. The Off isolation shall be as shown in figure 12.

3.5.13 Channel to channel crosstalk. The channel crosstalk shall be as shown in figure 13.

3.5.14 THD + noise. The THD + noise shall be as shown in figure 14.

3.5.15 Bandwidth. The bandwidth shall be as shown in figure 15.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{DD} = +15 V ±10%, V_{SS} = -15 V ±10%, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
±15 V dual supply							
Analog switch.							
Analog signal range			-55°C to +125°C	01, 02	V_{DD} to V_{SS}		V
On resistance	R_{ON}	V_S = ±10 V, I_S = -10 mA, see figure 5	+25°C	01, 02	13.5 typical		Ω
		V_{DD} = +13.5 V, V_{SS} = -13.5 V	+25°C			15	
			-40°C to +85°C			18	
			-55°C to +125°C			22	
On resistance match between channels	ΔR_{ON}	V_S = ±10 V, I_S = -10 mA	+25°C	01, 02	0.3 typical		Ω
			+25°C			0.8	
			-40°C to +85°C			1.3	
			-55°C to +125°C			1.4	
On resistance flatness	$\Delta R_{FLAT(ON)}$	V_S = ±10 V, I_S = -10 mA	+25°C	01, 02	1.8 typical		Ω
			+25°C			2.2	
			-40°C to +85°C			2.6	
			-55°C to +125°C			3	
Leakage currents.		V_{DD} = +16.5 V, V_{SS} = -16.5 V					
Source off leakage	I_S (off)	V_S = ±10 V, V_D = ∓10 V, see figure 6	+25°C	01, 02	±0.05 typical		nA
			+25°C			±0.25	
			-40°C to +85°C			±1	
			-55°C to +125°C			±7	
Drain off leakage	I_D (off)	V_S = ±10 V, V_D = ∓10 V, see figure 6	+25°C	01, 02	±0.1 typical		nA
			+25°C			±0.4	
			-40°C to +85°C			±4	
			-55°C to +125°C			±30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = +15 V ±10%, V_{SS} = -15 V ±10%, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
±15 V dual supply – continued.							
Leakage currents – continued.		V_{DD} = +16.5 V, V_{SS} = -16.5 V					
Channel on leakage	I_D (on), I_S(on)	V_S = V_D = ±10 V, see figure 7	+25°C	01, 02	±0.1 typical		nA
			+25°C			±0.4	
			-40°C to +85°C			±4	
			-55°C to +125°C			±30	
Digital inputs.							
Input high voltage	V_{INH}		-55°C to +125°C	01, 02	2.0		V
Input low voltage	V_{INL}		-55°C to +125°C	01, 02		0.8	V
Input current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}	+25°C	01, 02	0.002 typical		µA
			-55°C to +125°C			±0.1	
Digital input capacitance	C_{IN}		+25°C	01, 02	3 typical		pF
Dynamic characteristics. 2/							
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see figure 8	+25°C	01, 02	170 typical		ns
			+25°C			217	
			-40°C to +85°C			258	
			-55°C to +125°C			292	
Enable delay on	$t_{ON(EN)}$	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see figure 9	+25°C	01, 02	140 typical		ns
			+25°C			175	
			-40°C to +85°C			213	
			-55°C to +125°C			242	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = +15 V ±10%, V_{SS} = -15 V ±10%, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
±15 V dual supply – continued.							
Dynamic characteristics – continued. 2/							
Enable delay off	$t_{OFF(EN)}$	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see figure 9	+25°C	01, 02	130 typical		ns
			+25°C			161	
			-40°C to +85°C			183	
			-55°C to +125°C			198	
Break before make time delay	t_D	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 10 V, see figure 10	+25°C	01, 02	50 typical		ns
			-55°C to +125°C		13		
Charge injection	O_{INJ}	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see figure 11	+25°C	01, 02	115 typical		pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 12	+25°C	01, 02	-60 typical		dB
Channel to channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 13	+25°C	01, 02	-60 typical		dB
Total harmonic distortion + noise		R_L = 50 Ω, 15 V_{PP}, see figure 14, f = 20 Hz to 20 kHz	+25°C	01, 02	0.01 typical		%
-3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF, see figure 15	+25°C	01	50 typical		MHz
				02	87 typical		
Insertion loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 15	+25°C	01, 02	0.9 typical		dB
Source capacitance	$C_{S(off)}$	V_S = 0 V, f = 1 MHz	+25°C	01, 02	15 typical		pF
Drain capacitance	$C_{D(off)}$	V_S = 0 V, f = 1 MHz	+25°C	01	102 typical		pF
				02	50 typical		
Source and drain capacitance	$C_{S(on)}$, $C_{D(on)}$	V_S = 0 V, f = 1 MHz	+25°C	01	133 typical		pF
				02	81 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = +15 V ±10%, V_{SS} = -15 V ±10%, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
±15 V dual supply – continued.							
Power requirements.		V_{DD} = +16.5 V, V_{SS} = -16.5 V					
Positive power supply current	I_{DD}	Digital inputs = 0 V or V_{DD}	+25°C	01, 02	45 typical		µA
			+25°C			55	
			-55°C to +125°C			80	
Negative power supply current	I_{SS}	Digital inputs = 0 V or V_{DD}	+25°C	01, 02	0.001 typical		µA
			-55°C to +125°C			1	
Positive power supply voltage	V_{DD}	GND = 0 V	-55°C to +125°C	01, 02	±9		V
Negative power supply voltage	V_{SS}	GND = 0 V	-55°C to +125°C	01, 02		±22	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = +20 V ±10%, V_{SS} = -20 V ±10%, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
±20 V dual supply.							
Analog switch.							
Analog signal range			-55°C to +125°C	01, 02	V_{DD} to V_{SS}		V
On resistance	R_{ON}	V_S = ±15 V, I_S = -10 mA, see figure 5	+25°C	01, 02	12.5 typical		Ω
		V_{DD} = +18 V, V_{SS} = -18 V	+25°C			14	
			-40°C to +85°C			17	
			-55°C to +125°C			21	
On resistance match between channels	ΔR_{ON}	V_S = ±15 V, I_S = -10 mA	+25°C	01, 02	0.3 typical		Ω
			+25°C			0.8	
			-40°C to +85°C			1.3	
			-55°C to +125°C			1.4	
On resistance flatness	$\Delta R_{FLAT(ON)}$	V_S = ±15 V, I_S = -10 mA	+25°C	01, 02	2.3 typical		Ω
			+25°C			2.7	
			-40°C to +85°C			3.1	
			-55°C to +125°C			3.5	
Leakage currents.		V_{DD} = +22 V, V_{SS} = -22 V					
Source off leakage	I_S (off)	V_S = ±15 V, V_D = ∓15 V, see figure 6	+25°C	01, 02	±0.1 typical		nA
			+25°C			±0.25	
			-40°C to +85°C			±1	
			-55°C to +125°C			±7	
Drain off leakage	I_D (off)	V_S = ±15 V, V_D = ∓15 V, see figure 6	+25°C	01, 02	±0.15 typical		nA
			+25°C			±0.4	
			-40°C to +85°C			±4	
			-55°C to +125°C			±30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = +20 V ±10%, V_{SS} = -20 V ±10%, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
±20 V dual supply – continued.							
Leakage currents – continued.		V_{DD} = +22 V, V_{SS} = -22 V					
Channel on leakage	I_D (on), I_S(on)	V_S = V_D = ±15 V, see figure 7	+25°C	01, 02	±0.15 typical		nA
			+25°C			±0.4	
			-40°C to +85°C			±4	
			-55°C to +125°C			±30	
Digital inputs							
Input high voltage	V_{INH}		-55°C to +125°C	01, 02	2.0		V
Input low voltage	V_{INL}		-55°C to +125°C	01, 02		0.8	V
Input current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}	+25°C	01, 02	0.002 typical		µA
			-55°C to +125°C			±0.1	
Digital input capacitance	C_{IN}		+25°C	01, 02	3 typical		pF
Dynamic characteristics. 2/							
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see figure 8	+25°C	01, 02	160 typical		ns
			+25°C			207	
			-40°C to +85°C			237	
			-55°C to +125°C			262	
Enable delay on	$t_{ON(EN)}$	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see figure 9	+25°C	01, 02	140 typical		ns
			+25°C			165	
			-40°C to +85°C			194	
			-55°C to +125°C			218	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = +20 V ±10%, V_{SS} = -20 V ±10%, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
±20 V dual supply – continued.							
Dynamic characteristics – continued. 2/							
Enable delay off	$t_{OFF(EN)}$	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see figure 9	+25°C	01, 02	133 typical		ns
			+25°C			153	
			-40°C to +85°C			174	
			-55°C to +125°C			189	
Break before make time delay	t_D	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 10 V, see figure 10	+25°C	01, 02	38 typical		ns
			-55°C to +125°C		8		
Charge injection	Q_{INJ}	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see figure 11	+25°C	01, 02	155 typical		pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 12	+25°C	01, 02	-60 typical		dB
Channel to channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 13	+25°C	01, 02	-60 typical		dB
Total harmonic distortion + noise		R_L = 1 kΩ, 20 V_{PP}, see figure 14, f = 20 Hz to 20 kHz	+25°C	01, 02	0.012 typical		%
-3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF, see figure 15	+25°C	01	50 typical		MHz
				02	88 typical		
Insertion loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 15	+25°C	01, 02	0.8 typical		dB
Source capacitance	$C_{S(off)}$	V_S = 0 V, f = 1 MHz	+25°C	01, 02	17 typical		pF
Drain capacitance	$C_{D(off)}$	V_S = 0 V, f = 1 MHz	+25°C	01	98 typical		pF
				02	48 typical		
Source and drain capacitance	$C_{S(on)}$, $C_{D(on)}$	V_S = 0 V, f = 1 MHz	+25°C	01	128 typical		pF
				02	80 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = +20 V ±10%, V_{SS} = -20 V ±10%, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
±20 V dual supply – continued.							
Power requirements.		V_{DD} = +22 V, V_{SS} = -22 V					
Positive power supply current	I_{DD}	Digital inputs = 0 V or V_{DD}	+25°C	01, 02	50 typical		µA
			+25°C			70	
			-55°C to +125°C			120	
Negative power supply current	I_{SS}	Digital inputs = 0 V or V_{DD}	+25°C	01, 02	0.001 typical		µA
			-55°C to +125°C			1	
Positive power supply voltage	V_{DD}	GND = 0 V	-55°C to +125°C	01, 02	±9		V
Negative power supply voltage	V_{SS}	GND = 0 V	-55°C to +125°C	01, 02		±22	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 12 V ±10%, V_{SS} = 0 V, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
12 V dual supply.							
Analog switch.							
Analog signal range			-55°C to +125°C	01, 02	0 V to V_{DD}		V
On resistance	R_{ON}	V_S = 0 V to 10 V, I_S = -10 mA, see figure 5	+25°C	01, 02	26 typical		Ω
		V_{DD} = 10.8 V, V_{SS} = 0 V	+25°C			30	
			-40°C to +85°C			36	
			-55°C to +125°C			42	
On resistance match between channels	ΔR_{ON}	V_S = 0 V to 10 V, I_S = -10 mA	+25°C	01, 02	0.3 typical		Ω
			+25°C			1	
			-40°C to +85°C			1.5	
			-55°C to +125°C			1.6	
On resistance flatness	$\Delta R_{FLAT(ON)}$	V_S = 0 V to 10 V, I_S = -10 mA	+25°C	01, 02	5.5 typical		Ω
			+25°C			6.5	
			-40°C to +85°C			8	
			-55°C to +125°C			12	
Leakage currents		V_{DD} = 13.2 V, V_{SS} = 0 V					
Source off leakage	I_S (off)	V_S = 1 V/10 V, V_D = 10 V/1 V, see figure 6	+25°C	01, 02	±0.02 typical		nA
			+25°C			±0.25	
			-40°C to +85°C			±1	
			-55°C to +125°C			±7	
Drain off leakage	I_D (off)	V_S = 1 V/10 V, V_D = 10 V/1 V, see figure 6	+25°C	01, 02	±0.05 typical		nA
			+25°C			±0.4	
			-40°C to +85°C			±4	
			-55°C to +125°C			±30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 12 V ±10%, V_{SS} = 0 V, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
12 V dual supply – continued.							
Leakage currents – continued.		V_{DD} = 13.2 V, V_{SS} = 0 V					
Channel on leakage	I_D (on), I_S(on)	V_S = V_D = 1 V/10 V, see figure 7	+25°C	01, 02	±0.05 typical		nA
			+25°C			±0.4	
			-40°C to +85°C			±4	
			-55°C to +125°C			±30	
Digital inputs							
Input high voltage	V_{INH}		-55°C to +125°C	01, 02	2.0		V
Input low voltage	V_{INL}		-55°C to +125°C	01, 02		0.8	V
Input current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}	+25°C	01, 02	0.002 typical		µA
			-55°C to +125°C			±0.1	
Digital input capacitance	C_{IN}		+25°C	01, 02	3 typical		pF
Dynamic characteristics. 2/							
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V, see figure 8	+25°C	01, 02	230 typical		ns
			+25°C			321	
			-40°C to +85°C			388	
			-55°C to +125°C			430	
Enable delay on	t_{ON}(EN)	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V, see figure 9	+25°C	01, 02	215 typical		ns
			+25°C			276	
			-40°C to +85°C			345	
			-55°C to +125°C			397	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 12 V ±10%, V_{SS} = 0 V, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
12 V dual supply – continued.							
Dynamic characteristics – continued. 2/							
Enable delay off	$t_{OFF(EN)}$	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V, see figure 9	+25°C	01, 02	134 typical		ns
			+25°C			161	
			-40°C to +85°C			187	
			-55°C to +125°C			209	
Break before make time delay	t_D	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 8 V, see figure 10	+25°C	01, 02	118 typical		ns
			-55°C to +125°C		44		
Charge injection	O_{INJ}	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see figure 11	+25°C	01, 02	45 typical		pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 12	+25°C	01, 02	-60 typical		dB
Channel to channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 13	+25°C	01, 02	-60 typical		dB
Total harmonic distortion + noise		R_L = 1 kΩ, 6 V_{PP}, see figure 14, f = 20 Hz to 20 kHz	+25°C	01, 02	0.1 typical		%
-3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF, see figure 15	+25°C	01	35 typical		MHz
				02	74 typical		
Insertion loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 15	+25°C	01, 02	-1.8 typical		dB
Source capacitance	$C_{S(off)}$	V_S = 6 V, f = 1 MHz	+25°C	01, 02	22 typical		pF
Drain capacitance	$C_{D(off)}$	V_S = 6 V, f = 1 MHz	+25°C	01	119 typical		pF
				02	59 typical		
Source and drain capacitance	$C_{S(on)}$, $C_{D(on)}$	V_S = 6 V, f = 1 MHz	+25°C	01	146 typical		pF
				02	86 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 12 V ±10%, V_{SS} = 0 V, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
12 V dual supply – continued.							
Power requirements.		V_{DD} = 13.2 V					
Positive power supply current	I_{DD}	Digital inputs = 0 V or V_{DD}	+25°C	01, 02	40 typical		µA
			+25°C			50	
			-55°C to +125°C			75	
Positive power supply voltage	V_{DD}	GND = 0 V, V_{SS} = 0 V	-55°C to +125°C	01, 02	9	40	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 36 V ±10%, V_{SS} = 0 V, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
36 V single supply.							
Analog switch.							
Analog signal range			-55°C to +125°C	01, 02	0 V to V_{DD}		V
On resistance	R_{ON}	V_S = 0 V to 30 V, I_S = -10 mA, see figure 5	+25°C	01, 02	14.5 typical		Ω
		V_{DD} = 32.4 V, V_{SS} = 0 V	+25°C			16	
			-40°C to +85°C			19	
			-55°C to +125°C			23	
On resistance match between channels	ΔR_{ON}	V_S = 0 V to 30 V, I_S = -10 mA	+25°C	01, 02	0.3 typical		Ω
			+25°C			0.8	
			-40°C to +85°C			1.3	
			-55°C to +125°C			1.4	
On resistance flatness	$\Delta R_{FLAT(ON)}$	V_S = 0 V to 30 V, I_S = -10 mA	+25°C	01, 02	3.5 typical		Ω
			+25°C			4.3	
			-40°C to +85°C			5.5	
			-55°C to +125°C			6.5	
Leakage currents.		V_{DD} = 39.6 V, V_{SS} = 0 V					
Source off leakage	I_S (off)	V_S = 1 V/30 V, V_D = 30 V/1 V, see figure 6	+25°C	01, 02	±0.01 typical		nA
			+25°C			±0.25	
			-40°C to +85°C			±1	
			-55°C to +125°C			±7	
Drain off leakage	I_D (off)	V_S = 1 V/30 V, V_D = 30 V/1 V, see figure 6	+25°C	01, 02	±0.15 typical		nA
			+25°C			±0.4	
			-40°C to +85°C			±4	
			-55°C to +125°C			±30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 36 V ±10%, V_{SS} = 0 V, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
36 V singe supply – continued.							
Leakage currents – continued.		V_{DD} = 39.6 V, V_{SS} = 0 V					
Channel on leakage	I_D (on), I_S(on)	V_S = V_D = 1 V/30 V, see figure 7	+25°C	01, 02	±0.15 typical		nA
			+25°C			±0.4	
			-40°C to +85°C			±4	
			-55°C to +125°C			±30	
Digital inputs.							
Input high voltage	V_{INH}		-55°C to +125°C	01, 02	2.0		V
Input low voltage	V_{INL}		-55°C to +125°C	01, 02		0.8	V
Input current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}	+25°C	01, 02	0.002 typical		µA
			-55°C to +125°C			±0.1	
Digital input capacitance	C_{IN}		+25°C	01, 02	3 typical		pF
Dynamic characteristics. 2/							
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V, see figure 8	+25°C	01, 02	187 typical		ns
			+25°C			242	
			-40°C to +85°C			257	
			-55°C to +125°C			281	
Enable delay on	t_{ON}(EN)	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V, see figure 9	+25°C	01, 02	160 typical		ns
			+25°C			195	
			-40°C to +85°C			219	
			-55°C to +125°C			237	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 36 V ±10%, V_{SS} = 0 V, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
36 V single supply – continued.							
Dynamic characteristics – continued. 2/							
Enable delay off	$t_{OFF(EN)}$	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V, see figure 9	+25°C	01, 02	147 typical		ns
			+25°C			184	
			-40°C to +85°C			184	
			-55°C to +125°C			190	
Break before make time delay	t_D	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 18 V, see figure 10	+25°C	01, 02	53 typical		ns
			-55°C to +125°C		14		
Charge injection	O_{INJ}	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF, see figure 11	+25°C	01, 02	150 typical		pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 12	+25°C	01, 02	-60 typical		dB
Channel to channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 13	+25°C	01, 02	-60 typical		dB
Total harmonic distortion + noise		R_L = 1 kΩ, 18 V_{PP}, see figure 14, f = 20 Hz to 20 kHz	+25°C	01, 02	0.4 typical		%
-3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF, see figure 15	+25°C	01	45 typical		MHz
				02	76 typical		
Insertion loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see figure 15	+25°C	01, 02	-1 typical		dB
Source capacitance	$C_{S(off)}$	V_S = 18 V, f = 1 MHz	+25°C	01, 02	18 typical		pF
Drain capacitance	$C_{D(off)}$	V_S = 18 V, f = 1 MHz	+25°C	01	120 typical		pF
				02	60 typical		
Source and drain capacitance	$C_{S(on)}$, $C_{D(on)}$	V_S = 18 V, f = 1 MHz	+25°C	01	137 typical		pF
				02	80 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 36 V ±10%, V_{SS} = 0 V, GND = 0 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
36 V single supply – continued.							
Power requirements.		V_{DD} = 39.6 V					
Positive power supply current	I_{DD}	Digital inputs = 0 V or V_{DD}	+25°C	01, 02	80 typical		µA
			+25°C			100	
			-55°C to +125°C			155	
Positive power supply voltage	V_{DD}	GND = 0 V, V_{SS} = 0 V	-55°C to +125°C	01, 02	9	40	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Continuous current, Sx or D with θ_{JA} = 30.4°C/W		V_{DD} = +15 V, V_{SS} = -15 V	25°C	01		207	mA
			85°C			113	
			125°C			60	
		V_{DD} = +20 V, V_{SS} = -20 V	25°C			218	
			85°C			117	
			125°C			61	
		V_{DD} = 12 V, V_{SS} = 0 V	25°C			168	
			85°C			99	
			125°C			57	
		V_{DD} = 36 V, V_{SS} = 0 V	25°C			214	
			85°C			116	
			125°C			61	
		V_{DD} = +15 V, V_{SS} = -15 V	25°C	02		156	
			85°C			95	
			125°C			55	
		V_{DD} = +20 V, V_{SS} = -20 V	25°C			165	
			85°C			98	
			125°C			56	
		V_{DD} = 12 V, V_{SS} = 0 V	25°C			126	
			85°C			81	
			125°C			50	
		V_{DD} = 36 V, V_{SS} = 0 V	25°C			161	
			85°C			97	
			125°C			56	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Guaranteed by design, not subject to production test.

Case X

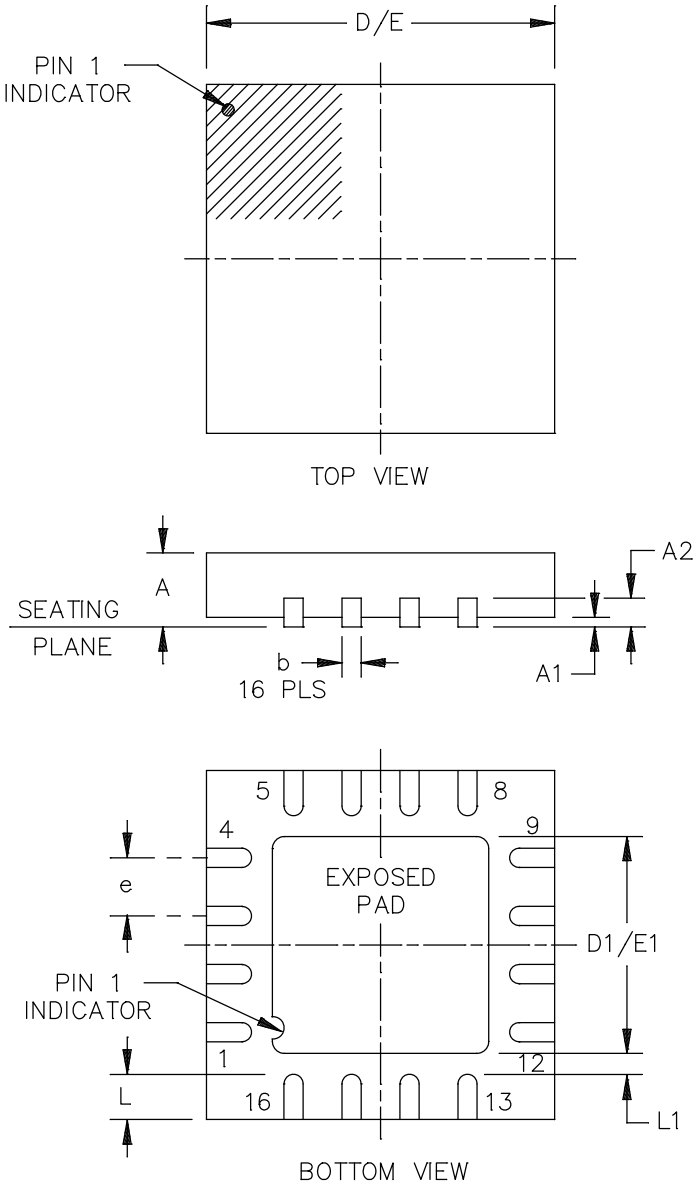

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/16607
		REV A	PAGE 22

Case X – continued.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.027	.029	.031	0.70	0.75	0.80
A1	.0007 NOM	---	.002	0.02 NOM	---	0.05
A2	.007 REF			0.20 REF		
b	.009	.011	.013	0.25	0.30	0.35
D/E	.153	.157	.161	3.90	4.00	4.10
D1/E1	.098	.102	.106	2.50	2.60	2.70
e	.025 BSC			0.65 BSC		
L	.013	.015	.017	0.35	0.40	0.45
L1	.007	---	---	0.20	---	---

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
3. Falls within reference to JEDEC MO-220-WGGC.

FIGURE 1. Case outlines - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{SS}	Most negative power supply potential. In single supply applications, this pin can be connected to ground.
2	S1	Source terminal 1. This pin can be an input or an output.
3	S2	Source terminal 2. This pin can be an input or an output.
4	S3	Source terminal 3. This pin can be an input or an output.
5	S4	Source terminal 4. This pin can be an input or an output.
6	D	Drain terminal. This pin can be an input or an output.
7	S8	Source terminal 8. This pin can be an input or an output.
8	S7	Source terminal 7. This pin can be an input or an output.
9	S6	Source terminal 6. This pin can be an input or an output.
10	S5	Source terminal 5. This pin can be an input or an output.
11	V_{DD}	Most positive power supply potential.
12	GND	Ground (0 V) reference.
13	A2	Logic control input.
14	A1	Logic control input.
15	A0	Logic control input.
16	EN	Active high digital input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
	EXPOSED PAD	The exposed pad is connected internally, for increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

FIGURE 2. Terminal connections.

Device type	02	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{SS}	Most negative power supply potential. In single supply applications, this pin can be connected to ground.
2	S1A	Source terminal 1A. This pin can be an input or an output.
3	S2A	Source terminal 2A. This pin can be an input or an output.
4	S3A	Source terminal 3A. This pin can be an input or an output.
5	S4A	Source terminal 4A. This pin can be an input or an output.
6	DA	Drain terminal A. This pin can be an input or an output.
7	DB	Drain terminal A. This pin can be an input or an output.
8	S4B	Source terminal 4B. This pin can be an input or an output.
9	S3B	Source terminal 3B. This pin can be an input or an output.
10	S3B	Source terminal 2B. This pin can be an input or an output.
11	S1B	Source terminal 1B. This pin can be an input or an output.
12	V_{DD}	Most positive power supply potential.
13	GND	Ground (0 V) reference.
14	A1	Logic control input.
15	A0	Logic control input.
16	EN	Active high digital input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
	EXPOSED PAD	The exposed pad is connected internally, for increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

FIGURE 2. Terminal connections - continued.

Device type 01

A2	A1	A0	EN	On switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Device type 02

A1	A0	EN	On switch pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

FIGURE 3. Truth tables.

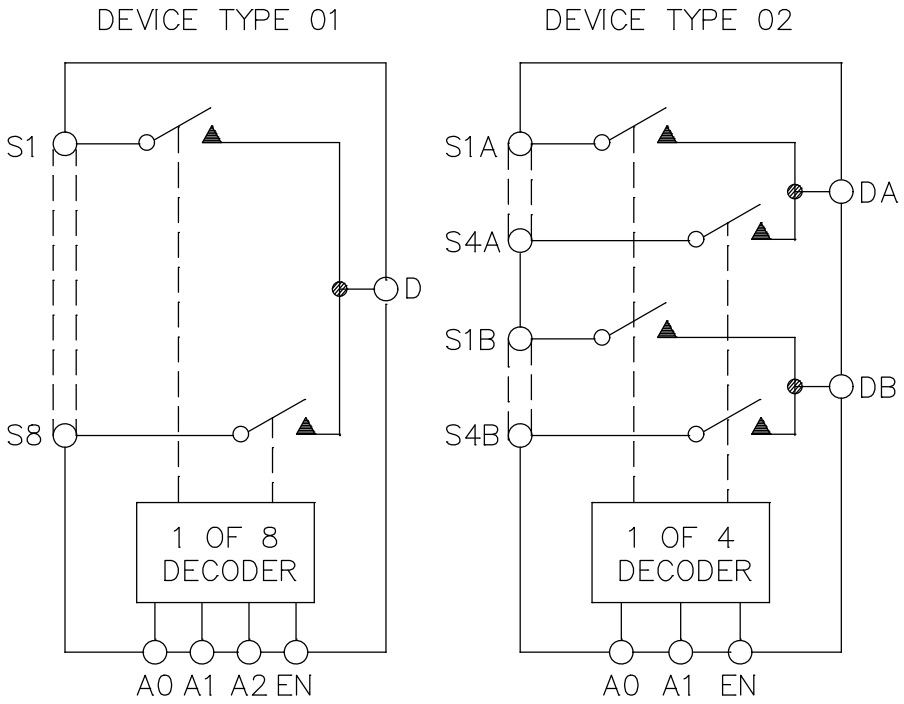

FIGURE 4. Logic diagram.

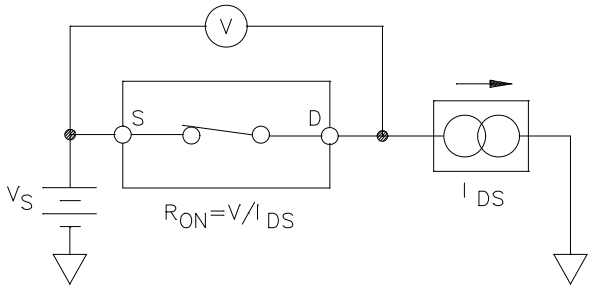

FIGURE 5. On resistance.

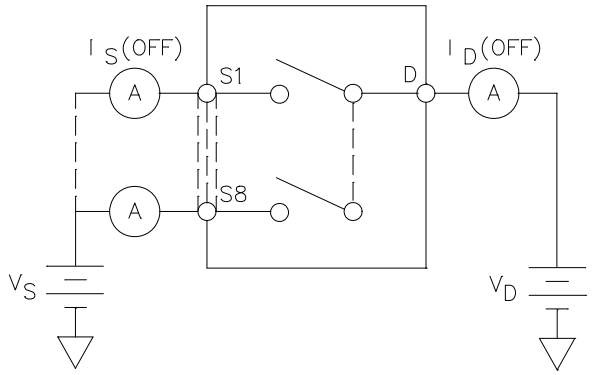

FIGURE 6. Off leakage.

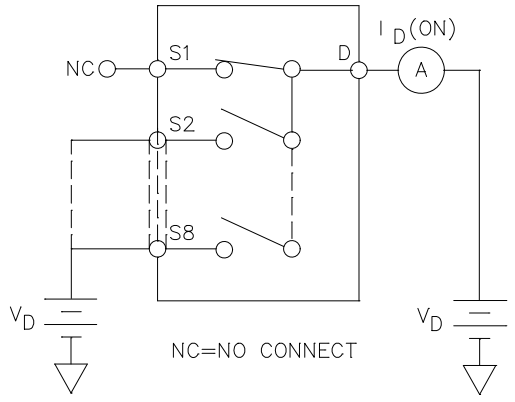

FIGURE 7. On leakage.

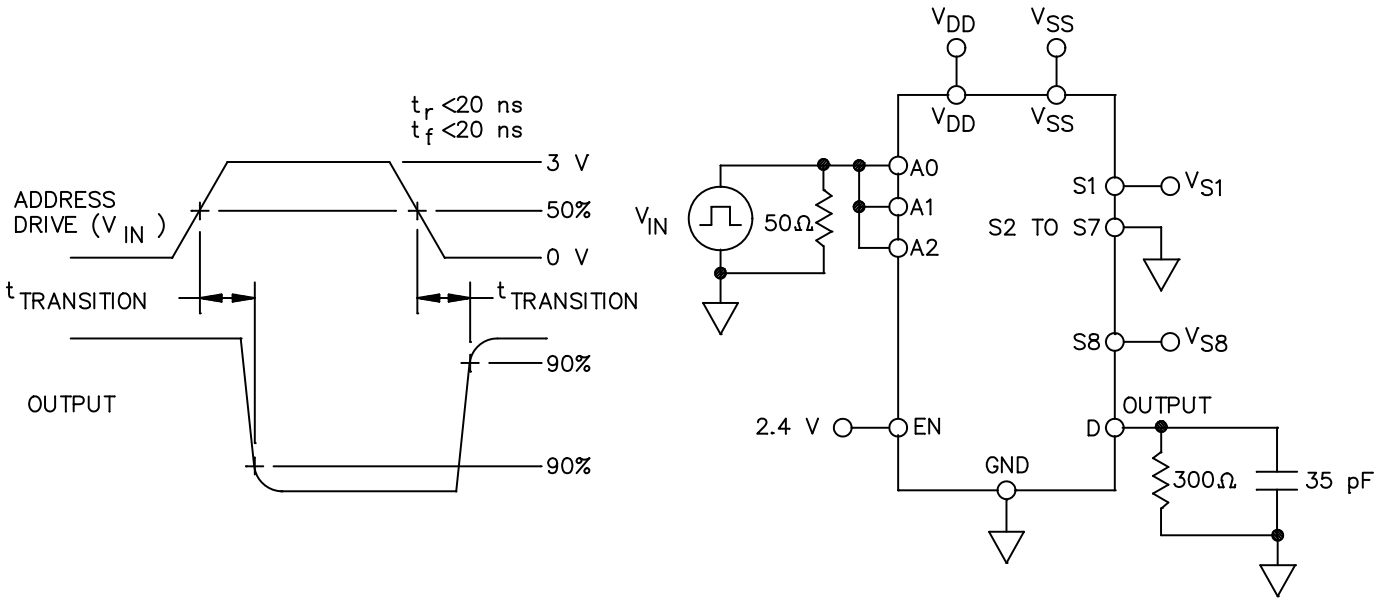

FIGURE 8. Address to output switching times, $t_{TRANSACTION}$.

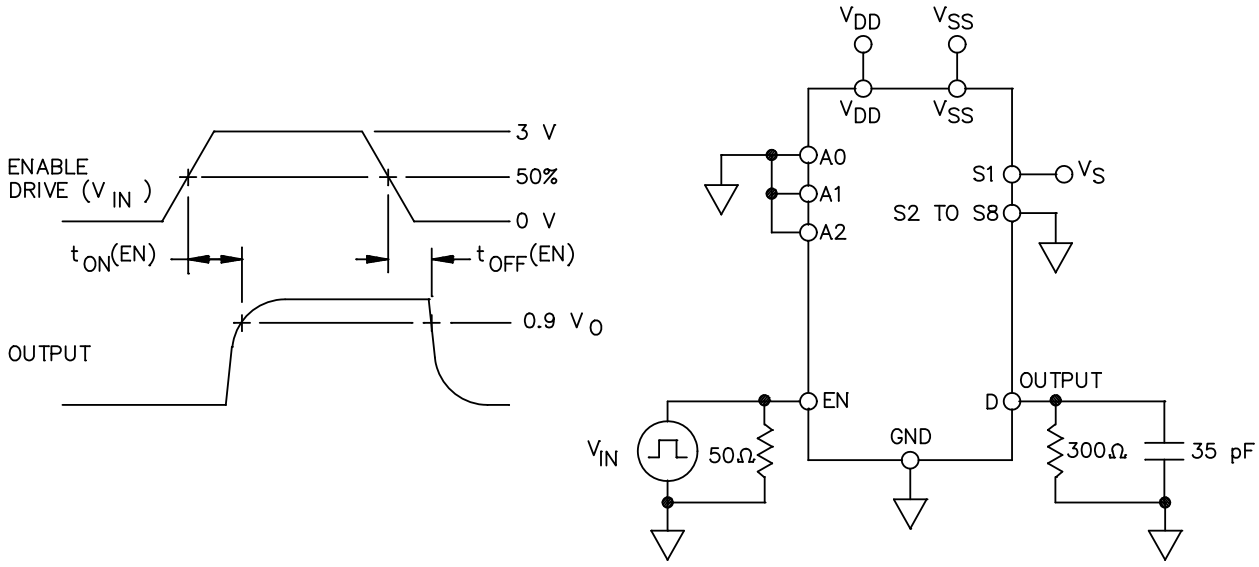

FIGURE 9. Enable delay, t_{ON}(EN), t_{OFF}(EN).

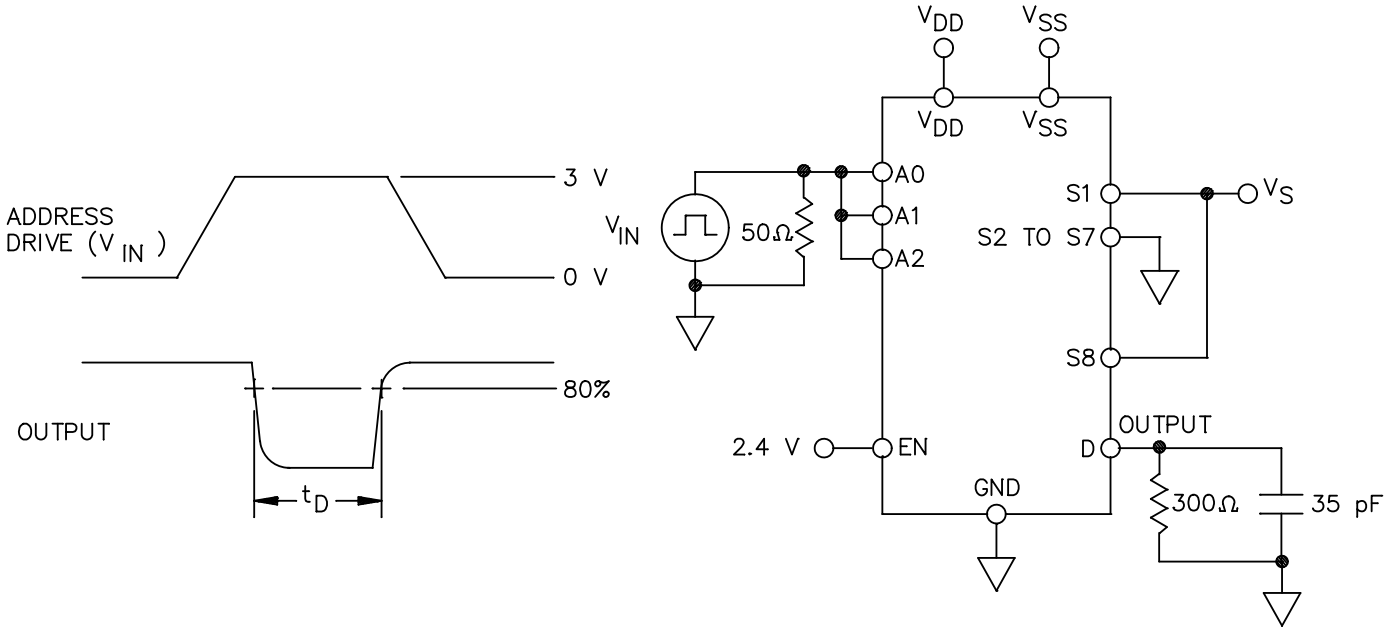

FIGURE 10. Break before make time delay, t_D.

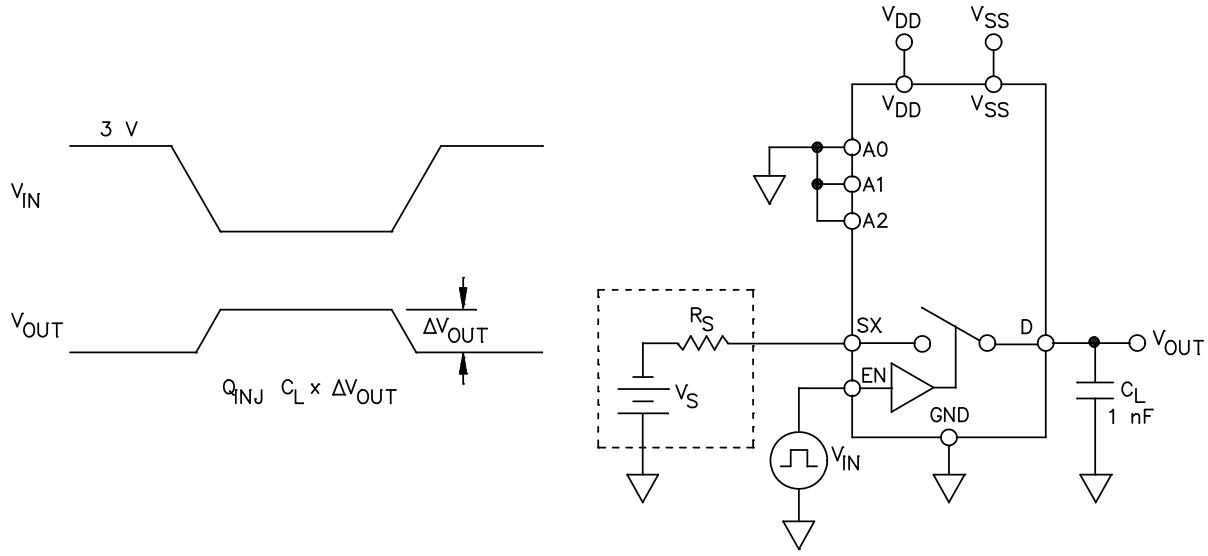

FIGURE 11. Charge injection.

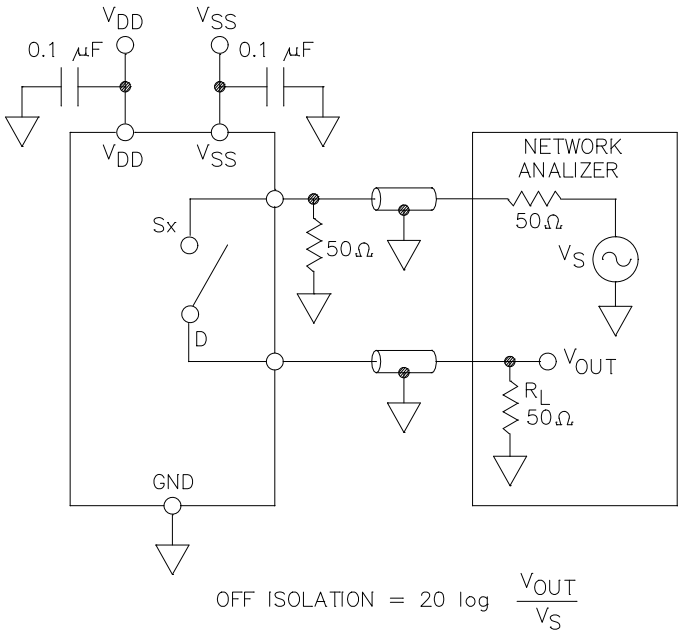

FIGURE 12. Off isolation.

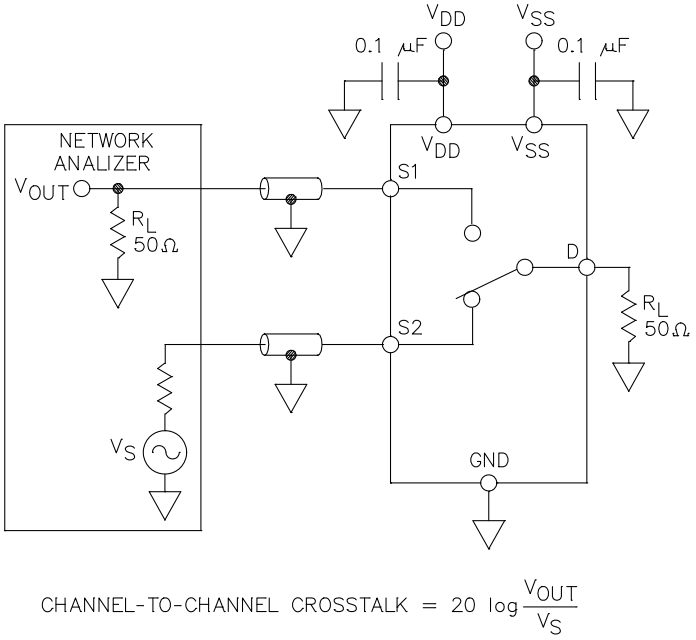

FIGURE 13. Channel to channel crosstalk.

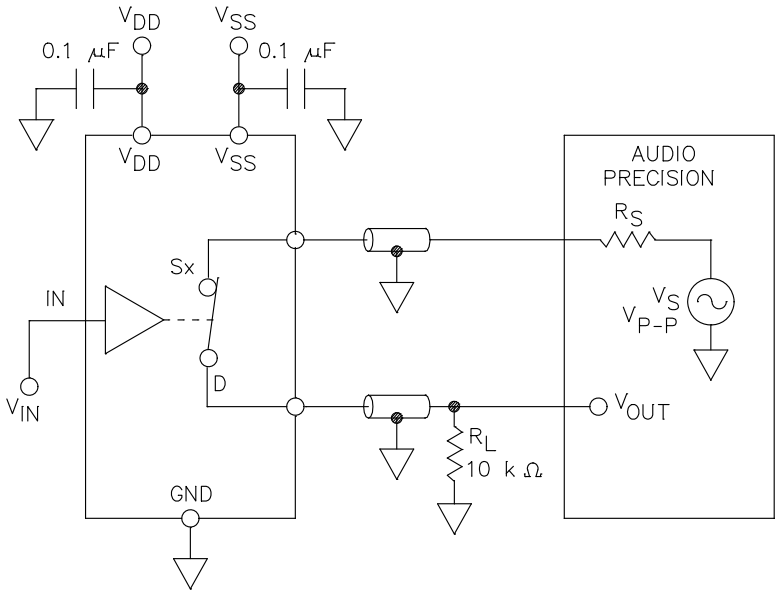

FIGURE 14. THD + noise figure.

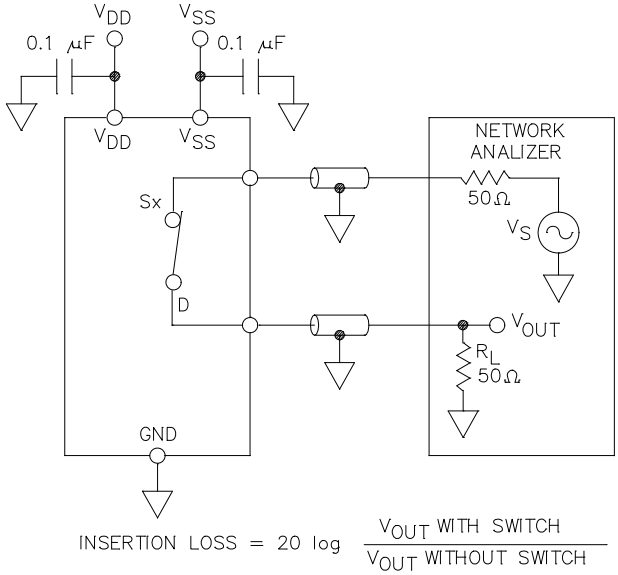

FIGURE 15. Bandwidth.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/16607-01XE	24355	ADG5408TCPZ-EP
V62/16607-02XE	24355	ADG5409TCPZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123