REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Under Table I, make changes to Differential nonlinearity, Signal to noise ratio with f_{IN} = 70 MHz, Signal to noise and distortion with f_{IN} = 70 MHz, and Worst other (harmonic or spur) with f_{IN} = 70 MHz parameter limits. Update document paragraphs to current requirements. - ro	21-06-10	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV	A	A	A	A	A	A	A	A	A	A	A	A										
PAGE	18	19	20	21	22	23	24	25	26	27	28	29										

REV STATUS OF PAGES																					
	REV		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 16-01-06	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, DIGITAL-LINEAR, 14 BIT, 125 MSPS, 1.8 V DUAL ANALOG TO DIGITAL, MONOLITHIC SILICON
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/16606**
	REV A	**PAGE** 1 **OF** 29

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V038-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance14 bit, 125 million samples per second (MSPS), 1.8 V dual analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16606	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD9648-EP	14 bit, 125 MSPS, 1.8 V dual analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	64	MO-220-WMMD	Quad lead frame chip scale package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Electrical:

AVDD to AGND	-0.3 V to +2.0 V
DRVDD to AGND	-0.3 V to +2.0 V
VIN+A/VINB+, VINA-/VINB- to AGND	-0.3 V to AVDD + 0.2 V
CLK+, CLK- to AGND	-0.3 V to AVDD + 0.2 V
SYNC to DRVDD	-0.3 V to AVDD + 0.2 V
VCM to AGND	-0.3 V to AVDD + 0.2 V
RBIAS to AGND	-0.3 V to AVDD + 0.2 V
CSB to AGND	-0.3 V to DRVDD + 0.2 V
SCLK/DFS to AGND	-0.3 V to DRVDD + 0.2 V
SDIO/DCS to AGND	-0.3 V to DRVDD + 0.2 V
OEB	-0.3 V to DRVDD + 0.2 V
PDWN	-0.3 V to DRVDD + 0.2 V
D0A/D0B through D13A/D13B to AGND	-0.3 V to DRVDD + 0.2 V
DCOA/DCOB to AGND	-0.3 V to DRVDD + 0.2 V

Environmental:

Operating ambient temperature range (T_A)	-55°C to +125°C
Maximum junction temperature under bias (T_J)	+150°C
Storage ambient temperature range	-65°C to +150°C

1.4 Recommended operating conditions. 2/

AVDD	+1.8 V
DRVDD	+1.8 V

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Airflow velocity		0	m/sec
Thermal resistance, junction-to-ambient 3/	θ_{JA}	22.3	°C/W
Thermal resistance, junction-to-case 4/	θ_{JC}	1.4	°C/W
Thermal resistance, junction-to-board 5/	θ_{JB}	11.8	°C/W
Characterization parameter, junction-to-top 6/	ψ_{JT}	0.1	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
3/ Per JEDEC 51-7.
4/ Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
5/ Per MIL-STD-883, method 1012.1.
6/ Per JEDEC JESD51-8 (still air).

2. APPLICABLE DOCUMENTS

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

JEDEC Solid State Technology Association

EIA/JESD 51-2	-	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
EIA/JEDEC 51-6	-	Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)
EIA/JEDEC 51-7	-	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
EIA/JESD51-8	-	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
JEDEC PUB 95	-	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figures 3, 4, 5, and 6.

TABLE I. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications section							
Resolution			-55°C to +125°C	01	14		Bits
Accuracy							
No missing codes			-55°C to +125°C	01	Guaranteed typical		
Offset error			-55°C to +125°C	01	-0.3 typical		%FSR
					-0.8	+0.2	
Gain error			-55°C to +125°C	01	±1.3 typical		%FSR
					-6.3	+6.3	
Differential nonlinearity	DNL	3/	+25°C	01	±0.5 typical		LSB
			-55°C to +125°C		-0.7	+1.3	
Integral nonlinearity	INL	3/	+25°C	01	±1.0 typical		LSB
			-55°C to +125°C		-2.6	+2.6	
Matching characteristics							
Offset error			-55°C to +125°C	01	±0.01 typical		%FSR
						±0.8	
Gain error			-55°C to +125°C	01	±0.5 typical		%FSR
						±7.0	
Temperature drift							
Offset error			-55°C to +125°C	01	±2 typical		ppm/ °C
Gain error			-55°C to +125°C	01	±50 typical		ppm/ °C
Internal voltage reference							
Output voltage			-55°C to +125°C	01	1.00 typical		V
(1 V mode)					0.98	1.02	
Load regulation error at 1.0 mA			-55°C to +125°C	01	2 typical		mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications section – continued.							
Input referred noise, VREF = 1.0 V			+25°C	01	0.98 typical		LSB rms
Analog input							
Input span, VREF = 1.0 V			-55°C to +125°C	01	2 typical		Vp-p
Input capacitance 4/			-55°C to +125°C	01	5 typical		pF
Input resistance (differential)			-55°C to +125°C	01	7.5 typical		kΩ
Input common mode voltage			-55°C to +125°C	01	0.9 typical		V
Input common mode range			-55°C to +125°C	01	0.5	1.3	V
Power supplies							
Analog power supply voltage	AVDD		-55°C to +125°C	01	1.8 typical		V
					1.7	1.9	
Digital output driver supply voltage	DRVDD		-55°C to +125°C	01	1.8 typical		V
					1.7	1.9	
Analog power supply current	I_{AVDD}	3/	-55°C to +125°C	01	95 typical		mA
						100	
Digital output driver supply current (1.8 V CMOS)	I_{DRVDD}	3/	-55°C to +125°C	01	22.5 typical		mA
						23.8	
Digital output driver supply current (1.8 V LVDS)	I_{DRVDD}	3/	-55°C to +125°C	01	65.0 typical		mA
						66.4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications section – continued.							
Power consumption							
DC input			-55°C to +125°C	01	155.5 typical		mW
Sine wave input		DRVDD = 1.8 V CMOS output mode	-55°C to +125°C	01	211.5 typical		mW
						223	
Sine wave input		DRVDD = 1.8 V LVDS output mode	-55°C to +125°C	01	288 typical		mW
						300	
Standby power 5/			-55°C to +125°C	01	120 typical		mW
Power down power			-55°C to +125°C	01	2.0 typical		mW

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC specifications section.							
Signal to noise ratio	SNR	f_{IN} = 9.7 MHz	+25°C	01	75.0 typical		dBFS
		f_{IN} = 30.5 MHz			74.7 typical		
		f_{IN} = 70 MHz			74.5 typical		
			-55°C to +125°C		72.5		
		f_{IN} = 100 MHz	+25°C		73.9 typical		
		f_{IN} = 200 MHz			71.5 typical		
Signal to noise and distortion	SINAD	f_{IN} = 9.7 MHz	+25°C	01	73.9 typical		dBFS
		f_{IN} = 30.5 MHz			73.4 typical		
		f_{IN} = 70 MHz			73.3 typical		
			-55°C to +125°C		72.3		
		f_{IN} = 100 MHz	+25°C		72.8 typical		
		f_{IN} = 200 MHz			70.3 typical		
Effective number of bits	ENOB	f_{IN} = 9.7 MHz	+25°C	01	12 typical		Bits
		f_{IN} = 30.5 MHz			11.9 typical		
		f_{IN} = 70 MHz	-55°C to +125°C		11.9 typical		
					11.8		
		f_{IN} = 100 MHz	+25°C		11.8 typical		
		f_{IN} = 200 MHz			11.4 typical		
Worst second or third harmonic		f_{IN} = 9.7 MHz	+25°C	01	-96 typical		dBc
		f_{IN} = 30.5 MHz			-90 typical		
		f_{IN} = 70 MHz			-91 typical		
			-55°C to +125°C			-82	
		f_{IN} = 100 MHz	+25°C		-90 typical		
		f_{IN} = 200 MHz			-84 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC specifications section – continued.							
Spurious free dynamic range	SFDR	f_{IN} = 9.7 MHz	+25°C	01	96 typical		dBc
		f_{IN} = 30.5 MHz			90 typical		
		f_{IN} = 70 MHz			91 typical		
			-55°C to +125°C		82		
		f_{IN} = 100 MHz	+25°C		90 typical		
		f_{IN} = 200 MHz			84 typical		
Worst other (harmonic or spur)		f_{IN} = 9.7 MHz	+25°C	01	-97 typical		dBc
		f_{IN} = 30.5 MHz			-97 typical		
		f_{IN} = 70 MHz			-97 typical		
			-55°C to +125°C			-89	
		f_{IN} = 100 MHz	+25°C		-92 typical		
		f_{IN} = 200 MHz			-90 typical		
Two tone spurious free dynamic range		f_{IN} = 29 MHz (-7 dBFS), 32 MHz (-7 dBFS)	+25°C	01	84 typical		dBc
Crosstalk 6/			-55°C to +125°C	01	-95 typical		dB
Analog input bandwidth			+25°C	01	650 typical		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital specification section.							
Differential clock inputs (CLK+, CLK-)							
Logic compliance				01	CMOS/LVDS/ LVPECL		
Internal common mode bias			-55°C to +125°C	01	0.9 typical		V
Differential input voltage			-55°C to +125°C	01	0.3	3.6	Vp-p
Input voltage range			-55°C to +125°C	01	AGND – 0.3	AVDD + 0.2	V
Input common mode range			-55°C to +125°C	01	0.9	1.4	V
High level input current			-55°C to +125°C	01	-10	+10	μA
Low level input current			-55°C to +125°C	01	-10	+10	μA
Input capacitance			-55°C to +125°C	01	4 typical		pF
Input resistance			-55°C to +125°C	01	10 typical		kΩ
					8	12	
Logic input (CSB) 7/							
High level input voltage			-55°C to +125°C	01	1.22	DRVDD + 0.2	V
Low level input voltage			-55°C to +125°C	01	0	0.6	V
High level input current			-55°C to +125°C	01	-10	+10	μA
Low level input current			-55°C to +125°C	01	40	132	μA
Input resistance			-55°C to +125°C	01	26 typical		kΩ
Input capacitance			-55°C to +125°C	01	2 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital specification section – continued.							
Logic input (SCLK/DFS/SYNC) 8/							
High level input voltage			-55°C to +125°C	01	1.22	DRVDD + 0.2	V
Low level input voltage			-55°C to +125°C	01	0	0.6	V
High level input current		VIN = 1.8 V	-55°C to +125°C	01	-92	-135	μA
Low level input current			-55°C to +125°C	01	-10	+10	μA
Input resistance			-55°C to +125°C	01	26 typical		kΩ
Input capacitance			-55°C to +125°C	01	2 typical		pF
Logic input/output (SDIO/DCS) 7/							
High level input voltage			-55°C to +125°C	01	1.22	DRVDD + 0.2	V
Low level input voltage			-55°C to +125°C	01	0	0.6	V
High level input current			-55°C to +125°C	01	-10	+10	μA
Low level input current			-55°C to +125°C	01	38	128	μA
Input resistance			-55°C to +125°C	01	26 typical		kΩ
Input capacitance			-55°C to +125°C	01	5 typical		pF
Logic inputs (OEB, PDWN) 8/							
High level input voltage			-55°C to +125°C	01	1.22	DRVDD + 0.2	V
Low level input voltage			-55°C to +125°C	01	0	0.6	V
High level input current		VIN = 1.8 V	-55°C to +125°C	01	-90	-134	μA
Low level input current			-55°C to +125°C	01	-10	+10	μA
Input resistance			-55°C to +125°C	01	26 typical		kΩ
Input capacitance			-55°C to +125°C	01	5 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital specification section – continued.							
Digital outputs		CMOS mode DRVDD = 1.8 V					
High level output voltage		I_{OH} = 50 μA	-55°C to +125°C	01	1.79		V
		I_{OH} = 0.5 mA			1.75		
Low level output voltage		I_{OL} = 1.6 mA	-55°C to +125°C	01		0.2	V
		I_{OL} = 50 μA				0.05	
Digital outputs		LVDS mode DRVDD = 1.8 V					
Differential output voltage, ANSI mode	V_{OD}		-55°C to +125°C	01	345 typical		mV
					290	400	
Output offset voltage, ANSI mode	V_{OS}		-55°C to +125°C	01	1.25 typical		V
					1.15	1.35	
Differential output voltage, reduced swing mode	V_{OD}		-55°C to +125°C	01	200 typical		mV
					160	230	
Output offset voltage, reduced swing mode	V_{OS}		-55°C to +125°C	01	1.25 typical		V
					1.15	1.35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching specifications section.							
Clock input parameters.							
Input clock rate			-55°C to +125°C	01		1000	MHz
Conversion rate 9/		DCS enabled	-55°C to +125°C	01	20	125	MSPS
		DCS disabled			10	125	
CLK period, divide by 1 mode	t_{CLK}		-55°C to +125°C	01	8 typical		ns
CLK pulse width high	t_{CH}		-55°C to +125°C	01	4 typical		ns
Aperture delay	t_A		-55°C to +125°C	01	1.0 typical		ns
Aperture uncertainty, jitter	t_J		-55°C to +125°C	01	0.137 typical		ps rms
Data output parameters		CMOS mode (DRVDD = 1.8 V)					
Data propagation delay	t_{PD}		-55°C to +125°C	01	2.9 typical		ns
					1.8	4.4	
DCO propagation delay	t_{DCO}	10/	-55°C to +125°C	01	3.1typical		ns
					2.0	4.4	
DCO to data skew	t_{SKEW}		-55°C to +125°C	01	-0.1 typical		ns
					-1.2	+1.0	
Data output parameters		LVDS mode (DRVDD = 1.8 V)					
Data propagation delay	t_{PD}		-55°C to +125°C	01	2.4 typical		ns
DCO propagation delay	t_{DCO}	10/	-55°C to +125°C	01	2.4 typical		ns
DCO to data skew	t_{SKEW}		-55°C to +125°C	01	+0.03 typical		ns
					-0.20	+0.25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching specifications section – continued.							
Data output parameters							
CMOS mode pipeline delay (latency)			-55°C to +125°C	01	16 typical		Cycles
LVDS mode pipeline delay (latency) channel A/channel B			-55°C to +125°C	01	16/16.5 typical		Cycles
Wake up time 11/ (power time)			-55°C to +125°C	01	350 typical		ns
Wake up time (standby)			-55°C to +125°C	01	250 typical		ns
Out of range recovery time			-55°C to +125°C	01	2 typical		Cycles
Timing specifications section.							
SYNC timing requirements.							
SYNC to rising edge of CLK+ setup time	tSSYNC		-55°C to +125°C	01	0.24 typical		ns
SYNC to rising edge of CLK+ hold time	tHSYNC		-55°C to +125°C	01	0.40 typical		ns
SPI timing requirements.							
Setup time between the data and the rising edge of SCLK	tDS		-55°C to +125°C	01	2		ns
Hold time between the data and the rising edge of SCLK	tDH		-55°C to +125°C	01	2		ns
Period of the SCLK	tCLK		-55°C to +125°C	01	40		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications section – continued.							
SPI timing requirements - continued.							
Setup time between CSB and SCLK	t_S		-55°C to +125°C	01	2		ns
Hold time between CSB and SCLK	t_H		-55°C to +125°C	01	2		ns
SCLK pulse width high	t_{HIGH}		-55°C to +125°C	01	10		ns
SCLK pulse width low	t_{LOW}		-55°C to +125°C	01	10		ns
Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	t_{EN_SDIO}		-55°C to +125°C	01	10		ns
Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	t_{DIS_SDIO}		-55°C to +125°C	01	10		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = -1.0 dBFS differential input, 1.0 V internal reference, and duty cycle stabilizer (DCS) enabled.

3/ Measure with a low input frequency, full scale sine wave, with approximately 5 pF loading on each output bit.

4/ Input capacitance refers to the effective capacitance between one differential input pin and analog ground (AGND).

5/ Standby power is measured with a dc input and with the CLK± pins active (1.8 V CMOS mode).

6/ Crosstalk is measured at 100 MHz with -1.0 dBFS on one channel and no input on the alternate channel.

7/ Pull up.

8/ Pull down.

9/ Conversion rate is the clock rate after the divider.

10/ Additional data clock output (DCO) delay can be added by writing to bits [2:0] in SPI register 0 x 17.

11/ Wake up time is defined as the time required to return to normal operation from power down mode.

Case X

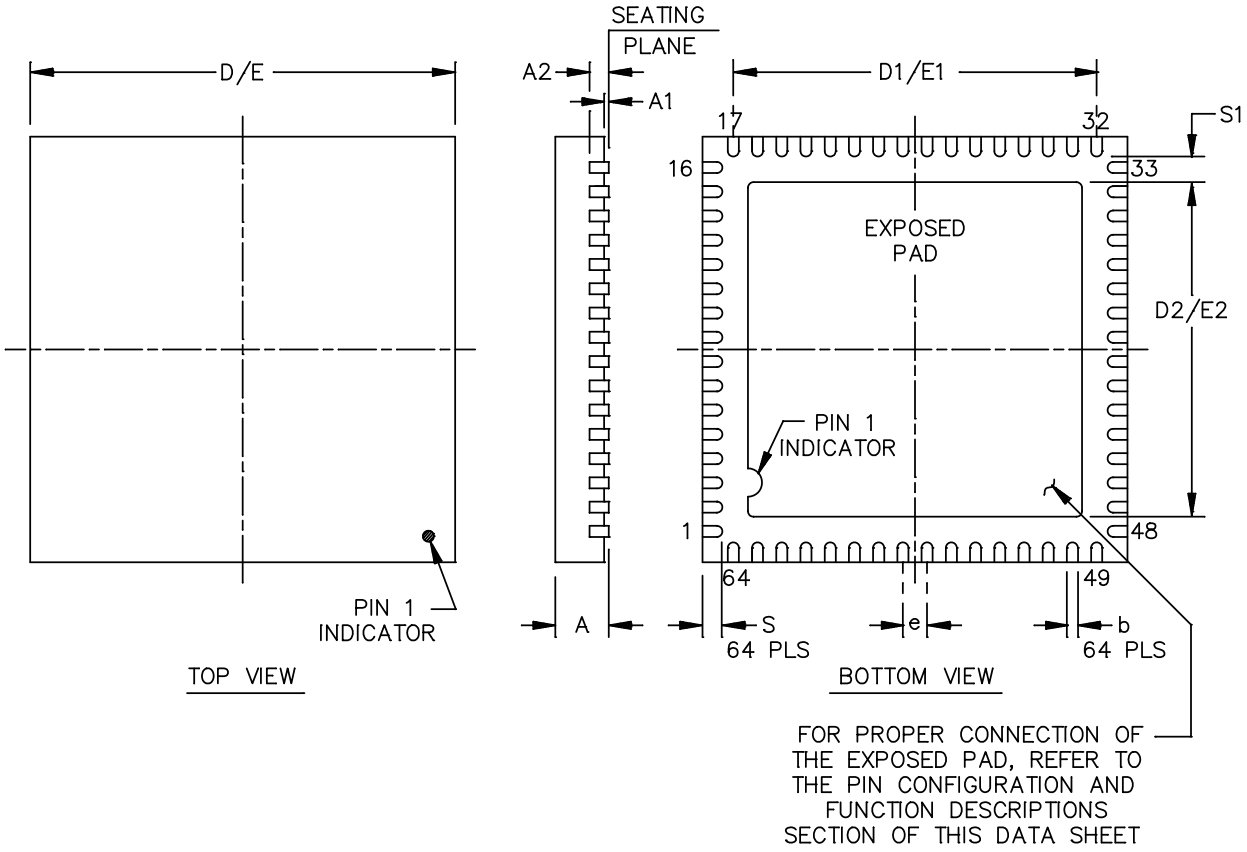

FIGURE 1. Case outline.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.027	.029	.031	0.70	0.75	0.80
A1	---	.0007	.0019	---	0.02	0.05
A2	.007 REF			0.203 REF		
b	.007	.009	.011	0.18	0.25	0.30
D/E	.350	.354	.358	8.90	9.00	9.10
D1/E1	.295 REF			7.50 REF		
D2/E2	.240	.244	.248	6.10	6.20	6.30
e	.019 BSC			0.50 BSC		
S	.013	.015	.017	0.35	0.40	0.45
S1	.007	---	---	0.20	---	---

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-220-WMMD.

FIGURE 1. Case outline - Continued.

Parallel CMOS mode

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
ADC power supplies			
10,19,28,37	DRVDD	Supply	Digital output driver supply (1.8 V nominal).
49,50,53,54, 59,60,63,64	AVDD	Supply	Analog power supply (1.8 V nominal).
4,5,25,26	NC		No connect. Do not connect to these pins.
Exposed pad	AGND	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the devices. This exposed pad must be connected to ground for proper operation.
ADC analog			
51	VIN+A	Input	Differential analog input pin (+) for channel A.
52	VIN-A	Input	Differential analog input pin (-) for channel A.
62	VIN+B	Input	Differential analog input pin (+) for channel B.
61	VIN-B	Input	Differential analog input pin (-) for channel B.
55	VREF	Input/output	Voltage reference input/output.
56	SENSE	Input	Reference mode selection.
58	RBIAS	Input/output	External reference bias resistor. Connect to a 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common mode level bias output for analog inputs.
1	CLK+	Input	ADC clock input – true.
2	CLK-	Input	ADC clock input – complement.
Digital input			
3	SYNC	Input	Digital synchronization pin. Slave mode only.
Digital outputs.			
27	D0A (LSB)	Output	Channel A CMOS output data.
29	D1A	Output	Channel A CMOS output data.
30	D2A	Output	Channel A CMOS output data.
31	D3A	Output	Channel A CMOS output data.
32	D4A	Output	Channel A CMOS output data.
33	D5A	Output	Channel A CMOS output data.

FIGURE 2. Terminal connections.

Parallel CMOS mode – continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
Digital outputs - continued.			
34	D6A	Output	Channel A CMOS output data.
35	D7A	Output	Channel A CMOS output data.
36	D8A	Output	Channel A CMOS output data.
38	D9A	Output	Channel A CMOS output data.
39	D10A	Output	Channel A CMOS output data.
40	D11A	Output	Channel A CMOS output data.
41	D12A	Output	Channel A CMOS output data.
42	D13A (MSB)	Output	Channel A CMOS output data.
43	ORA	Output	Channel A overrange output.
6	D0B (LSB)	Output	Channel B CMOS output data.
7	D1B	Output	Channel B CMOS output data.
8	D2B	Output	Channel B CMOS output data.
9	D3B	Output	Channel B CMOS output data.
11	D4B	Output	Channel B CMOS output data.
12	D5B	Output	Channel B CMOS output data.
13	D6B	Output	Channel B CMOS output data.
14	D7B	Output	Channel B CMOS output data.
15	D8B	Output	Channel B CMOS output data.
16	D9B	Output	Channel B CMOS output data.
17	D10B	Output	Channel B CMOS output data.
18	D11B	Output	Channel B CMOS output data.
20	D12B	Output	Channel B CMOS output data.
21	D13B (MSB)	Output	Channel B CMOS output data.
22	ORB	Output	Channel B overrange output
24	DCOA	Output	Channel A data clock output.
23	DCOB	Output	Channel B data clock output.

FIGURE 2. Terminal connections - continued.

Parallel CMOS mode – continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
SPI control			
45	SCLK/DFS	Input	SPI serial clock/data format select pin in external pin mode.
44	SDIO/DCS	Input/output	SPI serial data I/O duty cycle stabilizer pin in external pin mode.
46	CSB	Input	SPI chip select (active low).
ADC configuration			
47	OEB	Input	Output enable input (active low).
48	PDWN	Input	Power down input in external pin mode. In SPI mode, this input can be configured as power down or standby.

FIGURE 2. Terminal connections - continued.

Interleaved parallel LVDS mode

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
ADC power supplies.			
10,19,28,37	DRVDD	Supply	Digital output driver supply (1.8 V nominal).
49,50,53,54, 59,60,63,64	AVDD	Supply	Analog power supply (1.8 V nominal).
4,5,6,7	NC		No connect. Do not connect to these pins.
Exposed pad	AGND	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the devices. This exposed pad must be connected to ground for proper operation.
ADC analog			
51	VIN+A	Input	Differential analog input pin (+) for channel A.
52	VIN-A	Input	Differential analog input pin (-) for channel A.
62	VIN+B	Input	Differential analog input pin (+) for channel B.
61	VIN-B	Input	Differential analog input pin (-) for channel B.
55	VREF	Input/output	Voltage reference input/output.
56	SENSE	Input	Reference mode selection.
58	RBIAS	Input/output	External reference bias resistor. Connect to a 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common mode level bias output for analog inputs.
1	CLK+	Input	ADC clock input – true.
2	CLK-	Input	ADC clock input – complement.
Digital input			
3	SYNC	Input	Digital synchronization pin. Slave mode only.
Digital outputs			
9	D0+ (LSB)	Output	Channel A/channel B LVDS output data 0 - true.
8	D0- (LSB)	Output	Channel A/channel B LVDS output data 0 - complement.
12	D1+	Output	Channel A/channel B LVDS output data 1 - true.
11	D1-	Output	Channel A/channel B LVDS output data 1 - complement.
14	D2+	Output	Channel A/channel B LVDS output data 2 - true.
13	D2-	Output	Channel A/channel B LVDS output data 2 - complement.

FIGURE 2. Terminal connections - continued.

Interleaved parallel LVDS mode – continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
Digital outputs continued.			
16	D3+	Output	Channel A/channel B LVDS output data 3 - true.
15	D3-	Output	Channel A/channel B LVDS output data 3 - complement.
18	D4+	Output	Channel A/channel B LVDS output data 4 - true.
17	D4-	Output	Channel A/channel B LVDS output data 4 - complement.
21	D5+	Output	Channel A/channel B LVDS output data 5 - true.
20	D5-	Output	Channel A/channel B LVDS output data 5 - complement.
23	D6+	Output	Channel A/channel B LVDS output data 6 - true.
22	D6-	Output	Channel A/channel B LVDS output data 6 - complement.
27	D7+	Output	Channel A/channel B LVDS output data 7 - true.
26	D7-	Output	Channel A/channel B LVDS output data 7 - complement.
30	D8+	Output	Channel A/channel B LVDS output data 8 - true.
29	D8-	Output	Channel A/channel B LVDS output data 8 - complement.
32	D9+	Output	Channel A/channel B LVDS output data 9 - true.
31	D9-	Output	Channel A/channel B LVDS output data 9 - complement.
34	D10+	Output	Channel A/channel B LVDS output data 10 - true.
33	D10-	Output	Channel A/channel B LVDS output data 10 - complement.
36	D11+	Output	Channel A/channel B LVDS output data 11 - true.
35	D11-	Output	Channel A/channel B LVDS output data 11 - complement.
39	D12+	Output	Channel A/channel B LVDS output data 12 - true.
38	D12-	Output	Channel A/channel B LVDS output data 12 - complement.
41	D13+ (MSB)	Output	Channel A/channel B LVDS output data 13 - true.
40	D13- (MSB)	Output	Channel A/channel B LVDS output data 13 - complement.
43	OR+	Output	Channel A/channel B LVDS overrange output - true.
42	OR-	Output	Channel A/channel B LVDS overrange output - complement.
25	DCO+	Output	Channel A/channel B LVDS data clock output - true.
24	DCO-	Output	Channel A/channel B LVDS data clock output - complement.

FIGURE 2. Terminal connections - continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
SPI control			
45	SCLK/DFS	Input	SPI serial clock/data format select pin in external pin mode.
44	SDIO/DCS	Input/output	SPI serial data I/O duty cycle stabilizer pin in external pin mode.
46	CSB	Input	SPI chip select (active low).
ADC configuration.			
47	OEB	Input	Output enable input (active low).
48	PDWN	Input	Power down input in external pin mode. In SPI mode, this input can be configured as power down or standby.

FIGURE 2. Terminal connections - continued.

Channel multiplexed parallel LVDS mode

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
ADC power supplies			
10,19,28,37	DRVDD	Supply	Digital output driver supply (1.8 V nominal).
49,50,53,54, 59,60,63,64	AVDD	Supply	Analog power supply (1.8 V nominal).
4,5,6,7	NC		No connect. Do not connect to these pins.
Exposed pad	AGND	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the devices. This exposed pad must be connected to ground for proper operation.
ADC analog			
51	VIN+A	Input	Differential analog input pin (+) for channel A.
52	VIN-A	Input	Differential analog input pin (-) for channel A.
62	VIN+B	Input	Differential analog input pin (+) for channel B.
61	VIN-B	Input	Differential analog input pin (-) for channel B.
55	VREF	Input/output	Voltage reference input/output.
56	SENSE	Input	Reference mode selection.
58	RBIAS	Input/output	External reference bias resistor. Connect to a 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common mode level bias output for analog inputs.
1	CLK+	Input	ADC clock input – true.
2	CLK-	Input	ADC clock input – complement.
Digital input.			
3	SYNC	Input	Digital synchronization pin. Slave mode only.
Digital outputs.			
8	B D1-/D0- (LSB)	Output	Channel B LVDS output data 1/data 0 - complement.
9	B D1+/D0+ (LSB)	Output	Channel B LVDS output data 1/data 0 - true.
11	B D3-/D2-	Output	Channel B LVDS output data 3/data 2 - complement.
12	B D3+/D2+	Output	Channel B LVDS output data 3/data 2 - true.
13	B D5-/D4-	Output	Channel B LVDS output data 5/data 4 - complement.
14	B D5+/D4+	Output	Channel B LVDS output data 5/data 4 - true.

FIGURE 2. Terminal connections - continued.

Channel multiplexed parallel LVDS mode – continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
Digital outputs - continued.			
15	B D7-/D6-	Output	Channel B LVDS output data 7/data 6 - complement.
16	B D7+/D6+	Output	Channel B LVDS output data 7/data 6 - true.
17	B D9-/D8-	Output	Channel B LVDS output data 9/data 8 - complement.
18	B D9+/D8+	Output	Channel B LVDS output data 9/data 8 - true.
20	B D11-/D10-	Output	Channel B LVDS output data 11/data 10 - complement.
21	B D11+/D10+	Output	Channel B LVDS output data 11/data 10 - true.
22	B D13-/D12- (MSB)	Output	Channel B LVDS output data 13/data 12 - complement.
23	B D13+/D12+ (MSB)	Output	Channel B LVDS output data 13/data 12 - true.
26	A D1-/D0- (LSB)	Output	Channel A LVDS output data 1/data 0 - complement.
27	A D1+/D0+ (LSB)	Output	Channel A LVDS output data 1/data 0 - true.
29	A D3-/D2-	Output	Channel A LVDS output data 3/data 2 - complement.
30	A D3+/D2+	Output	Channel A LVDS output data 3/data 2 - true.
32	A D5+/D4+	Output	Channel A LVDS output data 5/data 4 - true.
31	A D5-/D4-	Output	Channel A LVDS output data 5/data 4 - complement.
34	A D7+/D6+	Output	Channel A LVDS output data 7/data 6 - true.
33	A D7-/D6-	Output	Channel A LVDS output data 7/data 6 - complement.
36	A D9+/D8+	Output	Channel A LVDS output data 9/data 8 - true.
35	A D9-/D8-	Output	Channel A LVDS output data 9/data 8 - complement.
39	A D11+/D10+	Output	Channel A LVDS output data 11/data 10 - true.
38	A D11-/D10-	Output	Channel A LVDS output data 11/data 10 - complement.
41	A D13+/D12+ (MSB)	Output	Channel A LVDS output data 13/data 12 - true.
40	A D13-/D12- (MSB)	Output	Channel A LVDS output data 13/data 12 - complement.
43	OR+	Output	Channel A/channel B LVDS overrange output - true.
42	OR-	Output	Channel A/channel B LVDS overrange output - complement.
25	DCO+	Output	Channel A/channel B LVDS data clock output - true.
24	DCO-	Output	Channel A/channel B LVDS data clock output - complement.

FIGURE 2. Terminal connections - continued.

Channel multiplexed parallel LVDS mode – continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
SPI control			
45	SCLK/DFS	Input	SPI serial clock/data format select pin in external pin mode.
44	SDIO/DCS	Input/output	SPI serial data I/O duty cycle stabilizer pin in external pin mode.
46	CSB	Input	SPI chip select (active low).
ADC configuration.			
47	OEB	Input	Output enable input (active low).
48	PDWN	Input	Power down input in external pin mode. In SPI mode, this input can be configured as power down or standby.

FIGURE 2. Terminal connections - continued.

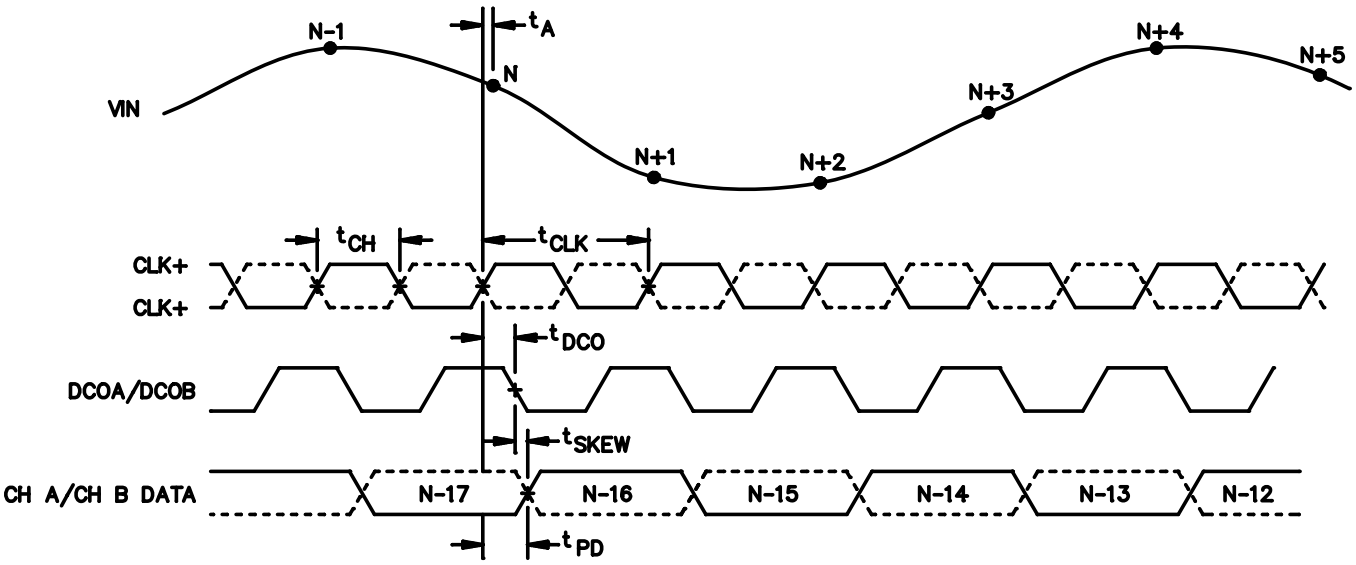

FIGURE 3. CMOS default output mode data output timing.

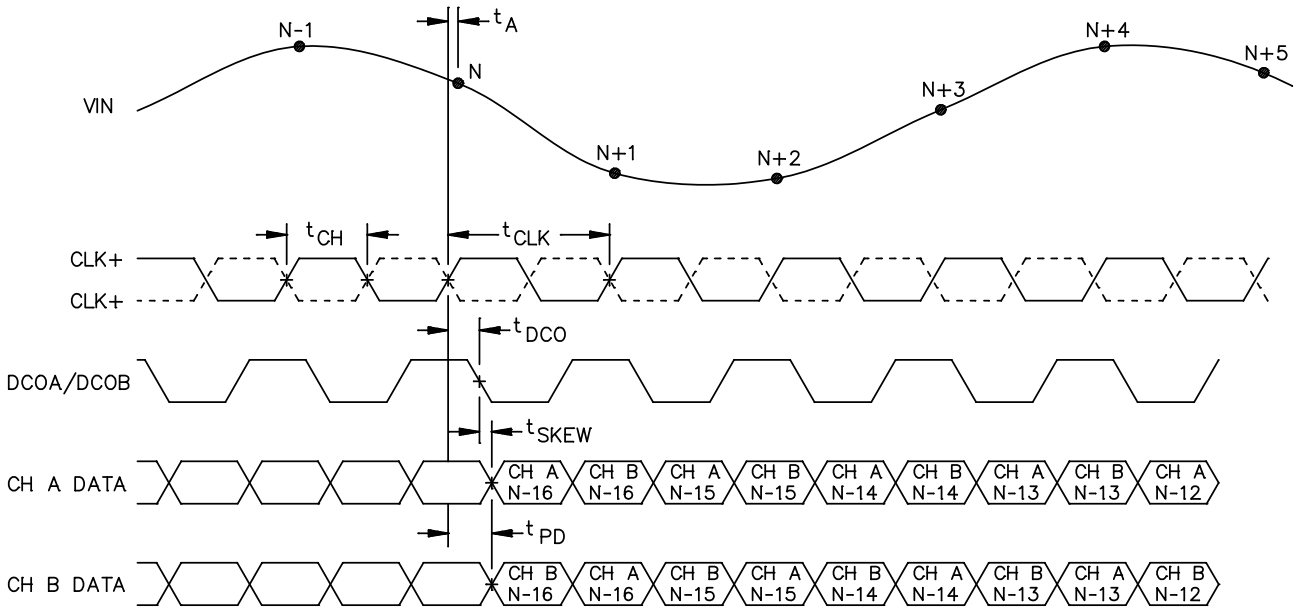

FIGURE 4. CMOS interleaved output mode data output timing.

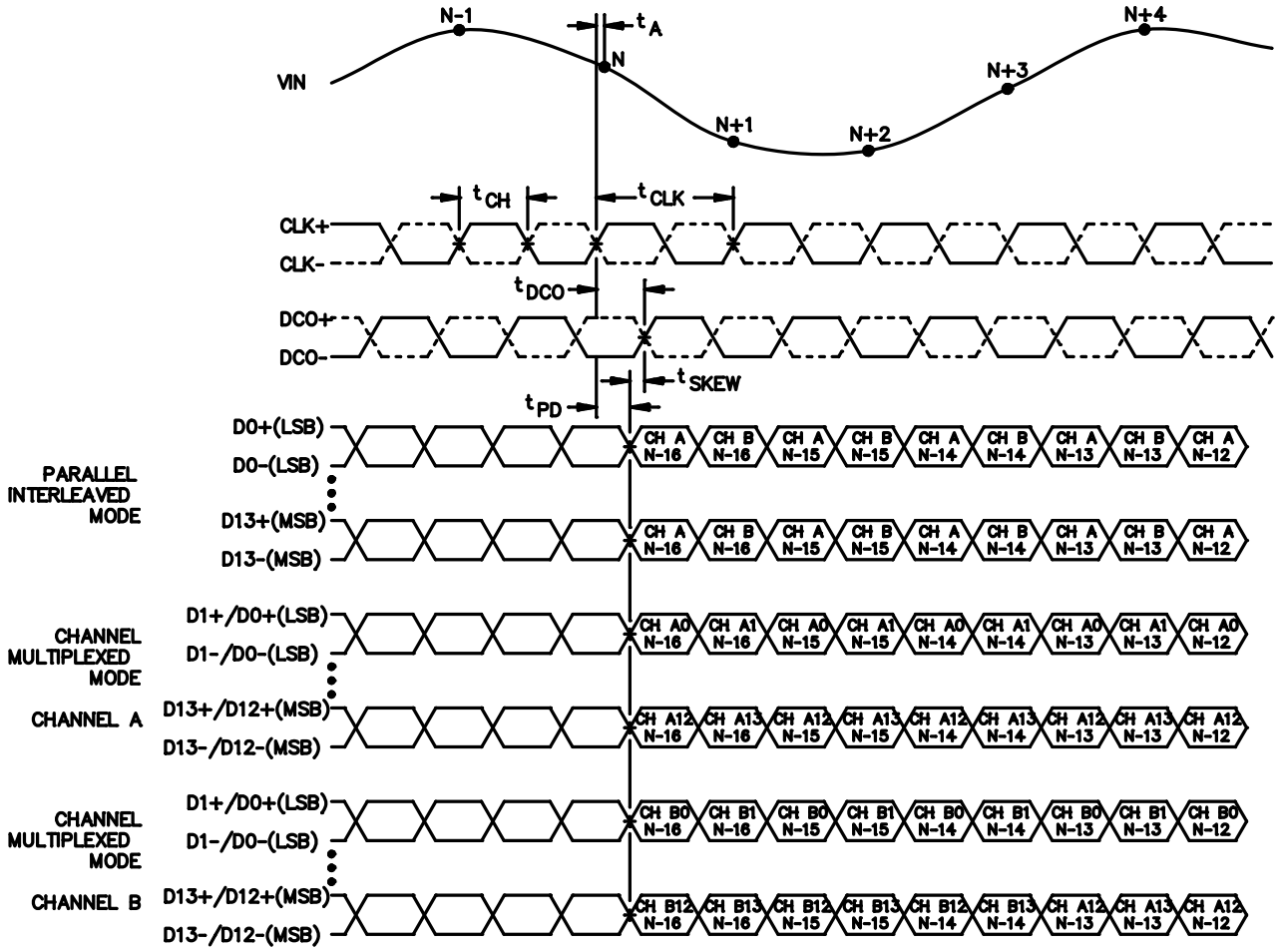

FIGURE 5. LVDS modes for data output timing.

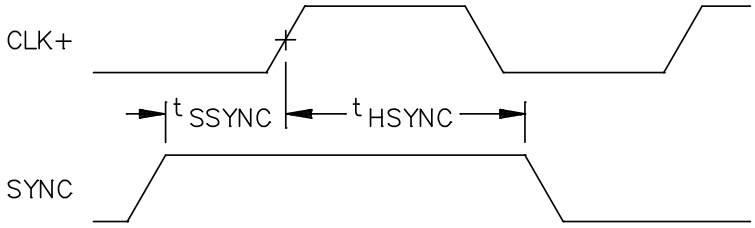

FIGURE 6. SYNC input timing requirements.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/16606-01XE	24355	Tray, 260 units	AD9648TCPZ-125-EP
V62/16606-01XE	24355	Reel, 750 units	AD9648TCPZ125EPRL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123