

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Modify Source current, IVTTOCLSRC and Sink current IVTTOCLSNK in Table I. Add Top side Marking and correct Vendor part number in last page. - PHN	15-12-08	Thomas M. Hess
B	Update document paragraphs to current requirements. - ro	21-12-15	James R. Eschmeyer



Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																				
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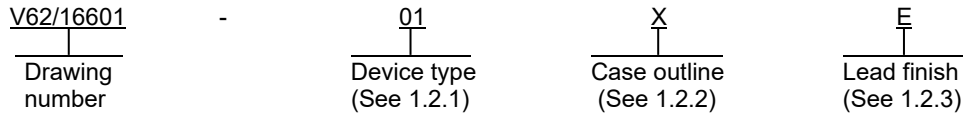
PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime	
Original date of drawing YY-MM-DD 15-11-24	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, LINEAR-DIGITAL, COMPLETE DDR2, DDR3 AND DDR3L MEMORY POWER SOLUTION SYNCHRONOUS BUS CONTROLLER, 2-A LDO, BUFFERED REFERENCE, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/16601
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DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance complete double data rate (DDR2), DDR3 and double data rate low voltage DDR3L memory power solution synchronous bus controller, 2 amp (A) low drop out (LDO), buffered reference microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TPS51216 –EP	Complete DDR2, DDR3 and DDR3L memory Power Solution Synchronous Bus Controller, 2-A LDO, Buffered Reference

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	JEDEC MO-220	Plastic quad flat pack no lead

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Input voltage: 2/	
VBST	-0.3 V to 36 V
VBST	-0.3 V to 6 V 3/
SW	-5.0 V to 30 V
VLDOIN, VDDQSNS, REFIN	-0.3 V to 3.6 V
VTTSENS	-0.3 V to 3.6 V
PGND, VTTGND	-0.3 V to 0.3 V
V5IN, S3, S5, TRIP, MODE	-0.3 V to 6 V
Output voltage: 2/	
DRVH	-5 V to 36 V
DRVH	-0.3 V to 6 V 3/
DRVH (duty cycle < 1%)	-2.5 V to 6 V 3/
VTTREF, VREF	-0.3 V to 3.6 V
VTT	-0.3 V to 3.6 V
DRVL	-0.3 V to 6 V
DRVL (duty cycle < 1%)	-2.5 V to 6 V
PGOOD	-0.3 V to 6 V
Junction temperature, (TJ)	-55°C to 135°C
Storage temperature range, (TSG)	-55°C to 150°C

1.4 ESD ratings:

Electrostatic discharge, V(ESD):

Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000 V 4/
Charged-device model (CDM), per JEDEC specification JESD22-C101	±500 V 5/

- 1/ Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- 2/ All voltage values are with respect to the network ground terminal unless otherwise noted.
- 3/ Voltage values are with respect to the SW terminal.
- 4/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- 5/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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1.5 Recommended operating conditions.

Supply voltage:

V5IN	4.5 V to 5.5 V	
VBST	-0.1 V to 33.5 V	
VBST	-0.1 V to 5.5 V	6/
SW	-3 V to 28 V	
SW	-4.5 V to 28 V	7/
VLDOIN, VDDQSNS, REFIN	-0.1 V to 3.5 V	
VTTSNS	-0.1 V to 3.5 V	
PGND, VTTGND	-0.1 V to 0.1 V	
S3, S5, TRIP, MODE	-0.1 V to 5.5 V	

Output voltage:

DRVH	-3 V to 33.5 V	
DRVH	-0.1 V to 5.5 V	6/
DRVH	-4.5 V to 33.5 V	7/
VTTREF, VREF	-0.1 V to 3.5 V	
VTT	-0.1 V to 3.5 V	
DRVL	-0.1 V to 5.5 V	
PGOOD	-0.1 V to 5.5 V	
Operating junction temperature, (T _J)	-55°C to 125°C	

1.6 Thermal characteristics.

Thermal metric 8/	Case outline X	Units
Junction to ambient thermal resistance, (R _{θJA})	94.1	°C/W
Junction to case (top) thermal resistance, (R _{θJctop})	58.1	°C/W
Junction to board thermal resistance, (R _{θJB})	64.3	°C/W
Junction to top characterization parameter, (Ψ _{JT})	31.8	°C/W
Junction to board characterization parameter, (Ψ _{JB})	58.0	°C/W
Junction to case (bottom) thermal resistance, (R _{θJcbot})	5.9	°C/W

6/ Voltage values are with respect to the SW terminal.

7/ This voltage should be applied for less than 30% of the repetitive period.

8/ For more information about traditional and new thermal metrics, see manufacturer's datasheet.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
- JEESD22-C101 – Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC JEP 155 – Recommended ESD Target Levels for HBM/MM Qualification
- JEDEC JEP 157 – Recommended ESD-CDM Target Levels

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/ 2/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Supply Current						
V5IN supply current, in S0	IV5IN(S0)	T _J = 25°C, No load, V _{S3} = V _{S5} = 5 V		590		μA
V5IN supply current, in S3	IV5IN(S3)	T _J = 25°C, No load, V _{S3} = 0 V, V _{S5} = 5 V		500		μA
V5IN shutdown current	IV5INSDN	T _J = 25°C, No load, V _{S3} = V _{S5} = 0 V			1	μA
VLDOIN supply current, in S0	IVLDOIN(S0)	T _J = 25°C, No load, V _{S3} = V _{S5} = 5 V			5	μA
VLDOIN supply current, in S3	IVLDOIN(S3)	T _J = 25°C, No load, V _{S3} = 0 V, V _{S5} = 5 V			5	μA
VLDOIN shutdown current	IVLDOINSDN	T _J = 25°C, No load, V _{S3} = V _{S5} = 0 V			5	μA
VREF Output						
Output voltage	VVREF	IVREF = 30 μA, T _J = 25°C		1.80		V
		0 μA ≤ IVREF < 300 μA, T _J = -55°C to 125°C	1.782		1.818	
Current limit	IVREFOCL	VVREF = 1.7 V	0.4	0.8		mA
VTTREF Output						
Output voltage	VVTTREF			VVDDQSNS/2		V
Output voltage tolerance to VVDDQ	VVTTREF	IVTTREF < 100 μA, 1.2 V ≤ VVDDQSNS ≤ 1.8 V	49.2%		50.8%	
		IVTTREF < 10 mA, 1.2 V ≤ VVDDQSNS ≤ 1.8 V	49%		51%	
Source current limit	IVTTREFOCLSRC	VVDDQSNS = 1.8 V, VVTTREF = 0 V	10	18		mA
Sink current limit	IVTTREFOCLSNK	VVDDQSNS = 1.8 V, VVTTREF = 1.8 V	10	17		mA
VTTREF discharge current	IVTTREFDIS	T _J = 25°C, V _{S3} = V _{S5} = 0 V, VVTTREF = 0.5 V	0.8	1.3		mA
VTT Output						
Output voltage				VVTTREF		V
Output voltage tolerance to VTTREF	VVTTTOL	IVTT ≤ 10 mA, 1.2 V ≤ VVDDQSNS ≤ 1.8 V, IVTTREF = 0 A	-20		20	mV
		IVTT ≤ 1 A, 1.2 V ≤ VVDDQSNS ≤ 1.8 V, IVTTREF = 0 A	-30		30	
		IVTT ≤ 2 A, 1.4 V ≤ VVDDQSNS ≤ 1.8 V, IVTTREF = 0 A	-40		40	
		IVTT ≤ 1.5 A, 1.2 V ≤ VVDDQSNS ≤ 1.4 V, IVTTREF = 0 A	-40		40	
Source current limit	IVTTOCLSRC	VVDDQSNS = 1.8 V, VVTT = VVTTSENS = 0.7 V, IVTTREF = 0 A	2	3		A
Sink current limit	IVTTOCLSNK	VVDDQSNS = 1.8 V, VVTT = VVTTSENS = 1.1 V, IVTTREF = 0 A	2	3		A

See footnote at end of table.

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ABLE I. Electrical performance characteristics - Continuous. 1/ 2/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
VTT Output – continued.						
Leakage current	IVTTLK	T _J = 25°C, V _{S3} = 0 V, V _{S5} = 5 V, V _{VTT} = V _{VTTREF}			5	μA
VTTSENS input bias current	IVTTSNSBIAS	V _{S3} = 5 V, V _{S5} = 5 V, V _{VTTSENS} = V _{VTTREF}	-0.5	0.0	0.5	μA
VTTSENS leakage current	IVTTSNSLK	V _{S3} = 0 V, V _{S5} = 5 V, V _{VTTSENS} = V _{VTTREF}	-1	0	1	μA
VTT Discharge current	IVTTDIS	T _J = 25°C, V _{S3} = V _{S5} = 0 V, V _{VDDQSNS} = 1.8 V, V _{VTT} = 0.5 V, I _{VTTREF} = 0 A		7.8		mA
VDDQ Output						
VDDQ sense voltage	V _{VDDQSNS}			V _{REFIN}		
VDDQSNS regulation voltage tolerance to REFIN	V _{VDDQSNSTOL}	T _J = 25°C	-3		3	mV
VDDQSNS input current	I _{VDDQSNS}	V _{VDDQSNS} = 1.8 V		39		μA
REFIN input current	I _{REFIN}	V _{REFIN} = 1.8 V	-0.1	0.0	0.1	μA
VDDQ discharge current	I _{VDDQDIS}	V _{S3} = V _{S5} = 0 V, V _{VDDQSNS} = 0.5 V, MODE pin pulled down to GND through 47 kΩ (Non-tracking)		12		mA
VLDOIN discharge current	I _{VLDOINDIS}	V _{S3} = V _{S5} = 0 V, V _{VDDQSNS} = 0.5 V, MODE pin pulled down to GND through 100 kΩ (Non-tracking)		1.2		A
Switch Mode Power Supply (SMPS) Frequency						
VDDQ switching frequency	f _{SW}	V _{IN} = 5 V, V _{VDDQSNS} = 1.8 V, R _{MODE} = 100 kΩ		300		kHz
		V _{IN} = 5 V, V _{VDDQSNS} = 1.8 V, R _{MODE} = 200 kΩ		400		
Minimum on time	t _{ON(min)}	DRVH rising to falling 3/		60		ns
Minimum off time	t _{OFF(min)}	DRVH falling to rising	200	320	450	ns
VDDQ MOSFET Driver						
DRVH resistance	R _{DRVH}	Source, I _{DRVH} = -50 mA		1.6	3.0	Ω
		Sink, I _{DRVH} = 50 mA		0.6	1.5	
DRVH resistance	R _{DRVH}	Source, I _{DRVH} = -50 mA		0.9	2.0	Ω
		Sink, I _{DRVH} = 50 mA		0.5	1.2	
Dead time	t _{DEAD}	DRVH-off to DRVH-on		10		ns
		DRVH-off to DRVH-on		20		

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continuous. 1/ 2/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Internal Boot Strap SW						
Forward voltage	VFBST	V _{V5IN-VBST} , T _J = 25°C, I _F = 10 mA		0.1	0.2	V
VBST leakage current	IVBSTLK	T _J = 25°C, V _{VBST} = 33 V, V _{SW} = 28 V		0.01	1.5	µA
Logic Threshold						
MODE source current	IMODE		14	15	16	µA
MODE threshold voltage	VTHMODE	MODE 0	580	600	620	mV
		MODE 1	829	854	879	
		MODE 2	1202	1232	1262	
		MODE 3	1760	1800	1840	
S3/S5 low-level voltage	V _{IL}				0.5	V
S3/S5 high-level voltage	V _{IH}		1.8			V
S3/S5 hysteresis voltage	V _{IHYST}			0.25		V
S3/S5 input leak current	V _{ILK}		-1	0	1	µA
Soft Start						
VDDQ soft-start time	t _{SS}	Internal soft-start time, C _{VREF} = 0.1 µF, S5 rising to V _{VDDQSNS} > 0.99 × V _{REFIN}		1.1		ms
PGOOD Comparator						
VDDQ PGOOD threshold	VTHPG	PGOOD in from higher	106%	108%	110%	
		PGOOD in from lower	90%	92%	94%	
		PGOOD out to higher	114%	116%	118%	
		PGOOD out to lower	82%	84%	86%	
PGOOD sink current	I _{PG}	V _{PGOOD} = 0.5 V	3	5.9		mA
PGOOD delay time	t _{PGDLY}	Delay for PGOOD in	0.8	1	1.2	ms
		Delay for PGOOD out, with 100 mV over drive		330		ns
PGOOD start-up delay	t _{PGSSDLY}	C _{VREF} = 0.1 µF, S5 rising to PGOOD rising		2.5		ms

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continuous. 1/ 2/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Protections						
TRIP source current	ITRIP	T _J = 25°C, V _{TRIP} = 0.4 V	9	10	11	μA
TRIP source current temperature coefficient	TCITRIP			4700		ppm/°C
VTRIP voltage range	VTRIP		0.2		3	V
Current limit threshold	VOCL	VTRIP = 3.0 V	360	375	390	mV
		VTRIP = 1.6 V	190	200	210	
		VTRIP = 0.2 V	20	25	30	
Negative current limit threshold	VOCLN	VTRIP = 3.0 V	-390	-375	-360	mV
		VTRIP = 1.6 V	-210	-200	-190	
		VTRIP = 0.2 V	-30	-25	-20	
Zero cross detection offset	VZC			0		mV
V5IN UVLO threshold voltage	VUVLO	Wake-up	4.2	4.4	4.5	V
		Shutdown	3.7	3.9	4.1	
VDDQ OVP threshold voltage	VOVP	OVP detect voltage	118%	120%	122%	
VDDQ OVP propagation delay	tOVDPDY	With 100 mV over drive		430		ns
VDDQ UVP threshold voltage	VUVP	UVP detect voltage	66%	66%	70%	
VDDQ UVP delay	tUVPDY			1		ms
VDDQ UVP enable delay	tUVPENDLY			1.2		ms
OOB threshold voltage	VOOB			108%		
Thermal Shutdown						
Thermal shutdown threshold	TSDN	Shutdown temperature <u>4/</u>		140		°C
		Hysteresis <u>4/</u>		10		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ T_J = -55°C to 125°C, V_{V5IN} = 5 V, VLDOIN is connected to VDDQ output, V_{MODE} = 0 V, V_{S3} = V_{S5} = 5 V (unless otherwise noted).

3/ Guaranteed by design, not subject to production test.

4/ See section 1.3 for absolute maximum and minimum recommended operating conditions.

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Case X

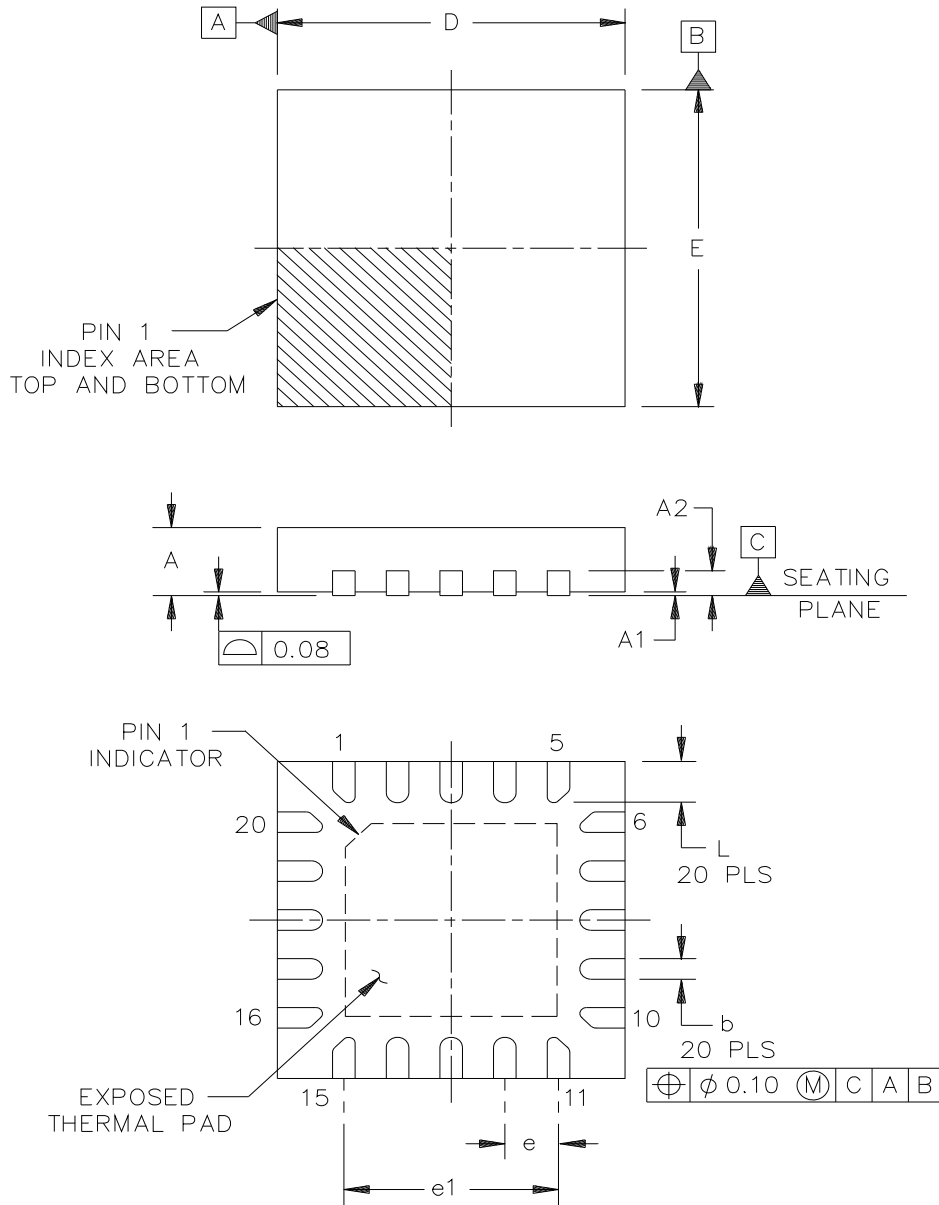


FIGURE 1. Case outline.

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/16601</p>
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Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.70	0.80	D/E	2.90	3.10
A1	0.00	0.50	e	0.40 BSC	
A2	0.20 REF		e1	1.60 BSC	
b	0.15	0.25	L	0.30	0.50

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the board for thermal and mechanical performance.
4. See the addition figure in the manufacturer data sheet for details regarding the exposed thermal pad features and dimensions.
5. Falls within JEDEC MO-220.

FIGURE 1. Case outline - Continued.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VTTSENS	11	DRV L
2	VLDOIN	12	V5IN
3	VTT	13	SW
4	VTTGND	14	DRVH
5	VTTREF	15	VBST
6	VREF	16	S5
7	GND	17	S3
8	REFIN	18	TRIP
9	VDDQSNS	19	MODE
10	PGND	20	PGOOD

FIGURE 2. Terminal connections.

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PIN		I/O	Description
Name	No.		
DRVH	14	O	High-side MOSFET gate driver output
DRVL	11	O	Low-side MOSFET gate driver output.
GND	7		Signal ground.
MODE	19	I	Connect resistor to GND to configure switching frequency and discharge mode.
PGND	10		Gate driver power ground. RDS(on) current sensing input (+).
PGOOD	20	O	Powergood signal open drain output. PGOOD goes high when VDDQ output voltage is within the target range.
REFIN	8	I	Reference input for VDDQ. Connect to the midpoint of a resistor divider from VREF to GND. Add a capacitor for stable operation
SW	13	I/O	High-side MOSFET gate driver return. RDS(on) current sensing input (-).
S3	17	I	S3 signal input.
S5	16	I	S5 signal input.
TRIP	18	I	Connect resistor to GND to set OCL at $V_{TRIP} / 8$. Output 10 μ A current at room temperature, $T_C = 4700$ ppm/ $^{\circ}$ C.
VBST	15	I	High-side MOSFET gate driver bootstrap voltage input. Connect a capacitor from the VBST pin to the SW pin.
VDDQSNS	9	I	VDDQ output voltage feedback. Reference input for VTTREF. Also serves as power supply for VTTREF.
VLDOIN	2	I	Power supply input for VTT LDO. Connect VDDQ in typical application.
VREF	6	O	1.8-V reference output.
VTT	3	O	VTT 2-A LDO output. Need to connect 10 μ F or larger capacitance for stability.
VTTGND	4		Power ground for VTT LDO.
VTTREF	5	O	Buffered VTT reference output. Need to connect 0.22 μ F or larger capacitance for stability.
VTTSENS	1	I	VTT output voltage feedback
V5IN	12	I	5 V power supply input for internal circuits and MOSFET gate drivers.
Thermal pad			Connect to GND

FIGURE 3. Terminal function.

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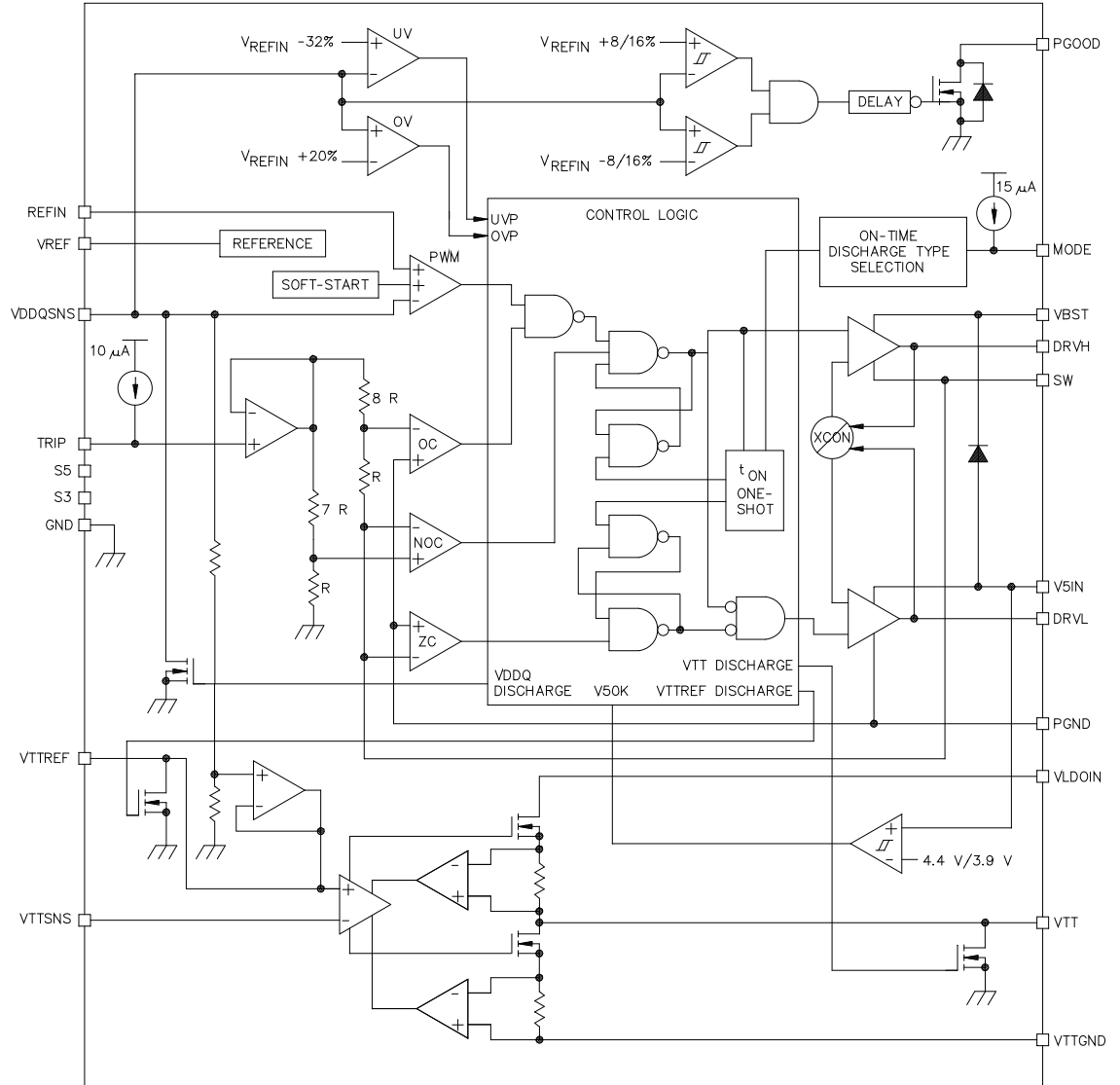


FIGURE 4. Functional block diagram.

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/16601</p>
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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/16601-01XE	01295	51216M	TPS51216MRUKREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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