

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 36 V single supply general purpose operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/15605</u>	-	<u>01</u>	X	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	OPA2171-EP	36 V single supply general purpose operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MO-187-CA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_S) ± 20 V minimum
 Signal input pins:
 Voltage $-V_S - 0.5$ V to $+V_S + 0.5$ V
 Current -10 mA to + 10 mA
 Output short circuit Continuous 2/
 Junction temperature range (T_J) +150°C
 Storage temperature range (T_{STG}) -65°C to +150°C
 Electrostatic discharge (ESD):
 Human body model (HBM) ± 4000 V 3/
 Charged device model (CDM) ± 750 V 4/

1.4 Recommended operating conditions. 5/

Supply voltage (V_S) 4.5 V (± 2.25 V) to 36 V (± 18 V)
 Operating temperature range (T_A) -55°C to +125°C

1.5 Thermal characteristics. 6/

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	175.2	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	74.9	°C/W
Thermal resistance, junction-to-board	θ_{JB}	22.2	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	1.6	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	22.8	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	N/A	°C/W

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Short circuit to ground, one amplifier per package.
- 3/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- 4/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
- 5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 6/ For more information about traditional and new thermal metrics, see integrated circuit package thermal metrics application report, SPRA953.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC JEP 155 - Recommended ESD Target Levels for HBM/MM Qualification
- JEDEC JEP 157 - Recommended ESD-CDM Target Levels

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Offset voltage							
Input offset voltage	V _{OS}		+25°C	01		±1.8	mV
			-55°C to +125°C		0.25 typical		
						±2	
					0.3 typical		
Input offset voltage drift	$\Delta V_{OS} / \Delta T$		-55°C to +125°C	01	0.3 typical		$\mu\text{V} / ^\circ\text{C}$
Input offset voltage versus power supply	PSRR	V _S = 4 V to 36 V	-55°C to +125°C	01		±5	$\mu\text{V}/\text{V}$
					1 typical		
Channel separation, dc		dc	+25°C	01	5 typical		$\mu\text{V}/\text{V}$
Input bias current							
Input bias current	I _B		+25°C	01		±15	pA
			-55°C to +125°C		±8 typical		
							±4
Input offset current	I _{OS}		+25°C	01	±4 typical		pA
			-55°C to +125°C			±4	nA
Noise							
Input voltage noise		f = 0.1 Hz to 10 Hz	+25°C	01	3 typical		μV_{PP}
Input voltage noise density	e _n	f = 100 Hz	+25°C	01	25 typical		$\text{nV} / \sqrt{\text{Hz}}$
		f = 1 kHz			14 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Input voltage							
Common mode voltage range <u>3/</u>	V _{CM}		+25°C	01	-V _S - 0.1	+V _S - 2	V
Common mode rejection ratio	CMRR	V _S = ±2 V, -V _S - 0.1 V < V _{CM} < +V _S - 2 V	+25°C	01	104 typical		dB
			-55°C to +125°C		87		
		V _S = ±18 V, -V _S - 0.1 V < V _{CM} < +V _S - 2 V	+25°C		120 typical		
			-55°C to +125°C		104		
Input impedance							
Differential		<u>4/</u>	+25°C	01	100 3 typical		MΩ pF
Common mode		<u>4/</u>	+25°C	01	6 3 typical		10 ¹² Ω pF
Open loop gain							
Open loop voltage gain	AOL	V _S = 4 V to 36 V, -V _S + 0.35 V < V _O < +V _S - 0.35 V	+25°C	01	130 typical		dB
			-55°C to +125°C		110		
Frequency response							
Gain bandwidth product	GBP		+25°C	01	3.0 typical		MHz
Slew rate	SR	G = +1	+25°C	01	1.5 typical		V/μs
Settling time	t _S	To 0.1%, V _S = ±18 V, G = +1, 10 V step	+25°C	01	6 typical		μs
		To 0.01% (12 bit), V _S = ±18 V, G = +1, 10 V step			10 typical		
Overload recovery time		V _{IN} x Gain > V _S	+25°C	01	2 typical		μs
Total harmonic distortion + noise	THD + N	Gain = + 1, f = 1 kHz, V _O = 3 V _{RMS}	+25°C	01	0.0002 typical		%

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Output							
Voltage output swing from rail	V _O	V _S = 5 V, R _L = 10 kΩ	+25°C	01	30 typical		mV
		R _L = 10 kΩ, A _{OL} ≥ 110 dB	-55°C to +125°C		-V _S + 0.35	+V _S - 0.35	V
Short circuit current	I _{SC}		+25°C	01	+25/-35 typical		mA
Open loop output resistance	R _O	f = 1 MHz, I _O = 0 A	+25°C	01	150 typical		Ω
Power supply							
Specified voltage range	V _S		+25°C	01	2.7	36	V
Quiescent current per amplifier	I _Q	I _O = 0 A	+25°C	01		595	μA
					475 typical		
			-55°C to +125°C			650	
Temperature							
Operating temperature				01	-55	+125	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_S = 2.7 V to 3.6 V, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2.

3/ The input range can be extended beyond +V_S - 2 V up to +V_S. See typical characteristics and application and implementation in the manufacturer's datasheet for more additional information.

4/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

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Case X

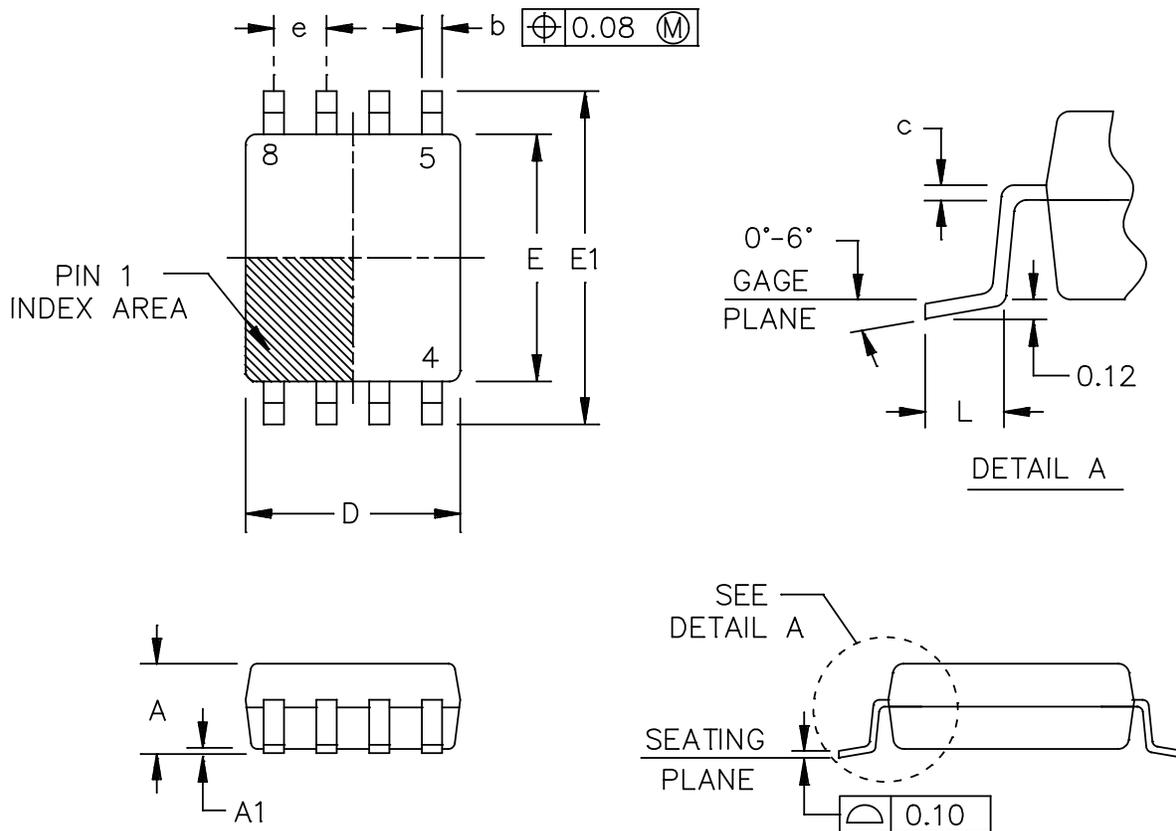


FIGURE 1. Case outline.

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/15605</p>
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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.023	.035	0.60	0.90
A1	.000	.003	0.00	0.10
b	.006	.009	0.17	0.25
c	.005 NOM		0.13 NOM	
D	.074	.082	1.90	2.10
E	.086	.094	2.20	2.40
E1	.118	.125	3.00	3.20
e	.019 BSC		0.50 BSC	
L	.007	.013	0.20	0.35

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm (.005 inch) per side.
3. Falls with JEDEC MO-187 variation CA.

FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	OUTPUT A	Output, channel A.
2	-INPUT A	Inverting input, channel A.
3	+INPUT A	Noninverting input, channel A.
4	-V _S	Negative (lowest) power supply.
5	+INPUT B	Noninverting input, channel B.
6	-INPUT B	Inverting input, channel B.
7	OUTPUT B	Output, channel B.
8	+V _S	Positive (highest) power supply.

FIGURE 2. Terminal connections.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/15605-01XE	01295	ZGAA	OPA2171-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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