REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add JEDEC references to paragraphs 1.3 and 2. Add I/O column to figure 2 Terminal connections. Make correction to Vendor part number as specified in paragraph 6.3. Update document paragraphs to current requirements. - ro	21-03-18	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	REV		A	A	A	A	A	A	A	A	A	A	A								
	PAGE		1	2	3	4	5	6	7	8	9	10	11								

PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime
Original date of drawing YY-MM-DD 15-10-20	CHECKED BY RAJESH PITHADIA APPROVED BY CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, 36 V SINGLE SUPPLY GENERAL PURPOSE OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	SIZE: A CODE IDENT. NO.: 16236	DWG NO. V62/15605
	REV A	PAGE 1 OF 11

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V109-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 36 V single supply general purpose operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/15605	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	OPA2171-EP	36 V single supply general purpose operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MO-187-CA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_S) ..... ±20 V minimum
Signal input pins:
  Voltage ..... $-V_S$ – 0.5 V to $+V_S$ + 0.5 V
  Current ..... -10 mA to + 10 mA
Output short circuit ..... Continuous 2/
Junction temperature range (T_J) ..... +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Electrostatic discharge (ESD):
  Human body model (HBM), per JEDEC JS-001 ..... ±4000 V 3/
  Charged device model (CDM), per JEDEC JESD22-C101 ..... ±750 V 4/

1.4 Recommended operating conditions. 5/

Supply voltage (V_S) ..... 4.5 V (±2.25 V) to 36 V (±18 V)
Operating temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics. 6/

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	175.2	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	74.9	°C/W
Thermal resistance, junction-to-board	θ_{JB}	22.2	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	1.6	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	22.8	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	N/A	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Short circuit to ground, one amplifier per package.

3/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

4/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

6/ For more information about traditional and new thermal metrics, see integrated circuit package thermal metrics application report, SPRA953.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JEDEC/JESD22-C101	–	Qualification Testing for Plastic Encapsulated Solid State Devices
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Offset voltage							
Input offset voltage	V_{OS}		+25°C	01		±1.8	mV
					0.25 typical		
			-55°C to +125°C			±2	
					0.3 typical		
Input offset voltage drift	$\Delta V_{OS} / \Delta T$		-55°C to +125°C	01	0.3 typical		µV /°C
Input offset voltage versus power supply	PSRR	V_S = 4 V to 36 V	-55°C to +125°C	01		±5	µV/V
					1 typical		
Channel separation, dc		dc	+25°C	01	5 typical		µV/V
Input bias current							
Input bias current	I_B		+25°C	01		±15	pA
					±8 typical		
			-55°C to +125°C			±4	nA
Input offset current	I_{OS}		+25°C	01	±4 typical		pA
			-55°C to +125°C			±4	nA
Noise							
Input voltage noise		f = 0.1 Hz to 10 Hz	+25°C	01	3 typical		μV_{PP}
Input voltage noise density	en	f = 100 Hz	+25°C	01	25 typical		nV / $\sqrt{Hz}$
		f = 1 kHz			14 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Input voltage							
Common mode 3/ voltage range	V_{CM}		+25°C	01	$-V_S$ - 0.1	$+V_S$ - 2	V
Common mode rejection ratio	CMRR	V_S = ±2 V,	+25°C	01	104 typical		dB
		$-V_S$ – 0.1 V < V_{CM} < $+V_S$ – 2 V	-55°C to +125°C		87		
		V_S = ±18 V,	+25°C		120 typical		
		$-V_S$ – 0.1 V < V_{CM} < $+V_S$ – 2 V	-55°C to +125°C		104		
Input impedance							
Differential		4/	+25°C	01	100||3 typical		MΩ||pF
Common mode		4/	+25°C	01	6||3 typical		10^{12}Ω||pF
Open loop gain							
Open loop voltage gain	A_{OL}	V_S = 4 V to 36 V,	+25°C	01	130 typical		dB
		$-V_S$ + 0.35 V < V_O < $+V_S$ – 0.35 V	-55°C to +125°C		110		
Frequency response							
Gain bandwidth product	GBP		+25°C	01	3.0 typical		MHz
Slew rate	SR	G = +1	+25°C	01	1.5 typical		V/μs
Settling time	t_S	To 0.1%, V_S = ±18 V, G = +1, 10 V step	+25°C	01	6 typical		μs
		To 0.01% (12 bit), V_S = ±18 V, G = +1, 10 V step			10 typical		
Overload recovery time		V_{IN} x Gain > V_S	+25°C	01	2 typical		μs
Total harmonic distortion + noise	THD + N	Gain = + 1, f = 1 kHz, V_O = 3 V_{RMS}	+25°C	01	0.0002 typical		%

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Output							
Voltage output swing from rail	V_O	V_S = 5 V, R_L = 10 kΩ	+25°C	01	30 typical		mV
		R_L = 10 kΩ, A_{OL} ≥ 110 dB	-55°C to +125°C		-V_S + 0.35	+V_S – 0.35	V
Short circuit current	I_{SC}		+25°C	01	+25/-35 typical		mA
Open loop output resistance	R_O	f = 1 MHz, I_O = 0 A	+25°C	01	150 typical		Ω
Power supply							
Specified voltage range	V_S		+25°C	01	2.7	36	V
Quiescent current per amplifier	I_Q	I_O = 0 A	+25°C	01		595	μA
					475 typical		
			-55°C to +125°C			650	
Temperature							
Operating temperature				01	-55	+125	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_S = 2.7 V to 3.6 V, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2.

3/ The input range can be extended beyond +V_S – 2 V up to +V_S. See typical characteristics and application and implementation in the manufacturer's datasheet for more additional information.

4/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

Case X

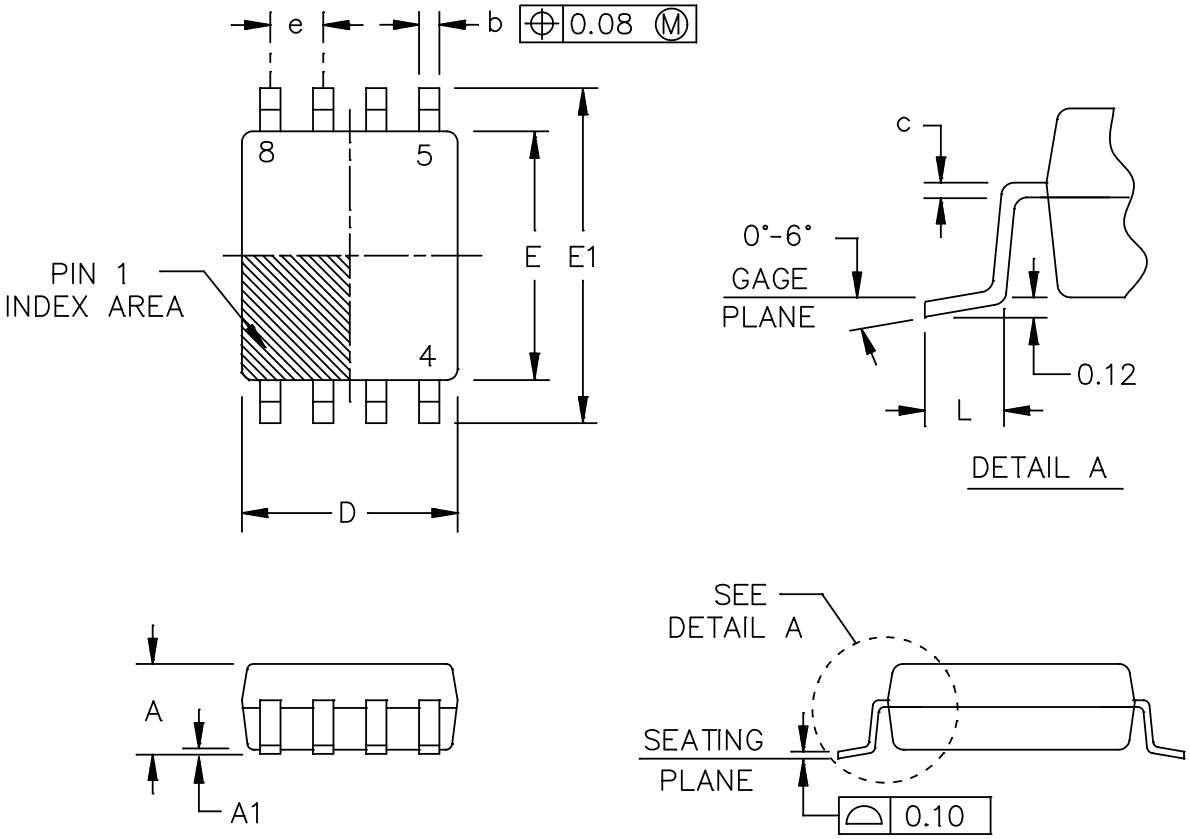

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/15605
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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.024	.035	0.60	0.90
A1	.000	.003	0.00	0.10
b	.007	.010	0.17	0.25
c	.005 NOM		0.13 NOM	
D	.075	.083	1.90	2.10
E	.087	.094	2.20	2.40
E1	.118	.126	3.00	3.20
e	.020 BSC		0.50 BSC	
L	.008	.014	0.20	0.35

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm (.006 inch) per side.
3. Falls with JEDEC MO-187 variation CA.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	OUTPUT A	O	Output, channel A.
2	-INPUT A	I	Inverting input, channel A.
3	+INPUT A	I	Noninverting input, channel A.
4	$-V_S$	---	Negative (lowest) power supply.
5	+INPUT B	I	Noninverting input, channel B.
6	-INPUT B	I	Inverting input, channel B.
7	OUTPUT B	O	Output, channel B.
8	$+V_S$	---	Positive (highest) power supply.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/15605-01XE	01295	ZGAA	OPA2171MDCUTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243