REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update JEDEC package from M0-187-AA-T to MO-187. Add limits to paragraph 1.4. Add JEDEC references to paragraph 1.3 and section 2. Make change to the L1 dimension as specified under Figure 1. Update document paragraphs to current requirements. - ro	21-03-11	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV																						
PAGE																						
REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A										
	PAGE		1	2	3	4	5	6	7	8	9	10										

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 15-09-21	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, 100 V INPUT, 50 mA, HIGH VOLTAGE LINEAR REGULATOR, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/15603**
	REV **A**	**PAGE** 1 **OF** 10

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 100 V input voltage, 50 mA, high voltage linear regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/15603	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS7A4001-EP	100 V input voltage, 50 mA, high voltage linear regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MO-187	Plastic small outline with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage:
- IN pin to GND pin ..... -0.3 V to 102 V
- OUT pin to GND pin ..... -0.3 V to 102 V
- OUT pin to IN pin ..... -102 V to 0.3 V
- FB pin to GND pin ..... -0.3 V to 2 V
- FB pin to IN pin ..... -102 V to 0.3 V
- EN pin to IN pin ..... -102 V to 0.3 V
- EN pin to GND pin ..... 0.3 V to 102 V

Current :
- Peak output ..... Internally limited

Operating virtual junction temperature range (T_J) ..... -55°C to +150°C

Storage temperature range (T_{STG}) ..... -65°C to +150°C

Electrostatic discharge (ESD) :
- Human body model (HBM) per JEDEC JS-001 ..... ±2500 V 2/
- Charged device model (CDM) per JEDEC JESD 22-C101 ..... ±500 V 3/

1.4 Recommended operating conditions. 4/

Input voltage (VIN) ..... 7 V to 100 V
Output voltage (VOUT) ..... 1.161 V to 90 V
Enable pin voltage (VEN) ..... 0 V to 100 V
Output voltage (IOUT) ..... 0 mA to 50 mA
Operating junction temperature range (T_J) ..... -55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	66.7	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	54.1	°C/W
Thermal resistance, junction-to-board	θ_{JB}	38.1	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	2	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	37.8	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	15.5	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ JEDEC document JEP155 states that 500 V HDM allows safe manufacturing with a standard ESD control process.

3/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
EIA/JESD 22	–	Qualification Testing for Plastic Encapsulated Solid State Devices
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Input voltage range	V_{IN}		-55°C to +125°C	01	7.0	100.0	V
Internal reference	V_{REF}	$V_{FB} = V_{REF}$, V_{IN} = 9 V, I_{OUT} = 25 mA	+25°C	01	1.173 typical		V
					1.161	1.173	
Output voltage range 3/	V_{OUT}	$V_{IN} \geq V_{OUT(NOM)}$ + 2.0 V	-55°C to +125°C	01	V_{REF}	90	V
Nominal accuracy	V_{OUT}	V_{IN} = 9 V, I_{OUT} = 25 mA	+25°C	01	-1.0	+1.0	$\%V_{OUT}$
Overall accuracy	V_{OUT}	$V_{OUT(NOM)}$ + 2.0 V ≤ V_{IN} ≤ 24 V 4/ 100 μA ≤ I_{OUT} ≤ 50 mA	-55°C to +125°C	01	-2.7	+2.7	$\%V_{OUT}$
Line regulation	$\Delta\%V_{OUT}/\Delta V_{IN}$	7 V ≤ V_{IN} ≤ 100 V	-55°C to +125°C	01	0.03 typical		$\%V_{OUT}$
Load regulation	$\Delta\%V_{OUT}/\Delta I_{OUT}$	100 μA ≤ I_{OUT} ≤ 50 mA	-55°C to +125°C	01	0.31 typical		$\%V_{OUT}$
Dropout voltage	V_{DO}	V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 20 mA	-55°C to +125°C	01	290 typical		mV
		V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 50 mA			0.78 typical		V
						1.3	
Current limit	I_{LIM}	V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 7.0 V	≤ +85°C	01	146 typical		mA
					51	207	
		V_{OUT} = 90%, $V_{OUT(NOM)}$, V_{IN} = 9.0 V	-55°C to +125°C		165 typical		
					51	220	
Ground current	I_{GND}	7 V ≤ V_{IN} ≤ 100 V, I_{OUT} = 0 mA	-55°C to +125°C	01	25 typical		μA
						65	
		I_{OUT} = 50 mA			25 typical		
Shutdown supply current	I_{SHDN}	V_{EN} = 4.0 V	-55°C to +125°C	01	4.1 typical		μA
						20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Feedback current 5/	I_{FB}		-55°C to +125°C	01	0.01 typical		µA
					-0.1	0.1	
Enable current	I_{EN}	7 V ≤ V_{IN} ≤ 100 V, V_{IN} = V_{EN}	-55°C to +125°C	01	0.02 typical		µA
						1.0	
Enable high level voltage	V_{EN_HI}		-55°C to +125°C	01	1.5	V_{IN}	V
Enable low level voltage	V_{EN_LO}		-55°C to +125°C	01	0	0.4	V
Output noise voltage	V_{NOISE}	V_{IN} = 12 V, C_{OUT} = 10 µF, $V_{OUT(NOM)}$ = V_{REF}, BW = 10 Hz to 100 kHz	-55°C to +125°C	01	58 typical		µVRMS
		V_{IN} = 12 V, C_{OUT} = 10 µF, $V_{OUT(NOM)}$ = 5 V, BW = 10 Hz to 100 kHz, C_{BYP} = 10 nF 6/			73 typical		
Power supply rejection ratio	PSRR	V_{IN} = 12 V, C_{OUT} = 10 µF, $V_{OUT(NOM)}$ = 5 V, f = 100 Hz, C_{BYP} = 10 nF 6/	-55°C to +125°C	01	65 typical		dB
Thermal shutdown temperature	T_{SD}	Shutdown, temperature increasing		01	+170 typical		°C
		Reset, temperature decreasing			+150 typical		
Operating junction temperature range	T_J			01	-55	+125	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{IN} = $V_{OUT(NOM)}$ + 2.0 V or V_{IN} = 7.0 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF and FB tied to OUT.

3/ To ensure stability at no load conditions, a current from the feedback resistive network greater than or equal to 10 µA is required.

4/ Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P \approx (V_{IN} - V_{OUT}) \times I_{OUT} = (24\ V - V_{REF}) \times 50\ mA \approx 1.14\ W$). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.

5/ $I_{FB} > 0$ flows out of the device.

6/ C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

Case X

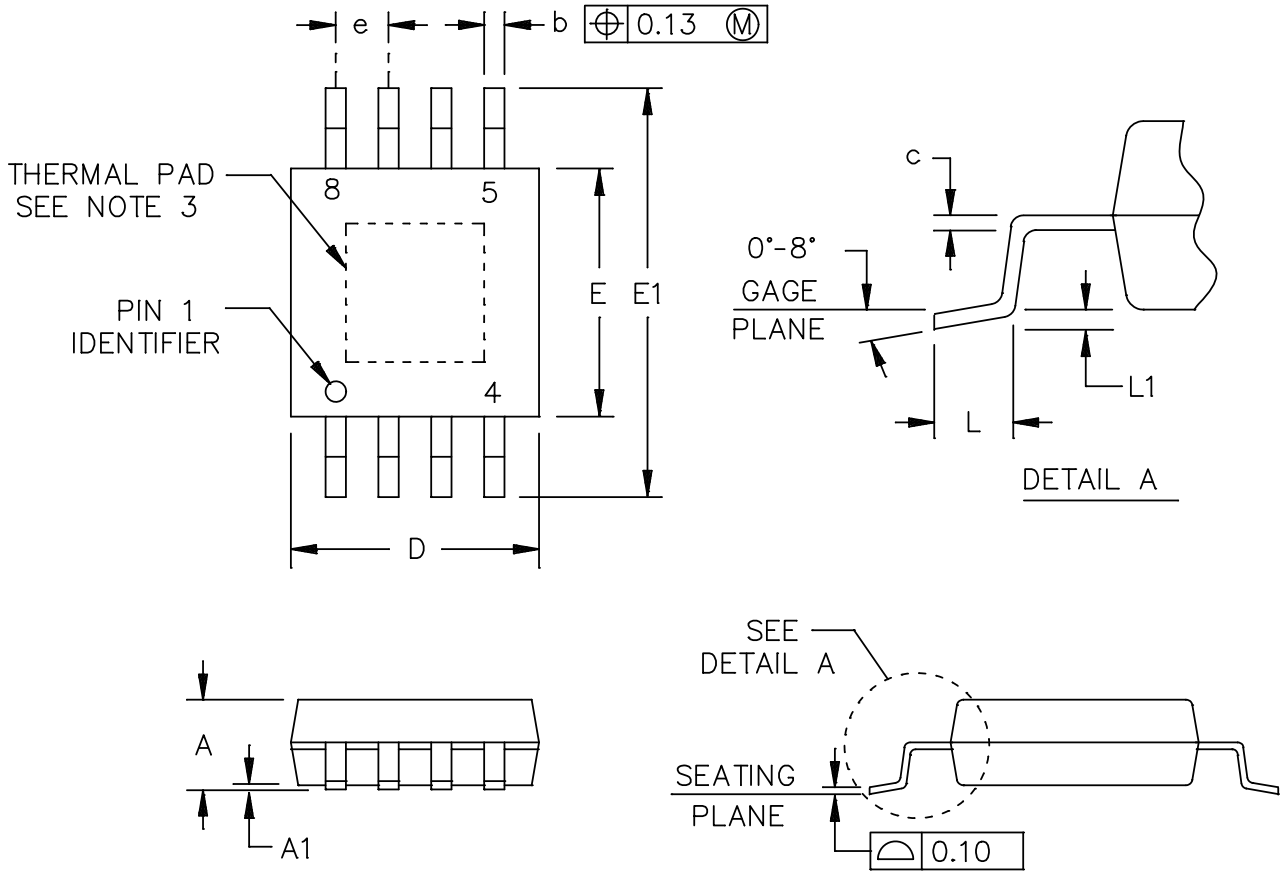

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/15603
		REV A	PAGE 7

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.043	---	1.10
A1	.002	.006	0.05	0.15
b	.010	.015	0.25	0.38
c	.005	.009	0.13	0.23
D	.114	.125	2.90	3.10
E	.114	.125	2.90	3.10
E1	.187	.199	4.75	5.05
e	0.025 BSC		0.65 BSC	
L	.016	.027	0.40	0.70
L1	.002	.006	0.05	0.15

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimension D does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (.006 inch) per end.
3. See the information in the product data sheet for detail regarding the exposed thermal pad features and dimensions.
4. Dimension E does not include interlead flash. Interlead flash shall not exceed 0.25 mm (0.010 inch) per side.
5. Falls with JEDEC MO-187.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I / O	Description
1	OUT	O	Regulator output. A capacitor > 4.7 μF must be tied from this pin to ground to assure stability.
2	FB	O	This pin the input to the control loop error amplifier. It is used to set the output voltage of the device.
3	NC	---	Not internally connected. This pin must be either be left open or tied to GND.
4	GND	---	Ground.
5	EN	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$, the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
6	NC	---	Not internally connected. This pin must be either be left open or tied to GND.
7	NC	---	Not internally connected. This pin must be either be left open or tied to GND.
8	IN	I	Input supply.
Thermal pad	---	---	Solder to printed circuit board (PCB) to enhanced thermal performance. Note that the thermal pad is internally connected to ground. Although it can be left floating, it is highly recommended to connect the thermal pad to the ground plane.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/15603-01XE	01295	ZFY4	TPS7A4001MDGNREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243