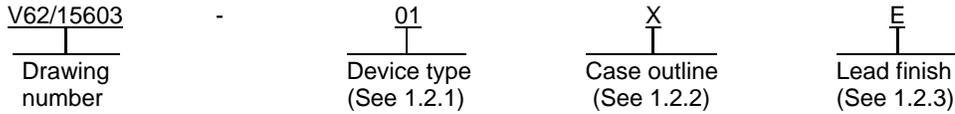


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 100 V input voltage, 50 mA, high voltage linear regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TPS7A4001-EP	100 V input voltage, 50 mA, high voltage linear regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MO-187-AA-T	Plastic small outline with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Voltage:

IN pin to GND pin	-0.3 V to 102 V
OUT pin to GND pin	-0.3 V to 102 V
OUT pin to IN pin	-102 V to 0.3 V
FB pin to GND pin	-0.3 V to 2 V
FB pin to IN pin	-102 V to 0.3 V
EN pin to IN pin	-102 V to 0.3 V
EN pin to GND pin	0.3 V to 102 V

Current :

Peak output	Internally limited
Operating virtual junction temperature range (T _J)	-55°C to +150°C
Storage temperature range (T _{STG})	-65°C to +150°C
Electrostatic discharge (ESD) :	
Human body model (HBM)	±2500 V 2/
Charged device model (CDM)	±500 V 3/

1.4 Recommended operating conditions. 4/

Operating junction temperature range (T _J)	-55°C to +125°C
--	-----------------

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ _{JA}	66.7	°C/W
Thermal resistance, junction-to-case (top)	θ _{JC(TOP)}	54.1	°C/W
Thermal resistance, junction-to-board	θ _{JB}	38.1	°C/W
Characterization parameter, junction-to-top	ψ _{JT}	2	°C/W
Characterization parameter, junction-to-board	ψ _{JB}	37.8	°C/W
Thermal resistance, junction-to-case (bottom)	θ _{JC(BOTTOM)}	15.5	°C/W

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ JEDEC document JEP155 states that 500 V HDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500 V HBM is possible with the necessary precautions.
- 3/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250 V CDM is possible with the necessary precautions.
- 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155 - Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 - Recommended ESD-CDM Target Levels

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _J	Device type	Limits		Unit	
					Min	Max		
Input voltage range	V _{IN}		-55°C to +125°C	01	7.0	100.0	V	
Internal reference	V _{REF}	V _{FB} = V _{REF} , V _{IN} = 9 V, I _{OUT} = 25 mA	+25°C	01	1.173 typical		V	
					1.161	1.173		
Output voltage range <u>3/</u>	V _{OUT}	V _{IN} ≥ V _{OUT(NOM)} + 2.0 V	-55°C to +125°C	01	V _{REF}	90	V	
Nominal accuracy	V _{OUT}	V _{IN} = 9 V, I _{OUT} = 25 mA	+25°C	01	-1.0	+1.0	%V _{OUT}	
Overall accuracy	V _{OUT}	V _{OUT(NOM)} + 2.0 V ≤ V _{IN} ≤ 24 V <u>4/</u> 100 μA ≤ I _{OUT} ≤ 50 mA	-55°C to +125°C	01	-2.7	+2.7	%V _{OUT}	
Line regulation	Δ%V _{OUT} / ΔV _{IN}	7 V ≤ V _{IN} ≤ 100 V	-55°C to +125°C	01	0.03 typical		%V _{OUT}	
Load regulation	Δ%V _{OUT} / ΔI _{OUT}	100 μA ≤ I _{OUT} ≤ 50 mA	-55°C to +125°C	01	0.31 typical		%V _{OUT}	
Dropout voltage	V _{DO}	V _{IN} = 17 V, V _{OUT(NOM)} = 18 V, I _{OUT} = 20 mA	-55°C to +125°C	01	290 typical		mV	
		V _{IN} = 17 V, V _{OUT(NOM)} = 18 V, I _{OUT} = 50 mA			0.78 typical			V
						1.3		
Current limit	I _{LIM}	V _{OUT} = 90% V _{OUT(NOM)} , V _{IN} = 7.0 V	≤ +85°C	01	146 typical		mA	
		V _{OUT} = 90%, V _{OUT(NOM)} , V _{IN} = 9.0 V	-55°C to +125°C		51	207		
				165 typical				
				51	220			
Ground current	I _{IGND}	7 V ≤ V _{IN} ≤ 100 V, I _{OUT} = 0 mA	-55°C to +125°C	01	25 typical		μA	
		I _{OUT} = 50 mA			65			
					25 typical			
Shutdown supply current	I _{SHDN}	V _{EN} = 4.0 V	-55°C to +125°C	01	4.1 typical		μA	
					20			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Feedback current <u>5/</u>	I _{FB}		-55°C to +125°C	01	0.01 typical		μA
					-0.1	0.1	
Enable current	I _{EN}	7 V ≤ V _{IN} ≤ 100 V, V _{IN} = V _{EN}	-55°C to +125°C	01	0.02 typical		μA
						1.0	
Enable high level voltage	V _{EN_HI}		-55°C to +125°C	01	1.5	V _{IN}	V
Enable low level voltage	V _{EN_LO}		-55°C to +125°C	01	0	0.4	V
Output noise voltage	V _{NOISE}	V _{IN} = 12 V, C _{OUT} = 10 μF, V _{OUT(NOM)} = V _{REF} , BW = 10 Hz to 100 kHz	-55°C to +125°C	01	58 typical		μV _{RMS}
		V _{IN} = 12 V, C _{OUT} = 10 μF, V _{OUT(NOM)} = 5 V, BW = 10 Hz to 100 kHz, C _{BYP} = 10 nF <u>6/</u>			73 typical		
Power supply rejection ratio	PSRR	V _{IN} = 12 V, C _{OUT} = 10 μF, V _{OUT(NOM)} = 5 V, f = 100 Hz, C _{BYP} = 10 nF <u>6/</u>	-55°C to +125°C	01	65 typical		dB
Thermal shutdown temperature	T _{SD}	Shutdown, temperature increasing		01	+170 typical		°C
		Reset, temperature decreasing			+150 typical		
Operating junction temperature range	T _J			01	-55	+125	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{IN} = V_{OUT(NOM)} + 2.0 V or V_{IN} = 7.0 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 μA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF and FB tied to OUT.

3/ To ensure stability at no load conditions, a current from the feedback resistive network greater than or equal to 10 μA is required.

4/ Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load

(P ≈ (V_{IN} - V_{OUT}) × I_{OUT} = (24 V - V_{REF}) × 50 mA ≈ 1.14 W). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.

5/ I_{FB} > 0 flows out of the device.

6/ C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

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Case X

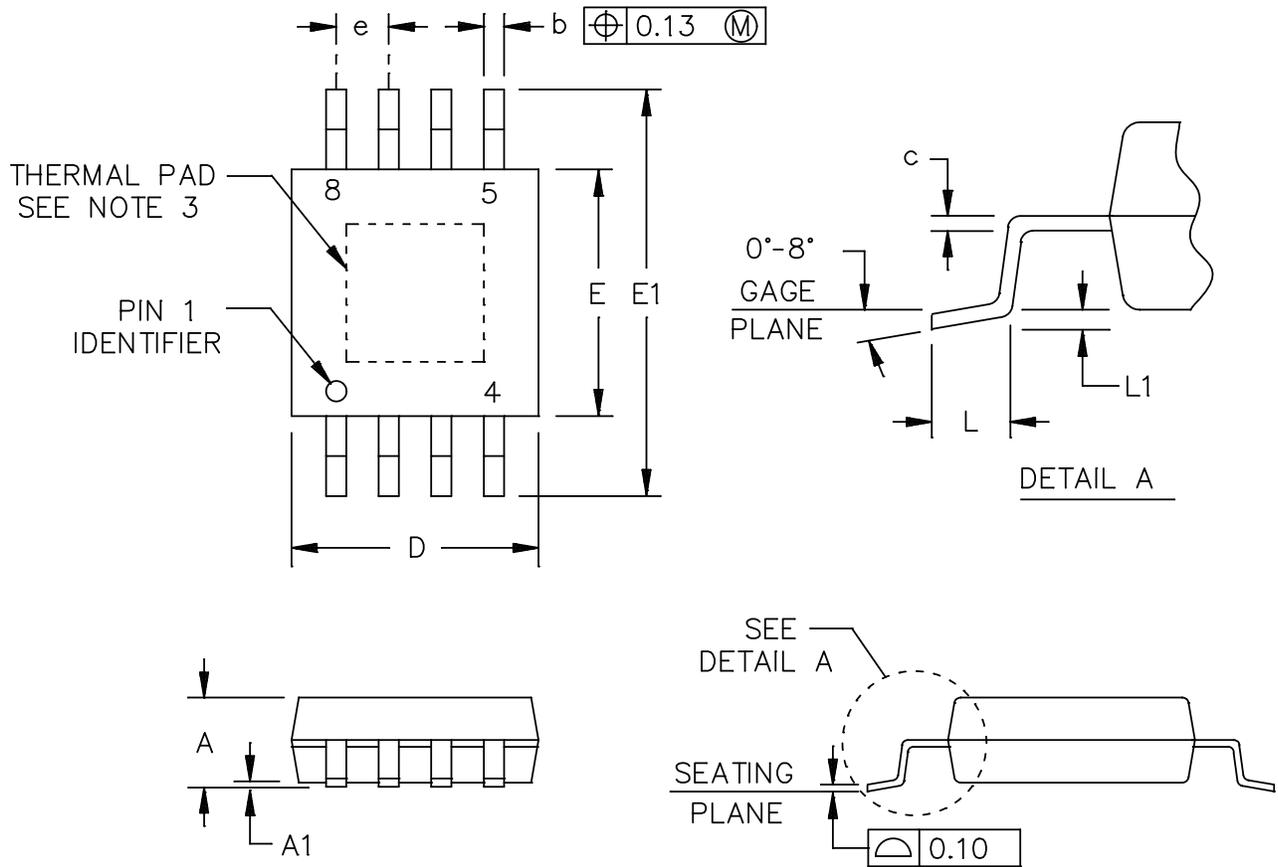


FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.043	---	1.10
A1	.001	.005	0.05	0.15
b	.009	.014	0.25	0.38
c	.005	.009	0.13	0.23
D	.114	.122	2.90	3.10
E	.114	.122	2.90	3.10
E1	.187	.198	4.75	5.05
e	0.025 BSC		0.65 BSC	
L	.015	.027	0.40	0.70
L1	.009 BSC		0.25 BSC	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion.
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, power pad thermally enhanced package, manufacturer literature number SLMA002 for information regarding recommended board layout. The datasheet is available from the manufacturer.
4. See the additional figure in the product data sheet for detail regarding the exposed thermal pad features and dimensions.
5. Falls with JEDEC MO-187 variation AA-T.

FIGURE 1. Case outline - Continued.

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Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I / O	Description
1	OUT	O	Regulator output. A capacitor > 4.7 μ F must be tied from this pin to ground to assure stability.
2	FB	O	This pin the input to the control loop error amplifier. It is used to set the output voltage of the device.
3	NC	---	Not internally connected. This pin must be either be left open or tied to GND.
4	GND	---	Ground.
5	EN	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN_HI}$, the regulator is enabled. If $V_{EN} \leq V_{EN_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
6	NC	---	Not internally connected. This pin must be either be left open or tied to GND.
7	NC	---	Not internally connected. This pin must be either be left open or tied to GND.
8	IN	I	Input supply.
Thermal pad	---	---	Solder to printed circuit board (PCB) to enhanced thermal performance. Note that the thermal pad is internally connected to ground. Although it can be left floating, it is highly recommended to connect the thermal pad to the ground plane.

FIGURE 2. Terminal connections.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/15603-01XE	01295	ZFY4	TPS7A4001MDGNREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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