REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add lead finish E devices. Under Table I, Continuous current per channel Sx, D, or Dx sections for both devices, delete LFCS package limits. Under paragraph 6.3, add Mode of transportation and quantity column. - ro	18-03-06	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	A	A	A	A	A																
PAGE	18	19	20	21	22																

REV STATUS OF PAGES																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17			

PMIC N/A

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Original date of drawing
YY-MM-DD

15-01-20

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

TITLE

MICROCIRCUIT, LINEAR, HIGH VOLTAGE, LATCH-UP PROOF, 4-/8 CHANNEL MULTIPLEXERS, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**
A	**16236**

DWG NO.
V62/15601

REV A

PAGE 1 **OF** 22

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AMSC N/A

5962-V043-18

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high voltage, latch-up proof, 4-/8- channel multiplexers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/15601	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG5208-EP	High voltage, latch-up proof, 4-/8 channel multiplexers
02	ADG5209-EP	High voltage, latch-up proof, 4-/8 channel multiplexers

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153-AB	Thin Shrink Small Outline Package (TSSOP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to V_{SS}	48 V
V_{DD} to GND	-0.3 V to +48 V
V_{SS} to GND	+0.3 V to -48 V
Analog inputs	V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first 2/
Digital inputs	V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first 2/
Peak current, Sx, D, or Dx pins:	
Device type 01	126 mA (pulsed at 1 ms, 10% duty cycle maximum)
Device type 02	92 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous current, Sx, D, or Dx pins	Data + 15% 3/
Temperature range operating	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Junction temperature	150°C
Thermal impedance, θ_{JA}:	
Case X	112.6°C/W
Reflow soldering peak temperature, Pb-Free	260(+0/-5) °C
Electrostatic discharge (ESD): Human body model (HBM):	
I/O Port to supplies	8 kV
I/O port to I/O port	2 kV
All other pins	8 kV

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at https://www.jedec.org).

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Over voltages at the Ax, EN, Sx, D, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
3/ See table I in Continuous current, Sx or D section.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 On leakage. The On leakage shall be as shown in figure 6.

3.5.7 Off leakage. The Off leakage shall be as shown in figure 7.

3.5.8 On resistance. The On resistance shall be as shown in figure 8.

3.5.9 Channel to channel crosstalk. The channel crosstalk shall be as shown in figure 9.

3.5.10 Off isolation. The Off isolation shall be as shown in figure 10.

3.5.11 Bandwidth. The bandwidth shall be as shown in figure 11.

3.5.12 Address to output. The address to output shall be as shown in figure 12.

3.5.13 Break before make time delay, t_D. The Break before make time delay, t_D shall be as shown in figure 13.

3.5.14 Enable delay, t_{ON}(EN), t_{OFF}(EN). The enable delay, t_{ON}(EN), t_{OFF}(EN) shall be as shown in figure 14.

3.5.15 Charge injection. The charge injection shall be as shown in figure 15.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions **±15 V Dual Supply** 2/	25°C			-40°C to +85°C			-55°C to +125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog switch												
Analog Signal Range									V_{DD}		V_{SS}	V
On Resistance	R_{ON}	V_S = ±10 V, I_S = −1 mA; see Figure 8		160								Ω
		V_{DD} = +13.5 V, V_{SS} = −13.5 V			200			250			280	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_S = ±10 V, I_S = −1 mA		3.5								Ω
					8			9			10	Ω
On-Resistance Flatness	$R_{FLAT (ON)}$	V_S = ±10 V, I_S = −1 mA		40								Ω
					50			65			70	Ω
Leakage currents (V_{DD} = +16.5 V, V_{SS} = −16.5 V)												
Source Off Leakage	I_S (Off)	V_S = ±10 V, V_D = ∓10 V; see Figure 7		±0.005								nA
					±0.1			±0.2			±0.4	
Drain Off Leakage	I_D (Off)	V_S = ±10 V, V_D = ∓10 V; see Figure 7		±0.005								
					±0.1			±0.4			±1.4	
Channel On Leakage	I_D (On), I_S (On)	V_S = V_D = ±10 V; see Figure 6		±0.01								
					±0.2			±0.5			±1.4	
Digital inputs												
Input High Voltage	V_{INH}								2.0			V
Input Low Voltage,	V_{INL}										0.8	
	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}		0.002								µA
Input Current											±0.1	
Digital Input Capacitance	C_{IN}			3								pF
Dynamic characteristics 3/												
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF		150								ns
		V_S = 10 V; see Figure 12			180			210			245	
t_{ON} (EN)		R_L = 300 Ω, C_L = 35 pF		125								
		V_S = 10 V; see Figure 14			150			185			215	
t_{OFF} (EN)		R_L = 300 Ω, C_L = 35 pF		160								
		V_S = 10 V; see Figure 14			185			210			230	
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF		55								
		V_{S1} = V_{S2} = 10 V; see Figure 13							20			
Charge Injection	Q_{INJ}	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 15		0.2								pC

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **±15 V Dual Supply** 4/	25°C			-40°C to +85°C			-55°C to +125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Dynamic characteristics - Continued 3/												
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 10		-86								dB
Channel-to-Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz , see Figure 9		-80								dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF; see Figure 11										MHz
Device type 01				110								
Device type 02				240								
Insertion Loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz see Figure 11		-6.4								dB
CS (Off)		V_S = 0 V, f = 1 MHz		2.9								pF
C_D (Off)												
Device type 01		V_S = 0 V, f = 1 MHz		34								
Device type 02		V_S = 0 V, f = 1 MHz		17								
C_D (On), C_S (On)												
Device type 01		V_S = 0 V, f = 1 MHz		37								
Device type 02		V_S = 0 V, f = 1 MHz		21								
Power requirements (V_{DD} = +16.5 V, V_{SS} = −16.5 V)												
I_{DD}		Digital inputs = 0 V or V_{DD}		45								µA
					55						80	
I_{SS}		Digital inputs = 0 V or V_{DD}		0.001								
											1	
V_{DD}/V_{SS}		GND = 0 V							±9		±22	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **±20 V Dual Supply** 4/	25°C			-40°C to +85°C			-55°C to +125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog switch												
Analog Signal Range									V_{DD}		V_{SS}	V
On Resistance	R_{ON}	V_S = ±15 V, I_S = −1 mA; see Figure 8		140								Ω
		V_{DD} = +18 V, V_{SS} = −18 V			160			200			230	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_S = ±15 V, I_S = −1 mA		3.5								Ω
					8			9			10	Ω
On-Resistance Flatness	$R_{FLAT (ON)}$	V_S = ±15 V, I_S = −1 mA		34								Ω
					45			55			60	Ω
Leakage currents (V_{DD} = +22 V, V_{SS} = −22 V)												
Source Off Leakage	I_S (Off)	V_S = ±15 V, V_D = ∓15 V; see Figure 7		±0.005								nA
					±0.1			±0.2			±0.4	
Drain Off Leakage	I_D (Off)	V_S = ±15 V, V_D = ∓15 V; see Figure 7		±0.005								
					±0.1			±0.4			±1.4	
Channel On Leakage	I_D (On), I_S (On)	V_S = V_D = ±15 V; see Figure 6		±0.01								
					±0.2			±0.5			±1.4	
Digital inputs												
Input High Voltage	V_{INH}								2.0			V
Input Low Voltage,	V_{INL}										0.8	
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}		0.002								µA
											±0.1	
Digital Input Capacitance	C_{IN}			3								pF
Dynamic characteristics 3/												
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF		140								ns
		V_S = 10 V; see Figure 12			170			195			220	
t_{ON} (EN)		R_L = 300 Ω, C_L = 35 pF		120								
		V_S = 10 V; see Figure 14			140			170			195	
t_{OFF} (EN)		R_L = 300 Ω, C_L = 35 pF		160								
		V_S = 10 V; see Figure 14			185			205			220	
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF		45								
		V_{S1} = V_{S2} = 10 V; see Figure 13							20			
Charge Injection	Q_{INJ}	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 15		0.4								pC

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **±20 V Dual Supply** 4/	25°C			-40°C to +85°C			-55°C to +125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Dynamic characteristics - Continued 3/												
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 10		-86								dB
Channel-to-Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz , see Figure 9		-80								dB
−3 dB Bandwidth Device type 01 Device type 02		R_L = 50 Ω, C_L = 5 pF; see Figure 11		 121 225								MHz
Insertion Loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz see Figure 11		-5.6								dB
CS (Off)		V_S = 0 V, f = 1 MHz		2.8								pF
C_D (Off) Device type 01 Device type 02		 V_S = 0 V, f = 1 MHz V_S = 0 V, f = 1 MHz		 33 17								
C_D (On), C_S (On) Device type 01 Device type 02		 V_S = 0 V, f = 1 MHz V_S = 0 V, f = 1 MHz		 36 21								
Power requirements (V_{DD} = +22 V, V_{SS} = −22 V)												
I_{DD}		Digital inputs = 0 V or V_{DD}		50								µA
					70						120	
I_{SS}		Digital inputs = 0 V or V_{DD}		0.001								
											1	
V_{DD}/V_{SS}		GND = 0 V							±9		±22	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **12 V Single Supply** 5/	25°C			-40°C to +85°C			-55°C to +125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog switch												
Analog Signal Range									0		V_{DD}	V
On Resistance	R_{ON}	V_S = 0 to 10 V, I_S = −1 mA; see Figure 8		350								Ω
		V_{DD} = 10.8 V, V_{SS} = 0 V			500			610			700	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_S = 0 to 10 V, I_S = −1 mA		5								Ω
					20			22			24	Ω
On-Resistance Flatness	$R_{FLAT (ON)}$	V_S = 0 to 10 V, I_S = −1 mA		160								Ω
					280			335			370	Ω
Leakage currents (V_{DD} = 13.2 V, V_{SS} = 0 V)												
Source Off Leakage	I_S (Off)	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 7		±0.005								nA
					±0.1			±0.2			±0.4	
Drain Off Leakage	I_D (Off)	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 7		±0.005								
					±0.1			±0.4			±1.4	
Channel On Leakage	I_D (On), I_S (On)	V_S = V_D = 1 V/10 V; see Figure 6		±0.01								
					±0.2			±0.5			±1.4	
Digital inputs												
Input High Voltage	V_{INH}								2.0			V
Input Low Voltage,	V_{INL}										0.8	
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}		0.002								µA
											±0.1	
Digital Input Capacitance	C_{IN}			3								pF
Dynamic characteristics 3/												
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF		200								ns
		V_S = 8 V; see Figure 12			250			295			335	
t_{ON} (EN)		R_L = 300 Ω, C_L = 35 pF		180								
		V_S = 8 V; see Figure 14			225			280			320	
t_{OFF} (EN)		R_L = 300 Ω, C_L = 35 pF		165								
		V_S = 8 V; see Figure 14			200			225			245	
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF		95								
		V_{S1} = V_{S2} = 8 V; see Figure 13							45			

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **12 V Single Supply** 5/	25°C			-40°C to +85°C			-55°C to +125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Dynamic characteristics - Continued 3/												
Charge Injection	Q_{INJ}	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 15		0.2								pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 10		-86								dB
Channel-to-Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz , see Figure 9		-80								dB
−3 dB Bandwidth Device type 01 Device type 02		R_L = 50 Ω, C_L = 5 pF; see Figure 11		 95 180								MHz
Insertion Loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz see Figure 11		-8.9								dB
CS (Off)		V_S = 6 V, f = 1 MHz		3.3								pF
C_D (Off) Device type 01 Device type 02		 V_S = 6 V, f = 1 MHz V_S = 6 V, f = 1 MHz		 38 19								
C_D (On), C_S (On) Device type 01 Device type 02		 V_S = 6 V, f = 1 MHz V_S = 6 V, f = 1 MHz		 41 24								
Power requirements (V_{DD} = 13.2 V)												
I_{DD}		Digital inputs = 0 V or V_{DD}		40								µA
					50						75	
V_{DD}		GND = 0 V, V_{SS} = 0 V							9		40	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **36 V Single Supply** 6/	25°C			-40°C to +85°C			-55°C to +125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog switch												
Analog Signal Range									0		V_{DD}	V
On Resistance	R_{ON}	V_S = 0 to 30 V, I_S = −1 mA; see Figure 8		150								Ω
		V_{DD} = 32.4 V, V_{SS} = 0 V			170			215			245	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_S = 0 to 30 V, I_S = −1 mA		3.5								Ω
					8			9			10	Ω
On-Resistance Flatness	$R_{FLAT (ON)}$	V_S = 0 to 30 V, I_S = −1 mA		35								Ω
					55			65			70	Ω
Leakage currents (V_{DD} = 39.6 V, V_{SS} = 0 V)												
Source Off Leakage	I_S (Off)	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 7		±0.005								nA
					±0.1			±0.2			±0.4	
Drain Off Leakage	I_D (Off)	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 7		±0.005								
					±0.1			±0.4			±1.4	
Channel On Leakage	I_D (On), I_S (On)	V_S = V_D = 1 V/30 V; see Figure 6		±0.01								
					±0.2			±0.5			±1.4	
Digital inputs												
Input High Voltage	V_{INH}								2.0			V
Input Low Voltage,	V_{INL}										0.8	
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}		0.002								µA
											±0.1	
Digital Input Capacitance	C_{IN}			3								pF
Dynamic characteristics 3/												
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF		170								ns
		V_S = 18 V; see Figure 12			205			225			235	
t_{ON} (EN)		R_L = 300 Ω, C_L = 35 pF		150								
		V_S = 18 V; see Figure 14			180			195			215	
t_{OFF} (EN)		R_L = 300 Ω, C_L = 35 pF		180								
		V_S = 18 V; see Figure 14			225			225			230	
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF		55								
		V_{S1} = V_{S2} = 18 V; see Figure 13							20			

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **36 V Single Supply** 6/	25°C			-40°C to +85°C			-55°C to +125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Dynamic characteristics - Continued 3/												
Charge Injection	Q_{INJ}	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF, see Figure 15		0.3								pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 10		-86								dB
Channel-to-Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz , see Figure 9		-80								dB
−3 dB Bandwidth Device type 01 Device type 02		R_L = 50 Ω, C_L = 5 pF; see Figure 11		 105 195								MHz
Insertion Loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz see Figure 11		-6.2								dB
CS (Off)		V_S = 18 V, f = 1 MHz		2.7								pF
C_D (Off) Device type 01 Device type 02		 V_S = 18 V, f = 1 MHz V_S = 18 V, f = 1 MHz		 32 16								
C_D (On), C_S (On) Device type 01 Device type 02		 V_S = 18 V, f = 1 MHz V_S = 18 V, f = 1 MHz		 35 20								
Power requirements (V_{DD} = 39.6 V)												
I_{DD}		Digital inputs = 0 V or V_{DD}		80								µA
					100						155	
V_{DD}		GND = 0 V, V_{SS} = 0 V							9		40	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	25°C		85°C		125°C		Unit
			Min	Max	Min	Max	Min	Max	
CONTINUOUS CURRENT PER CHANNEL Sx, D, or Dx (for device type 01)									
Continuous current, Sx or D									
V_{DD} = +15 V, V_{SS} = -15 V TSSOP (θ_{JA} = 112.6 °C/W)				40		24		14.5	mA
V_{DD} = +20 V, V_{SS} = -20 V TSSOP (θ_{JA} = 112.6 °C/W)				42		26.5		14.5	
V_{DD} = 12 V, V_{SS} = 0 V TSSOP (θ_{JA} = 112.6 °C/W)				28		19		12	
V_{DD} = 36 V, V_{SS} = 0 V TSSOP (θ_{JA} = 112.6 °C/W)				40		26		14.5	
CONTINUOUS CURRENT PER CHANNEL Sx, D, or Dx (for device type 02)									
Continuous current, Sx or D									
V_{DD} = +15 V, V_{SS} = -15 V TSSOP (θ_{JA} = 112.6 °C/W)				29		19		12	mA
V_{DD} = +20 V, V_{SS} = -20 V TSSOP (θ_{JA} = 112.6 °C/W)				30		20		12.5	
V_{DD} = 12 V, V_{SS} = 0 V TSSOP (θ_{JA} = 112.6 °C/W)				20		14		10	
V_{DD} = 36 V, V_{SS} = 0 V TSSOP (θ_{JA} = 112.6 °C/W)				30		20		12.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = +15 V ±10%, V_{SS} = -15 V ±10%, GND = 0 V, unless otherwise noted.

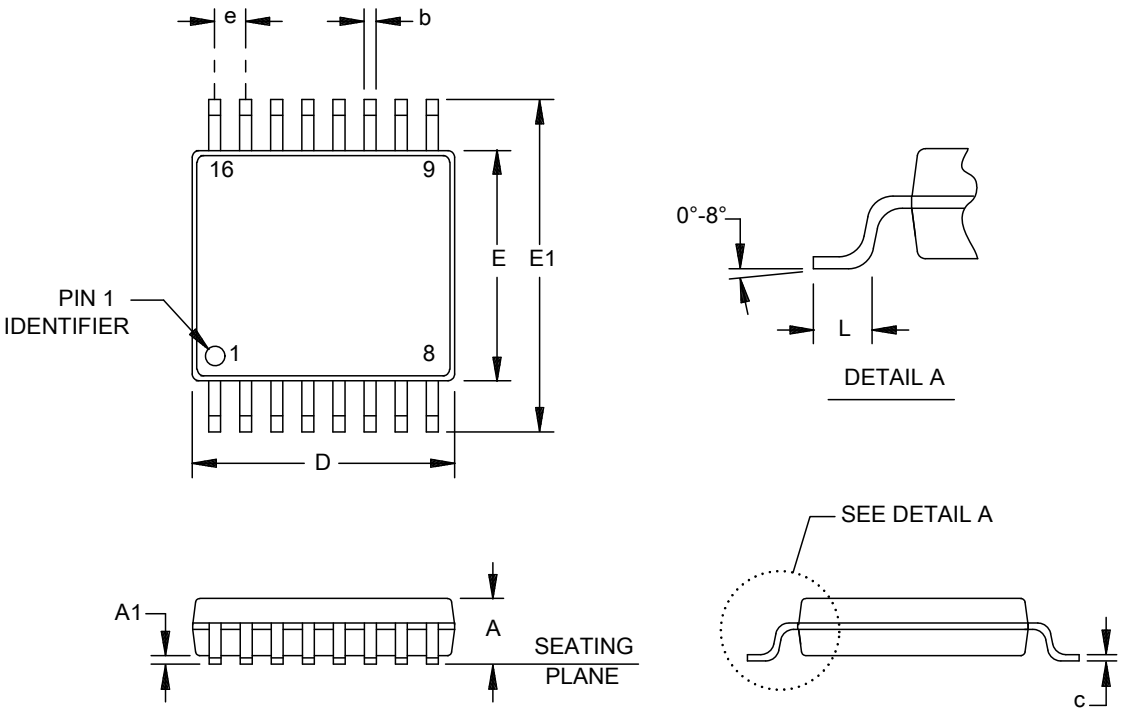
3/ Guaranteed by design; not subject to production test.

4/ V_{DD} = +20 V ±10%, V_{SS} = -20 V ±10%, GND = 0 V, unless otherwise noted.

5/ V_{DD} = 12 V ±10%, V_{SS} = 0 V. GND = 0 V, unless otherwise noted.

6/ V_{DD} = 36 V ±10%, V_{SS} = 0 V. GND = 0 V, unless otherwise noted.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 BSC	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-153-AB.

FIGURE 1. Case outline.

Case outline X								
Device type 01					Device type 02			
Terminal number	Terminal symbol	Terminal number	Terminal symbol		Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	16	A1		1	A0	16	A1
2	EN	15	A2		2	EN	15	GND
3	V_{SS}	14	GND		3	V_{SS}	14	V_{DD}
4	S1	13	V_{DD}		4	S1A	13	S1B
5	S2	12	S5		5	S2A	12	S2B
6	S3	11	S6		6	S3A	11	S3B
7	S4	10	S7		7	S4A	10	S4B
8	D	9	S8		8	DA	9	DB

FIGURE 2. Terminal connections.

Device Type 01		
Terminal number	Terminal symbol	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, the Ax logic inputs determine the on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1	Source Terminal 1. This pin can be an input or an output.
5	S2	Source Terminal 2. This pin can be an input or an output.
6	S3	Source Terminal 3. This pin can be an input or an output.
7	S4	Source Terminal 4. This pin can be an input or an output.
8	D	Drain Terminal. This pin can be an input or an output.
9	S8	Source Terminal 8. This pin can be an input or an output.
10	S7	Source Terminal 7. This pin can be an input or an output.
11	S6	Source Terminal 6. This pin can be an input or an output.
12	S5	Source Terminal 5. This pin can be an input or an output.
13	V_{DD}	Most Positive Power Supply Potential.
14	GND	Ground (0 V) Reference.
15	A2	Logic Control Input.
16	A1	Logic Control Input.

FIGURE 3. Terminal function.

Device Type 02		
Terminal number	Terminal symbol	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine the on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1A	Source Terminal 1A. This pin can be an input or an output.
5	S2A	Source Terminal 2A. This pin can be an input or an output.
6	S3A	Source Terminal 3A. This pin can be an input or an output.
7	S4A	Source Terminal 4A. This pin can be an input or an output.
8	DA	Drain Terminal A. This pin can be an input or an output.
9	DB	Drain Terminal B. This pin can be an input or an output.
10	S4B	Source Terminal 4B. This pin can be an input or an output.
11	S3B	Source Terminal 3B. This pin can be an input or an output.
12	S2B	Source Terminal 2B. This pin can be an input or an output.
13	S1B	Source Terminal 1B. This pin can be an input or an output.
14	V_{DD}	Most Positive Power Supply Potential.
15	GND	Ground (0 V) Reference.
16	A1	Logic Control Input.

FIGURE 3. Terminal function - Continued.

Device Type 01				
A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't care

Device Type 02			
A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't care

FIGURE 4. Truth table.

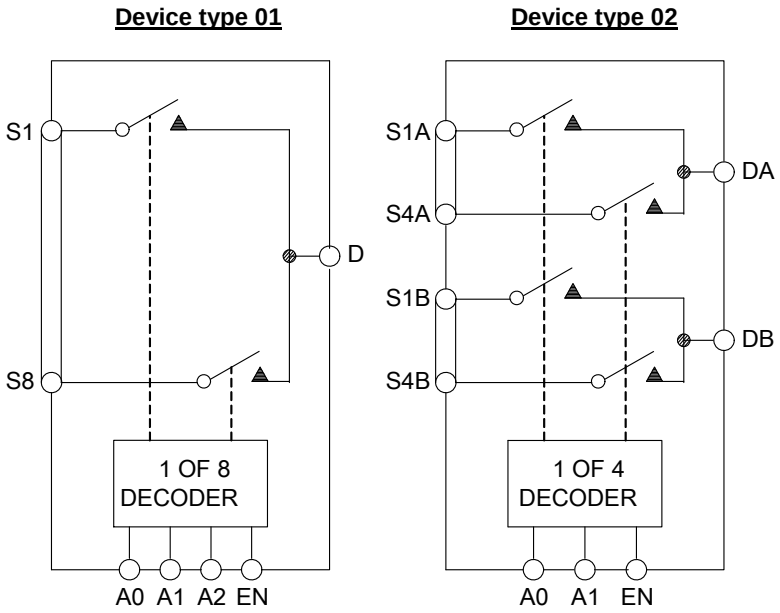


FIGURE 5. Functional block diagram.

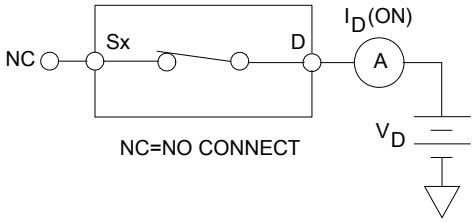


FIGURE 6. On leakage.

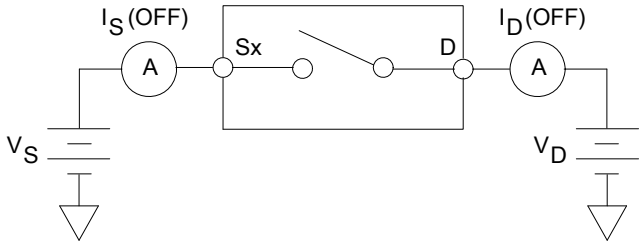


FIGURE 7. Off leakage.

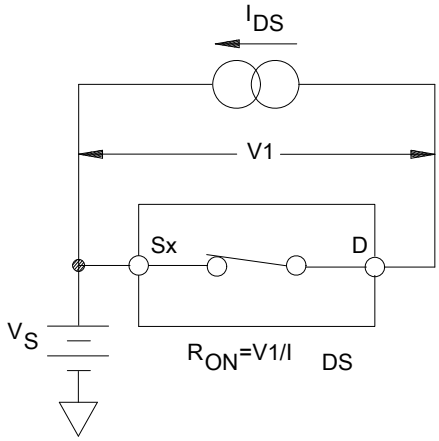
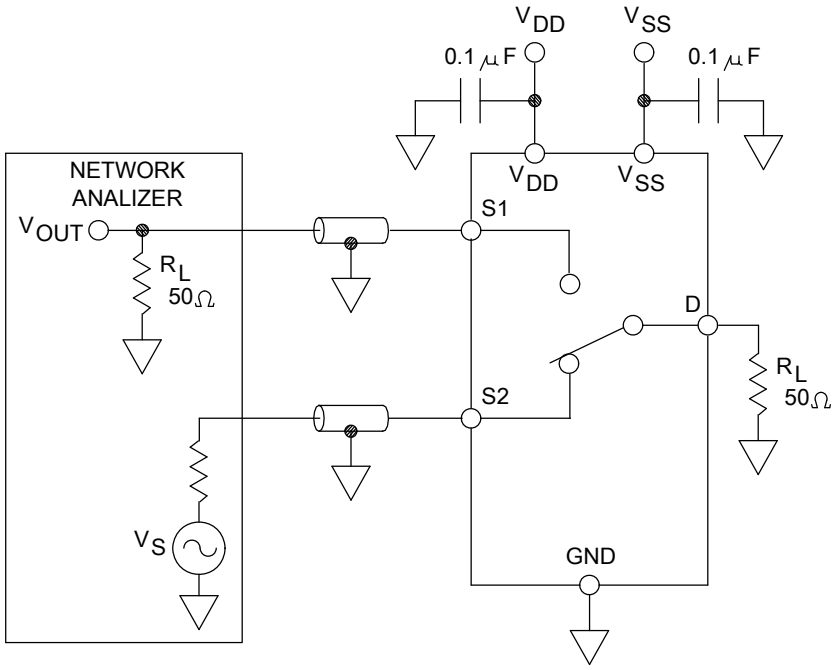


FIGURE 8. On resistance.



CHANNEL-TO-CHANNEL CROSSTALK = 20 log $\frac{V_{OUT}}{V_S}$

FIGURE 9. Channel to channel crosstalk.

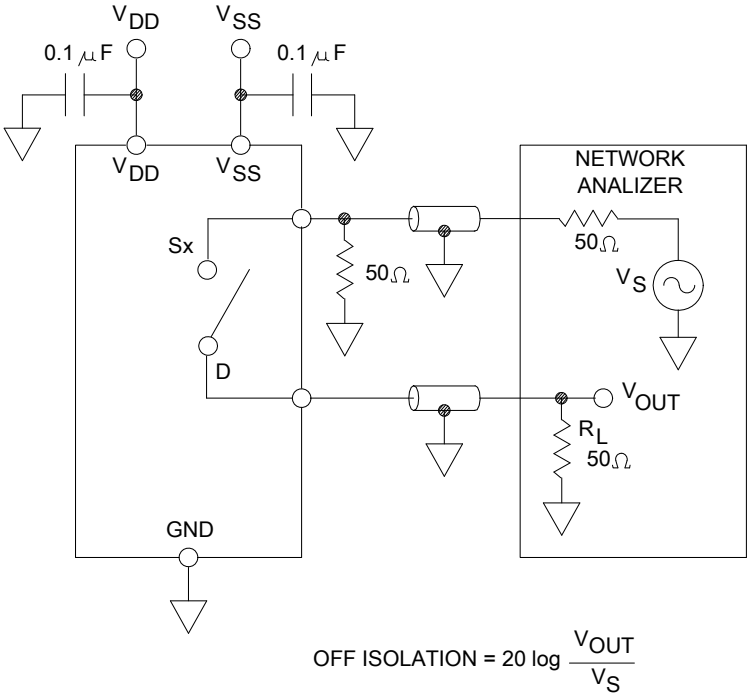


FIGURE 10. Off isolation.

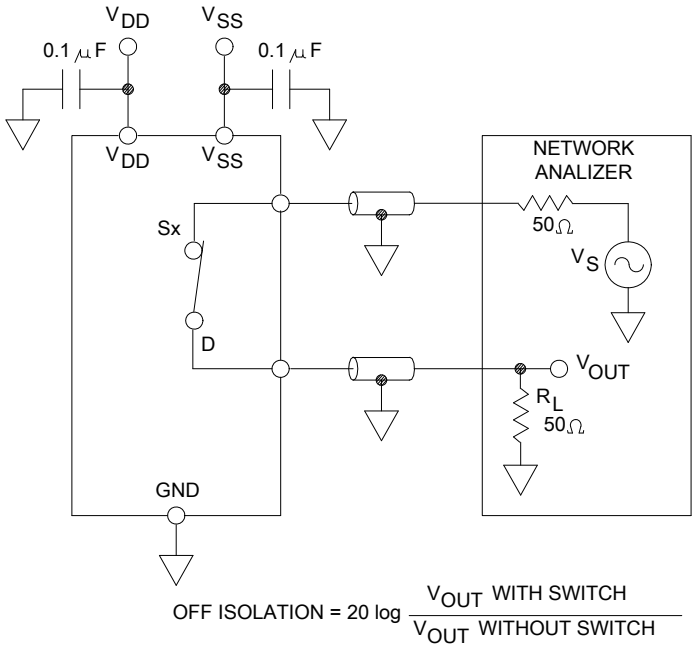


FIGURE 11. Bandwidth.

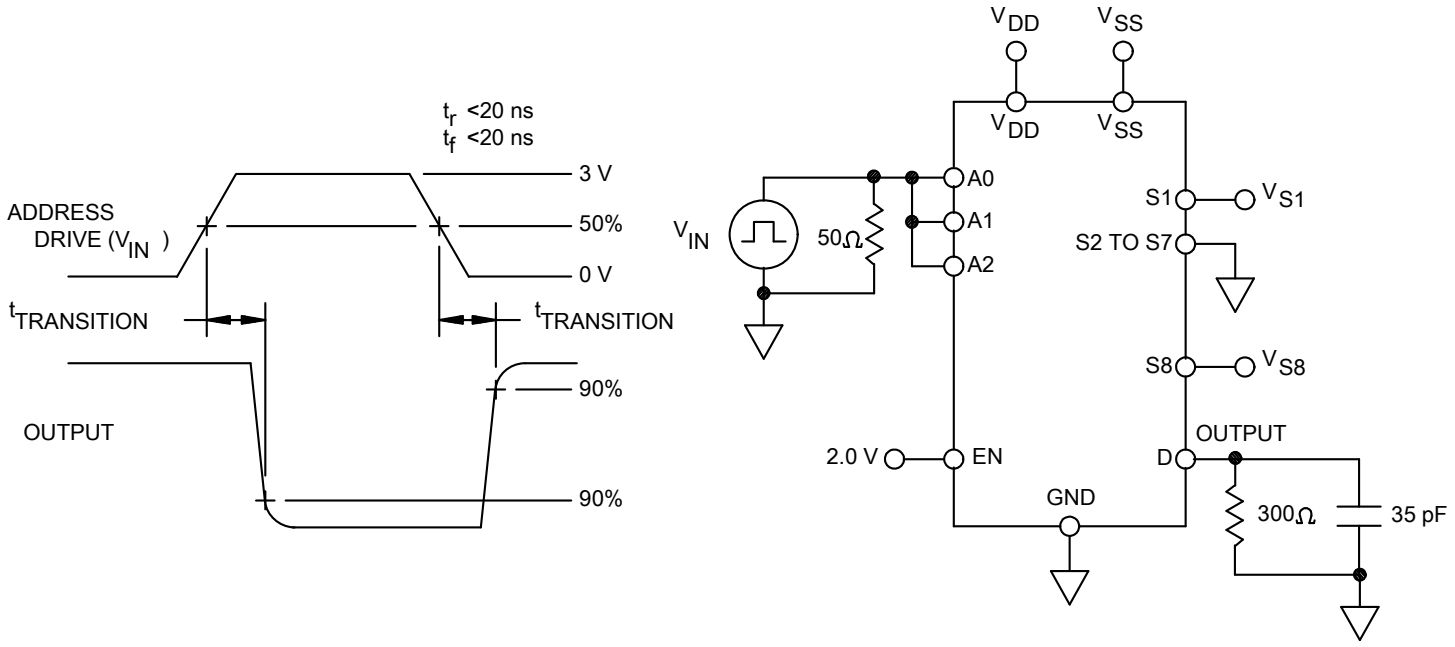


FIGURE 12. Address to output switching times, $t_{TRANSACTION}$.

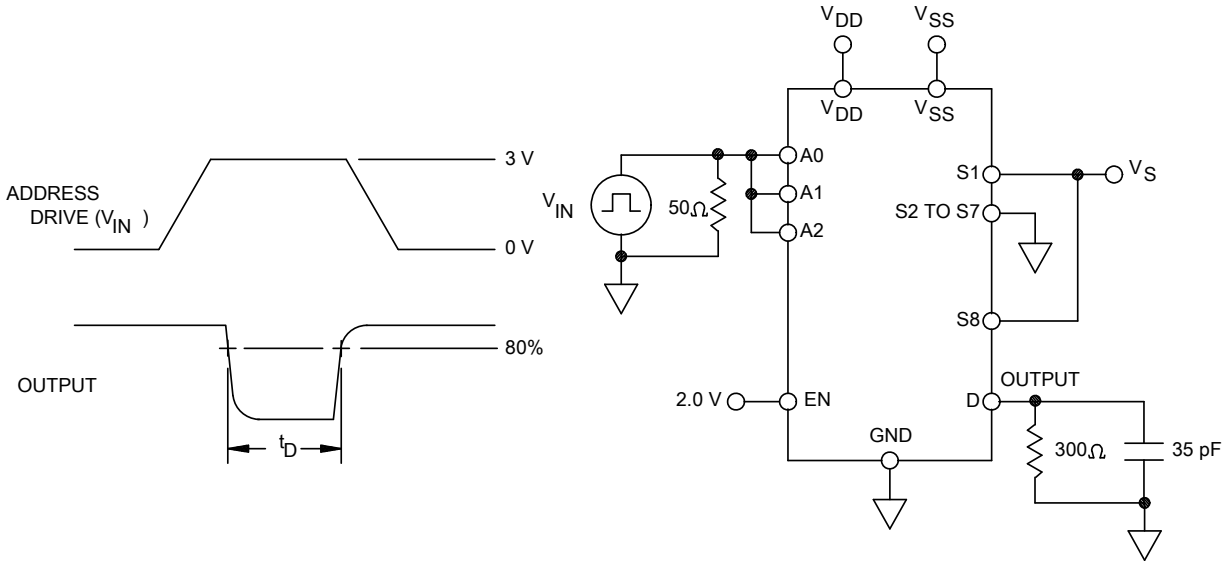


FIGURE 13. Break before make time delay, t_D.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/15601
		REV A	PAGE 20

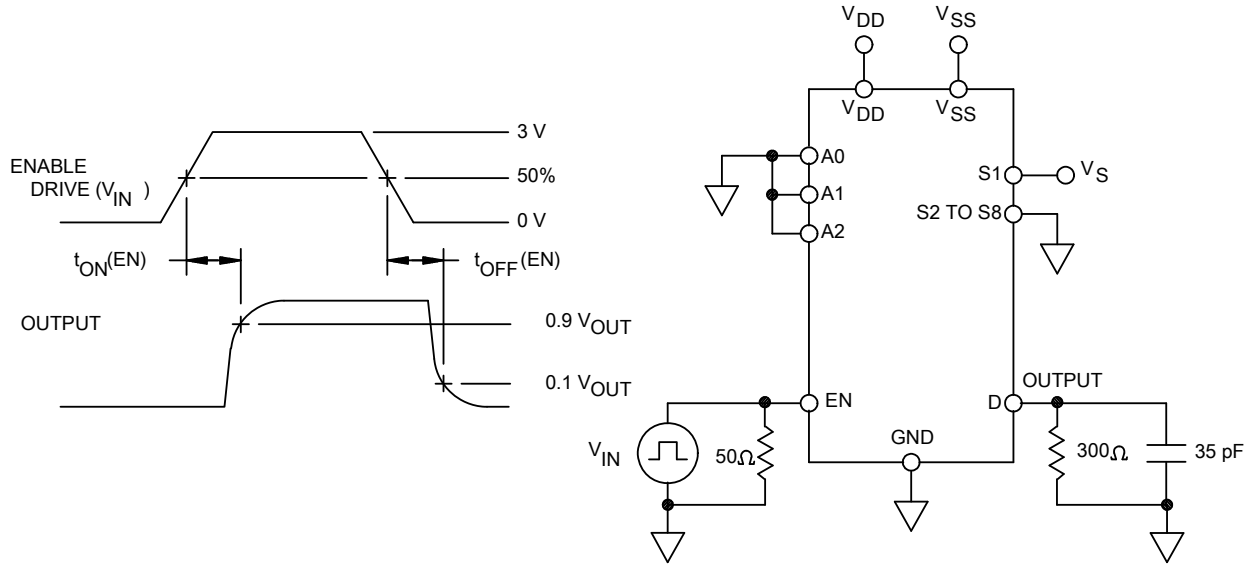


FIGURE 14. Enable delay, t_{ON}(EN), t_{OFF}(EN)

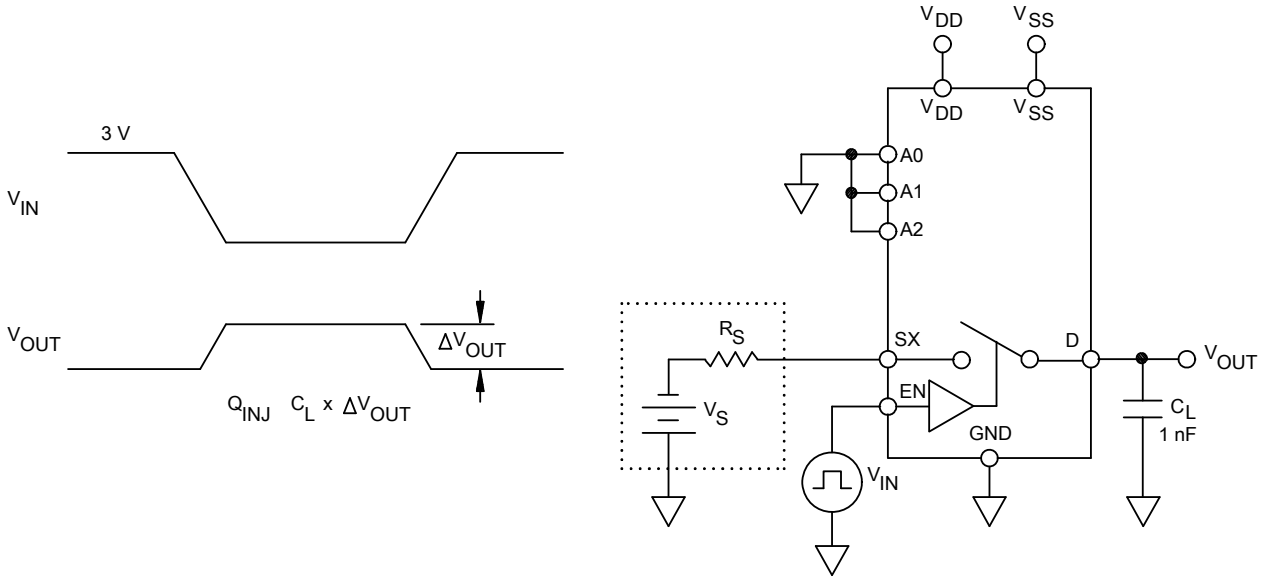


FIGURE 15. Charge injection.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/15601-01XB	24355	Reel, 1000 units	ADG5208SRU-EP-RL7
V62/15601-01XE	24355	Reel, 1000 units	ADG5208SRUZ-EP-RL7
V62/15601-02XB	24355	Reel, 1000 units	ADG5209SRU-EP-RL7
V62/15601-02XE	24355	Reel, 1000 units	ADG5209SRUZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland