REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct $I_{AM,100\%}$ and $I_{AM,RAM}$ values in Table I. - PHN	15-01-26	Thomas M. Hess
B	Correct Vendor part number in section 6.3. phn	15-08-25	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - PHN	22-03-28	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV	C	C	C	C	C	C	C	C														
SHEET	23	24	25	26	27	28	29	30														
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

Original date of drawing

YY MM DD

14-12-22

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TITLE
MICROCIRCUIT, DIGITAL, MIXED SIGNAL MICROCONTROLLERS, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/14644
REV C		PAGE 1 OF 30

AMSC N/A

5962-V028-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance mixed signal microcontrollers microcircuit, with an operating temperature range of -55ºC to +85ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14644	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	MSP430FR5739-EP	Mixed signal microcontrollers

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	40	JEDEC MO-220	Plastic quad Flatpack no-lead

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage applied at V_{CC} to V_{SS}	-0.3 V to 4.1 V
Voltage applied to any pin (excluding VCORE)	-0.3 V to V_{CC} + 0.3 V 2/
Maximum diode current at any device pin	±2 mA
Maximum junction temperature, T_J	95°C
Storage temperature range, T_{stg}	-55°C to 125°C 3/ 4/ 5/

1.4 Recommended operating conditions. 6/

Supply voltage during program execution and FRAM programming (AVCC = DVCC)	2.0 V to 3.6 V 7/
Supply voltage (AVSS = DVSS), V_{SS}	0 V TYP
Operating free air temperature, T_J	-55°C to 85°C
Typical required capacitor at VCORE, C_{VCORE}	470 nF 8/
Minimum capacitor ratio of VCC to VCORE , C_{VCC}/C_{VCORE}	10 pF
Processor frequency (maximum MCLK frequency), f_{SYSTEM} 9/:	
No FRAME wait states, 10/ $2V \le V_{CC} \le 3.6$ V	0 MHz to 8.0 MHz
With FRAME wait state, 10/:	
NACCESS = {2}, NPERCHING = {1}, $2V \le V_{CC} \le 3.6$ V	0 MHz to 24.0 MHz

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices.
JESD J-STD020	–	Standard for moisture/reflow sensitivity classification for nonhermetric solid state surface mount devices.

(Copies of these documents are available online at https://www.jedec.org).

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltages referenced to VSS. VCORE is for internal device use only. No external DC loading or voltage should be applied.
3/ Data retention on FRAM memory cannot be ensured when exceeding the specified maximum storage temperature, Tstg.
4/ For soldering during board manufacturing, it is required to follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
5/ Programming of devices with user application code should only be performed after reflow or hand soldering. Factory programmed information, such as calibration values, are designed to withstand the temperatures reached in the current JEDEC J-STD-020 specification.
6/ Typical values are specified at VCC = 3.3 V and TA = 25°C (unless otherwise noted).
7/ It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
8/ A capacitor tolerance of ±20% or better is required.
9/ Modules may have a different maximum input clock specification. See the specification of the respective module in the manufacturer data sheet.
10/ When using manual wait state control, see the *MSP430FR57xx Family User's Guide* (SLAU272) from manufacturer data sheet for recommended settings for common system frequencies.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Typical Active mode supply currents, No Wait states. The typical Active mode supply currents, No Wait states shall be as shown in figure 4.

3.5.5 Typical Low-Level Output Current vs Low-Level Output Voltage, V_{CC} = 2.0 V. The typical Low-Level Output Current vs Low-Level Output Voltage, V_{CC} = 2.0 V shall be as shown in figure 5.

3.5.6 Typical Low-Level Output Current vs Low-Level Output Voltage, V_{CC} = 3.0 V. The typical Low-Level Output Current vs Low-Level Output Voltage, V_{CC} = 3.0 V shall be as shown in figure 6.

3.5.7 Typical High-Level Output Current vs High-Level Output Voltage, V_{CC} = 2.0 V. The Typical High-Level Output Current vs High-Level Output Voltage, V_{CC} = 2.0 V shall be as shown in figure 7.

3.5.8 Typical High-Level Output Current vs High-Level Output Voltage, V_{CC} = 3.0 V. The Typical High-Level Output Current vs High-Level Output Voltage, V_{CC} = 3.0 V shall be as shown in figure 8.

3.5.9 SPI Master mode, CKPH = 0. The SPI Master mode, CKPH = 0 shall be as shown in figure 9.

3.5.10 SPI Master mode, CKPH = 1. The SPI Master mode, CKPH = 0 shall be as shown in figure 10.

3.5.11 SPI Slave mode, CKPH = 0. The SPI Slave mode, CKPH = 0 shall be as shown in figure 11.

3.5.12 SPI Slave mode, CKPH = 1. The SPI Slave mode, CKPH = 0 shall be as shown in figure 12.

3.5.13 I2C Mode timing. The I2C mode timing shall be as shown in figure 13.

3.5.14 Typical temperature sensor voltage. The typical temperature sensor voltage shall be as shown in figure 14.

TABLE I. Electrical performance characteristics. 1/

Test	Execution Memory	V_{CC}	Frequency ($f_{MCLK} = f_{SMCLK}$) 5/												Unit
			1 MHz		4 MHz		8 MHz		16 MHz		20 MHz		24 MHz		
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Active Mode Supply Current Into VCC Excluding External Current 2/ 3/ 4/ 5/															
$I_{AM, FRAM\_UNI}$ 7/	FRAM	3 V	0.27		0.58		1.0		1.53		1.9		2.2		mA
$I_{AM,0\%}$ 8/	FRAM 0% cache hit ratio	3 V	0.42	0.75	1.2	1.7	2.2	2.9	2.3	3.0	2.8	3.7	3.45	4.3	
$I_{AM,50\%}$ 8/ 9/	FRAM 50% cache hit ratio	3 V	0.31		0.73		1.3		1.75		2.1		2.5		
$I_{AM,66\%}$ 8/ 9/	FRAM 66% cache hit ratio	3 V	0.27		0.58		1.0		1.55		1.9		2.2		
$I_{AM,75\%}$ 8/ 9/	FRAM 75% cache hit ratio	3 V	0.25		0.5		0.82		1.3		1.6		1.8		
$I_{AM,100\%}$ 8/ 9/	FRAM 100% cache hit ratio	3 V	0.2	0.44	0.3	0.56	0.42	0.81	0.73	1.17	0.88	1.32	1.0	1.53	
$I_{AM, RAM}$ 9/ 10/	RAM	3 V	0.2	0.41	0.35	0.56	0.55	0.77	1.0	1.27	1.20	1.47	1.45	1.8	

Test	Symbol	V_{CC}	-55 °C		25 °C		85 °C		Unit
			Typ	Max	Typ	Max	Typ	Max	
Low-Power Mode Supply Currents (Into VCC) Excluding External Current 11/ 3/ 4/									
Low power mode 0 12/ 13/	$I_{LPM0, 1MHz}$	2 V, 3 V	166		175		225		µA
Low power mode 0 13/ 14/	$I_{LPM0, 8MHz}$	2 V, 3 V	170		177	244	225	360	
Low power mode 0 13/ 15/	$I_{LPM0, 24MHz}$	2 V, 3 V	274		285	340	340	455	
Low power mode 2 16/ 17/	I_{LMP2}	2 V, 3 V	56		61	80	110	210	
Low power mode 3, crystal mode 17/ 18/	$I_{LMP3, XT1LF}$	2 V, 3 V	3.4		6.4	15	48	150	
Low power mode 3, VLO mode 17/ 19/	$I_{LPM3,VLO}$	2 V, 3 V	3.3		6.3	15	48	150	
Low power mode 4 17/ 20/	I_{LPM4}	2 V, 3 V	2.9		5.9	15	48	150	
Low power mode 3.5 21/	$I_{LPM3.5}$	2 V, 3 V	1.3		1.5	2.2	2.8	5.0	
Low power mode 4.5 22/	$I_{LPM4.5}$	2 V, 3 V	0.3		0.32	0.66	0.57	2.55	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Schmitt-Trigger Inputs – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{RST}$/NMI)							
Positive going input threshold voltage	V_{IT+}		2 V	0.7		1.7	V
			3 V	1.45		2.12	
Negative going input threshold voltage	V_{IT-}		2 V	0.41		1.101	
			3 V	0.72		1.68	
Input voltage hysteresis (V_{IT+} - V_{IT-})	V_{hys}		2 V	0.24		0.855	
			3 V	0.27		1.02	
Pull up or pull down resistor	R_{Pull}	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		19	35	51	kΩ
Input capacitance	C_I				5		pF
Inputs – Ports P1 and P2 (P1.0 to P1.7, P2.0 to P2.7) 23/							
External interrupt timing 24/	$t_{(int)}$	External trigger pulse duration to set interrupt flag	2 V, 3V	20			ns
Leakage Current – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{RST}$/NMI)							
High-impedance leakage current		25/ 26/	2 V, 3 V	-65		65	nA
Outputs – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)							
High level output voltage	V_{OH}	$I_{(OHmax)}$ = –1 mA 27/	2 V	V_{CC} – 0.25		V_{CC}	V
		$I_{(OHmax)}$ = –3 mA 28/		V_{CC} – 0.60		V_{CC}	
		$I_{(OHmax)}$ = –2 mA 27/	3 V	V_{CC} – 0.25		V_{CC}	
		$I_{(OHmax)}$ = –6 mA 28/		V_{CC} – 0.60		V_{CC}	
Low level output voltage	V_{OL}	$I_{(OLmax)}$ = 1 mA 27/	2 V	V_{SS}		V_{SS} + 0.25	
		$I_{(OLmax)}$ = 3 mA 28/		V_{SS}		V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA 27/	3 V	V_{SS}		V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA 28/		V_{SS}		V_{SS} + 0.60	
Output Frequency – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)							
Port output frequency (with load)	$f_{Px,y}$	Px.y 29/ 30/	2 V			16	MHz
			3 V			24	
Clock output frequency	f_{Port_CLK}	ACLK, SMCLK, or MCLK at configured output port,	2 V			16	
		C MHz L = 20 pF, no DC loading 30/	3 V			24	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Crystal Oscillator, XT1, Low-Frequency (LF) Mode 31/							
Additional current consumption XT1 LF mode from lowest drive setting	$\Delta I_{VCC.LF}$	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {1}, $C_{L,eff}$ = 9 pF, T_A = 25°C,	3 V		60		nA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {2}, T_A = 25°C, $C_{L,eff}$ = 9 pF	3 V		90		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12 pF	3 V		140		
XT1 oscillator crystal frequency, LF mode	$f_{XT1,LF0}$	XTS = 0, XT1BYPASS = 0			32768		Hz
XT1 oscillator logic-level square-wave input frequency, LF mode	$f_{XT1,LF,SW}$	XTS = 0, XT1BYPASS = 1 32/ 33/		10	32.768	50	kHz
Oscillation allowance for LF crystals 34/	OA_{LF}	XTS = 0, XT1BYPASS = 0, XT1DRIVE = {0}, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
Duty cycle, LF mode		XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30		70	%
Oscillator fault frequency, LF mode 35/	$f_{Fault,LF}$	XTS = 0 36/		10		10000	Hz
Startup time, LF mode 37/	$t_{START,LF}$	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 6 pF	3 V		1000		ms
		fOSC = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12 pF			1000		
Integrated effective load capacitance, LF mode 38/ 39/	$C_{L,eff}$	XTS = 0			1		pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Crystal Oscillator, XT1, Low-Frequency (LF) Mode 31/							
XT1 oscillator crystal current HF mode	IVCC,HF	f_{OSC} = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 16 pF	3 V		175		µA
		f_{OSC} = 8 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {1}, T_A = 25°C, $C_{L,eff}$ = 16 pF			300		
		f_{OSC} = 16 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {2}, T_A = 25°C, $C_{L,eff}$ = 16 pF			350		
		f_{OSC} = 24 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 16 pF			550		
XT1 oscillator crystal frequency, HF mode 0	$f_{XT1,HF0}$	XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0} 33/		4		6	MHz
XT1 oscillator crystal frequency, HF mode 1	$f_{XT1,HF1}$	XTS = 1, XT1BYPASS = 0, XT1DRIVE = {1} 33/		6		10	
XT1 oscillator crystal frequency, HF mode 2	$f_{XT1,HF2}$	XTS = 1, XT1BYPASS = 0, XT1DRIVE = {2} 33/		10		16	
XT1 oscillator crystal frequency, HF mode 3	$f_{XT1,HF3}$	XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3} 33/		16		24	
XT1 oscillator logic-level square-wave input frequency, HF mode	$f_{XT1,HF,SW}$	XTS = 1, XT1BYPASS = 1 32/ 33/		1		24	
Oscillation allowance for HF crystals 40/	OA_{HF}	XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0}, $f_{XT1,HF}$ = 4 MHz, $C_{L,eff}$ = 16 pF			450		Ω
		XTS = 1, XT1BYPASS = 0, XT1DRIVE = {1}, $f_{XT1,HF}$ = 8 MHz, $C_{L,eff}$ = 16 pF			320		
		XTS = 1, XT1BYPASS = 0, XT1DRIVE = {2}, $f_{XT1,HF}$ = 16 MHz, $C_{L,eff}$ = 16 pF			200		
		XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3}, $f_{XT1,HF}$ = 24 MHz, $C_{L,eff}$ = 16 pF			200		
Startup time, HF mode 37/	$t_{START,HF}$	f_{OSC} = 4 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 16 pF	3 V		8		ms
		f_{OSC} = 4 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 16 pF			2		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Crystal Oscillator, XT1, Low-Frequency (LF) Mode - Continued 31/							
Integrated effective load capacitance 41/ 42/	$C_{L,eff}$	XTS = 1			1		pF
Duty cycle, HF mode		XTS = 1, Measured at ACLK, $f_{XT1,HF2}$ = 24 MHz		40	50	60	%
Oscillator fault frequency, HF mode 35/	$f_{Fault,HF}$	XTS = 1 36/		145		900	kHz
Internal Very-Low-Power Low-Frequency Oscillator (VLO)							
VLO frequency	f_{VLO}	Measured at ACLK	2 V to 3.6 V	4.3	8.3	13.3	kHz
VLO frequency temperature drift	df_{VLO}/d_T	Measured at ACLK 43/			0.5		%/°C
VLO frequency supply voltage drift	df_{VLO}/d_{VCC}	Measured at ACLK 44/			4		%/V
Duty cycle	$f_{VLO,DC}$	Measured at ACLK		35	50	65	%
DCO frequencies							
DCO frequency low, trimmed	$f_{DCO,LO}$	Measured at ACLK, DCORSEL = 0	2 V to 3.6 V, -40°C to 85°C		5.37	±5%	MHz
		Measured at ACLK, DCORSEL = 1	2 V to 3.6 V, -40°C to 85°C		16.2	±5%	
DCO frequency mid, trimmed	$f_{DCO,MD}$	Measured at ACLK, DCORSEL = 0	2 V to 3.6 V, -40°C to 85°C		6.67	±5%	
		Measured at ACLK, DCORSEL = 1	2 V to 3.6 V, -40°C to 85°C		20	±5%	
DCO frequency high, trimmed	$f_{DCO,HI}$	Measured at ACLK, DCORSEL = 0	2 V to 3.6 V, -40°C to 85°C		8	±5%	
		Measured at ACLK, DCORSEL = 1	2 V to 3.6 V, -40°C to 85°C		23.8	±5%	
Duty cycle	$f_{DCO,DC}$	Measured at ACLK, divide by 1, No external divide, All DCO setting	2 V to 3.6 V, -40°C to 85°C	35	50	65	%

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
MODOSC							
Current consumption	I_{MODOSC}	Enabled	2 V to 3.6 V		44		µA
MODOSC frequency	f_{MODOSC}		2 V to 3.6 V	4.2	5.0	5.7	MHz
Duty cycle	$f_{MODOSC,DC}$	Measured at ACLK, divide by 1	2 V to 3.6 V	35	50	65	%
PMM, Core Voltage							
Core voltage, active mode	V_{CORE}(AM)	2 V ≤ DV_{CC} ≤ 3.6 V			1.5		V
Core voltage, low-current mode	V_{CORE}(LPM)	2 V ≤ DV_{CC} ≤ 3.6 V			1.5		
PMM, SVS, BOR							
SVS_H current consumption, active mode	$I_{SVSH,AM}$	VCC = 3.6 V			5		µA
SVS_H current consumption, low power modes	$I_{SVSH,LPM}$	VCC = 3.6 V			0.8		
SVS_H on voltage level, falling supply voltage	V_{SVSH-}			1.81	1.88	1.95	V
SVS_H off voltage level, rising supply voltage	V_{SVSH+}			1.85	1.93	2	
SVS_H propagation delay, active mode	$t_{PD,SVSH, AM}$	dVCC/dt = 10 mV/µs			10		µs
SVS_H propagation delay, low power modes	$t_{PD,SVSH, LPM}$	dVCC/dt = 1 mV/µs			30		
SVS_L current consumption	I_{SVSL}				0.3		µA
SVS_L on voltage level	$V_{SVSL–}$				1.42		V
SVS_L off voltage level	V_{SVSL+}				1.47		
Wake-Up from Low Power Modes							
Wake-up time from LPM0 to active mode 45/	$t_{WAKE-UP\ LPM0}$		2 V, 3 V, -40°C to 85°C		0.58	1.1	µs
Wake-up time from LPM1, LPM2 to active mode 45/	$t_{WAKE-UP\ LPM12}$				12	25	
Wake-up time from LPM3 or LPM4 to active mode 45/	$t_{WAKE-UP\ LPM34}$				78	165	
Wake-up time from LPM3.5 or LPM4.5 to	$t_{WAKE-UP}$		2 V, 3 V, 0°C to 85°C		310	575	
active mod	$_{LPMx.5}$		2 V, 3 V, -40°C to 85°C		310	1100	
Wake-up time from $\overline{RST}$ to active mode 46/	$t_{WAKE-UP\ RESET}$	V_{CC} stable	2 V, 3 V, -40°C to 85°C		230		
Wake-up time from BOR or power-up to active mode	$t_{WAKE-UP\ BOR}$	dV_{CC}/dt = 2400 V/s			1.6		ms
Pulse duration required at $\overline{RST}$/NMI terminal to accept a reset event 47/	t_{RESET}			4			ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Timer_A							
Timer_A input clock frequency	f_{TA}	Internal: SMCLK, ACLK, External: TACLK Duty cycle = 50% ± 10%	2 V, 3 V			24	MHz
Timer_A capture timing	$t_{TA,cap}$	All capture inputs, Minimum pulse duration required for capture		20			ns
Timer_B							
Timer_B input clock frequency	f_{TA}	Internal: SMCLK, ACLK, External: TBCLK Duty cycle = 50% ± 10%	2 V, 3 V			24	MHz
Timer_B capture timing	$t_{TA,cap}$	All capture inputs, Minimum pulse duration required for capture		20			ns
eUSCI (UART Mode) Recommended Operating Conditions							
eUSCI input clock frequency	f_{eUSCI}	Internal: SMCLK, ACLK, External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
BITCLK clock frequency (equals baud rate in MBaud)	f_{BITCLK}					5	
eUSCI (UART Mode)							
UART receive deglitch time 48/	t_t	UCGLITx = 0	2 V, 3 V	5	15	20	ns
		UCGLITx = 1		20	45	60	
		UCGLITx = 2		35	80	120	
		UCGLITx = 3		50	110	180	
eUSCI (SPI Master Mode) Recommended Operating Conditions							
eUSCI input clock frequency	f_{eUSCI}	Internal: SMCLK, ACLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
eUSCI (SPI Master Mode) 49/							
STE lead time, STE active to	$t_{STE,LEAD}$	UCSTEM = 0, UCMODEx = 01 or 10	2 V, 3 V	1			UCxCLK
clock		UCSTEM = 1, UCMODEx = 01 or 10		1			cycles
STE lag time, Last clock to	$t_{STE,LAG}$	UCSTEM = 0, UCMODEx = 01 or 10		1			
STE inactive		UCSTEM = 1, UCMODEx = 01 or 10		1			
STE access time, STE active	$t_{STE,ACC}$	UCSTEM = 0, UCMODEx = 01 or 10				55	ns
to SIMO data out		UCSTEM = 1, UCMODEx = 01 or 10				35	
STE disable time, STE inactive	$t_{STE,DIS}$	UCSTEM = 0, UCMODEx = 01 or 10				40	
to SIMO high impedance		UCSTEM = 1, UCMODEx = 01 or 10				30	
SOMI input data setup time	$t_{SU,MI}$		2 V	35			
			3 V	35			
SOMI input data hold time	$t_{HD,MI}$		2 V	0			
			3 V	0			
SIMO output data valid time	$t_{VALID,MO}$	UCLK edge to SIMO valid,	2 V			30	
50/		C_L = 20 pF	3 V			30	
SIMO output data hold time	$t_{HD,MO}$	C_L = 20 pF	2 V	0			
51/			3 V	0			
eUSCI (SPI Slave Mode) 52/							
STE lead time, STE active to	$t_{STE,LEAD}$		2 V	7			ns
clock			3 V	7			
STE lag time, Last clock to STE	$t_{STE,LAG}$		2 V	0			
inactive			3 V	0			
STE access time, STE active to	$t_{STE,ACC}$		2 V			65	
SOMI data out			3 V			40	
STE disable time, STE inactive	$t_{STE,DIS}$		2 V			40	
to SOMI high impedance			3 V			35	
SIMO input data setup time	$t_{SU,SI}$		2 V	2			
			3 V	2			
SIMO input data hold time	$t_{HD,SI}$		2 V	5			
			3 V	5			
SOMI output data valid time (	$t_{VALID,SO}$	UCLK edge to SOMI valid,	2 V			30	
		CL = 20 pF	3 V			30	
SOMI output data hold time	$t_{HD,SO}$	CL = 20 pF	2 V	4			
			3 V	4			

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
eUSCI (I2C Mode) see FIGURE 13.							
eUSCI input clock frequency	f_{eUSCI}	Internal: SMCLK, ACLK, External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
SCL clock frequency	f_{SCL}		2 V, 3 V	0		400	kHz
Hold time (repeated) START	$t_{HD,STA}$	f_{SCL} = 100 kHz		4.0			µs
		f_{SCL} > 100 kHz		0.6			
Setup time for a repeated START	$t_{SU,STA}$	f_{SCL} = 100 kHz		4.7			
		f_{SCL} > 100 kHz		0.6			
Data hold time	$t_{HD,DAT}$			0			ns
Data setup time	$t_{SU,DAT}$			250			
Setup time for STOP	$t_{SU,STO}$	f_{SCL} = 100 kHz		4.0			µs
		f_{SCL} > 100 kHz		0.6			
Pulse duration of spikes suppressed by input filter	t_{SP}	UCGLITx = 0		50		600	ns
		UCGLITx = 1		25		300	
		UCGLITx = 2		12.5		150	
		UCGLITx = 3		6.25		75	
Clock low timeout	$t_{TIMEOUT}$	UCCLTOx = 1			27		ms
		UCCLTOx = 2			30		
		UCCLTOx = 3			33		
10-Bit ADC, Power Supply and Input Range Conditions							
Analog supply voltage	AV_{CC}	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.0		3.6	V
Analog input voltage range	$V_{(Ax)}$	All ADC10 pins		0		AV_{CC}	
Operating supply current into AVCC terminal, reference current not included	I_{ADC10_A}	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0	2 V		90	150	µA
			3 V		100	170	
Input capacitance	C_I	Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad			6		pF
Input MUX ON resistance	R_I	$AV_{CC} \geq 2$ V, $0 \text{ V} \leq V_{Ax} \leq AV_{CC}$				36	kΩ

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
10-Bit ADC, Timing Parameters							
	$f_{ADC10CLK}$	For specified performance of ADC10 linearity parameters	2 V to 3.6 V	0.45	5	5.5	MHz
Internal ADC10 oscillator (MODOSC)	$f_{ADC100SC}$	ADC10DIV = 0, $f_{ADC10CLK} = f_{ADC10OSC}$	2 V to 3.6 V	4.2	4.5	5.7	
Conversion time	$t_{CONVERT}$	REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, $f_{ADC10OSC}$ = 4.5 MHz to 5.5 MHz	2 V to 3.6 V	2.18		2.67	µs
		External $f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK, ADC10SSEL ≠ 0	2 V to 3.6 V		55/		
Turn on settling time of the ADC	$t_{ADC10ON}$	The error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB, Reference and input signal already settled				100	ns
Sampling time	t_{Sample}	R_S = 1000 Ω, R_I = 36000 Ω, C_I = 3.5 pF, Approximately eight Tau (T) are required to get an error of less than ±0.5 LSB	2 V 3 V	1.5 2.0			µs
10-Bit ADC, Linearity Parameters							
Integral linearity error	E_I	1.4 V ≤ (V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)min ≤ 1.6 V	2 V to 3.6 V	-1.4		1.4	LSB
		1.6 V < (V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)min ≤ V_{AVCC}		-1.3		1.3	
Differential linearity error	E_D	(V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)min ≤ (V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)	2 V to 3.6 V	-1.2		1.2	
Offset error	E_O	(V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)min ≤ (V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)	2 V to 3.6 V		±2.5		mV
Gain error, external reference	E_G	(V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)min ≤ (V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)	2 V to 3.6 V	-1.4		1.4	LSB
Gain error, internal reference					±4		%
Total unadjusted error, external reference	E_T	(V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)min ≤ (V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)	2 V to 3.6 V		±2.3		LSB
Total unadjusted error, internal reference 56/					±4		%

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
REF, External Reference 57/							
Positive external reference voltage input	V_{eREF+}	$V_{eREF+} > V_{eREF-}$ 58/		1.4		AV_{CC}	V
Negative external reference voltage input	V_{eREF-}	$V_{eREF+} > V_{eREF-}$ 59/		0		1.2	
Differential external reference voltage input	($V_{eREF+} - V_{REF-}/V_{eREF-}$)	$V_{eREF+} > V_{eREF-}$ 60/		1.4		AV_{CC}	
Static input current	I_{VeREF+}, I_{VeREF-}	1.4 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 1h, Conversion rate 200 ksps	2 V, 3 V		±6		µA
		1.4 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 1h, Conversion rate 200 ksps			±1		
Capacitance at VREF+ or VREF- terminal 61/	C_{VREF+}, C_{VREF-}				10		µF
REF, Built-In Reference							
Positive built-in reference voltage output	VREF+	REFVSEL = {2} for 2.5 V, REFON = 1	3 V	2.39	2.5	2.61	V
		REFVSEL = {1} for 2 V, REFON = 1		1.91	2.0	2.09	
		REFVSEL = {0} for 1.5 V, REFON = 1		1.43	1.5	1.57	
AVCC minimum voltage, Positive built-in reference active	$AV_{CC(min)}$	REFVSEL = {0} for 1.5 V		2.0			
		REFVSEL = {1} for 2 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
Operating supply current into AVCC terminal 62/	I_{REF+}	fADC10CLK = 5 MHz REFON = 1, REFBURST = 0	3 V		33		µA
Temperature coefficient of built-in reference	T_{REF+}	REFVSEL = (0, 1, 2}, REFON = 1			±35		ppm/ °C
Power supply rejection ratio (DC)	PSRR_DC	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, T_A = 25°C, REFON = 1, REFVSEL = (0} for 1.5 V			1600		µV/V
		AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, T_A = 25°C, REFON = 1, REFVSEL = (1} for 2 V			1900		
		AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, T_A = 25°C, REFON = 1, REFVSEL = (2} for 2.5 V			3600		
Settling time of reference voltage 63/	t_{SETTLE}	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, REFVSEL = (0, 1, 2}, REFON = 0 → 1			30		µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
REF, Temperature Sensor and Built-In V_{MID}							
64/	V_{SENSOR}	ADC10ON = 1, INCH = 0Ah, T_A = 0°C	2 V, 3 V		790		
	TC_{SENSOR}	ADC10ON = 1, INCH = 0Ah	2 V, 3 V		2.55		mV/°C
Sample time required if channel 10 is selected 65/	$t_{SENSOR(sample)}$	ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2 V	30			µs
			3V	30			
AVCC divider at channel 11	V_{MID}	ADC10ON = 1, INCH = 0Bh, VMID is ~0.5 × V_{AVCC}	2 V	0.96	1.0	1.04	V
			3V	1.43	1.5	1.57	
Sample time required if channel 11 is selected 66/	$t_{VMID(sample)}$	ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2 V, 3 V	1000			ns
Comparator_D							
Propagation delay, AVCC = 2 V to 3.6 V	t_{pd}	Overdrive = 10 mV, VIN- = (VIN+ – 400 mV) to (VIN+ + 10 mV)		49	100	202	ns
		Overdrive = 100 mV, VIN- = (VIN+ – 400 mV) to (VIN+ + 100 mV)			80		
		Overdrive = 250 mV, VIN- = (VIN+ – 400 mV) to (VIN+ + 250 mV)			50		
Filter timer added to the propagation delay of the comparator	t_{filter}	CDF = 1, CDFDLY = 00		0.28	0.5	1.1	µs
		CDF = 1, CDFDLY = 01		0.49	0.9	1.8	
		CDF = 1, CDFDLY = 10		0.85	1.6	3.31	
		CDF = 1, CDFDLY = 11		1.59	3.0	6.5	
Input offset	V_{offset}	AVCC = 2 V to 3.6 V		-26		26	mV
Common mode input range	V_{ic}	AVCC = 2 V to 3.6 V		0		AVCC - 1	V
Comparator only	$I_{comp(AVCC)}$	CDON = 1, AVCC = 2 V to 3.6 V			28		µA
Reference buffer and R-ladder	$I_{ref(AVCC)}$	CDREFLx = 01, AVCC = 2 V to 3.6 V			20		µA
Comparator enable time	$t_{enable,comp}$	CDON = 0 to CDON = 1, AVCC = 2 V to 3.6 V			1.1	2.3	µs
Resistor ladder enable time	$t_{enable,rladder}$	CDON = 0 to CDON = 1, AVCC = 2 V to 3.6 V			1.1	2.3	
Reference voltage for a tap	V_{CB_REF}	VIN = voltage input to the R-ladder, n = 0 to 31		VIN x (n +0.49) / 32	VIN x (n + 1) / 32	VIN x (n + 1.51) / 32	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 11/	V_{CC}	Limits			Unit
				Min	Typ	Max	
FRAM							
Write supply voltage	$DV_{CC(WRITE)}$			2.0		3.6	V
Word or byte write time	t_{WRITE}					120	ns
Read access time 67/	t_{ACCESS}					60	
Precharge time 67/	$t_{PRECHARGE}$					60	
Cycle time, read or write operation 67/	t_{CYCLE}			120			
Read and write endurance				10^{15}			cycles
Data retention duration	$t_{Retention}$	T_J = 25°C		100			years
		T_J = 70°C		40			
		T_J = 85°C		10			
JTAG and Spy-Bi-Wire Interface							
Spy-Bi-Wire input frequency	f_{SBW}		2 V, 3 V	0		20	MHz
Spy-Bi-Wire low clock pulse duration	$t_{SBW,Low}$		2 V, 3 V	0.025		15	µs
Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)	$t_{SBW, En}$		2 V, 3 V			1	
Spy-Bi-Wire return to normal operation time	$t_{SBW,Rst}$			18		37	
TCK input frequency, 4-wire JTAG	f_{TCK}		2 V	0		5	MHz
			3V	0		10	MHz
Internal pulldown resistance on TEST	$R_{internal}$		2 V, 3 V	19	35	51.5	kΩ

See footnote at end of table.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over recommended operating free-air temperature (unless otherwise noted).

3/ All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.

4/ The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.

5/ Characterized with program executing typical data processing.

6/ At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency, $f_{MCLK,eff}$, decreases. The effective MCLK frequency is also dependent on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio. The following equation can be used to compute $f_{MCLK,eff}$:
$f_{MCLK,eff,MHz} = f_{MCLK,MHz} \times 1 / [\#\text{ of wait states} \times ((1 - \text{cache hit ratio percent}/100)) + 1]$.

7/ Program and data reside entirely in FRAM. No wait states enabled. DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz). MCLK = SMCLK.

8/ Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 25% ratio implies one of every four accesses is from cache, the remaining are FRAM accesses.
For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz). MCLK = SMCLK. No wait states enabled.
For 16 MHz, DCORSEL = 1, DCOFSELx = 0 (f_{DCO} = 16 MHz).MCLK = SMCLK. One wait state enabled.
For 20 MHz, DCORSEL = 1, DCOFSELx = 2 (f_{DCO} = 20 MHz).MCLK = SMCLK. Three wait states enabled.
For 24 MHz, DCORSEL = 1, DCOFSELx = 3 (f_{DCO} = 24 MHz).MCLK = SMCLK. Three wait states enabled.

9/ See FIGURE 4 for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in manufacturer data.
f_{ACLK} = 32786 Hz, $f_{MCLK} = f_{SMCLK}$ at specified frequency. No peripherals active.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.

10/ All execution is from RAM.
For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 (fDCO = 8 MHz). MCLK = SMCLK.
For 16 MHz, DCORSEL = 1, DCOFSELx = 0 (f_{DCO} = 16 MHz). MCLK = SMCLK.
For 20 MHz, DCORSEL = 1, DCOFSELx = 2 (f_{DCO} = 20 MHz). MCLK = SMCLK.
For 24 MHz, DCORSEL = 1, DCOFSELx = 3 (f_{DCO} = 24 MHz). MCLK = SMCLK

11/ Over recommended ranges of supply voltage and operating at $-40°C \le T_J \le 80°C$ (unless otherwise noted).

12/ Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = 1 MHz. DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz).

13/ Current for brownout, high-side supervisor (SVSH) and low-side supervisor (SVSL) included.

14/ Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = 8 MHz. DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz).

15/ Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = 24 MHz. DCORSEL = 1, DCOFSELx = 3 (f_{DCO} = 24 MHz).

16/ Current for watchdog timer (clocked by ACLK) and RTC (clocked by XT1 LF mode) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 0 MHz, DCORSEL = 0, DCOFSELx = 3, DCO bias generator enabled.

17/ Current for brownout, high-side supervisor (SVSH) included. Low-side supervisor disabled (SVSL).

18/ Current for watchdog timer (clocked by ACLK) and RTC (clocked by XT1 LF mode) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ = 0 MHz.

19/ Current for watchdog timer (clocked by ACLK) included. ACLK = VLO.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ = 0 MHz

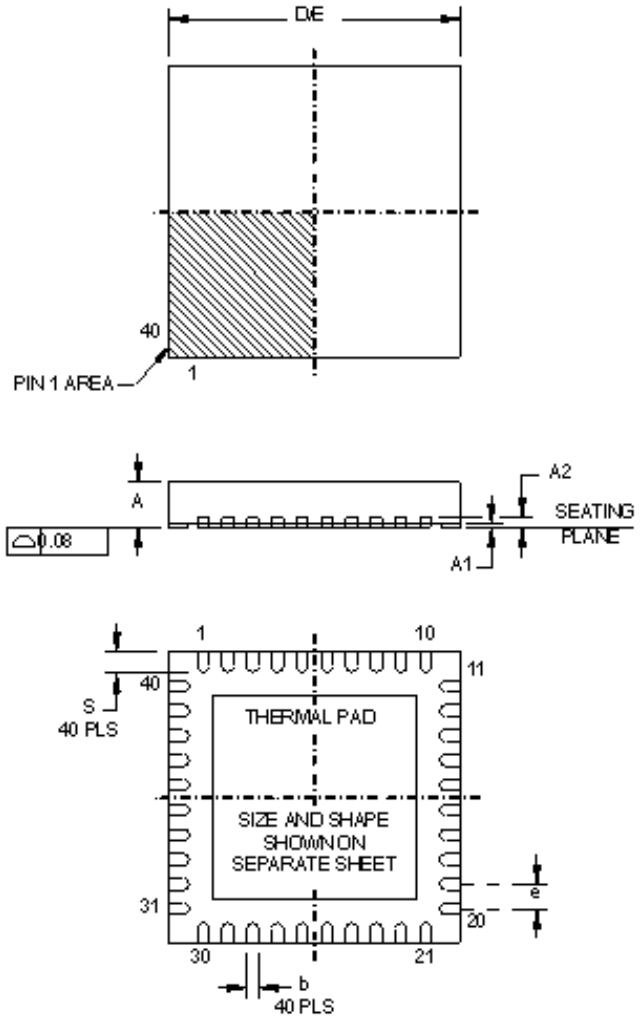
20/ CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), fDCO = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz.
21/ Internal regulator disabled. No data retention. RTC active clocked by XT1 LF mode.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM3.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
22/ Internal regulator disabled. No data retention.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
23/ Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
24/ An external signal sets the interrupt flag every time the minimum interrupt pulse duration t(int) is met. It may be set by trigger signals shorter than $t_{(int)}$.
25/ The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
26/ The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
27/ The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
28/ The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.
29/ A resistive divider with 2 × 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected from the output to V_{SS}.
30/ The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.
31/ To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

32/ When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of the manufacturer data sheet.
33/ Maximum frequency of operation of the entire device cannot be exceeded.
34/ Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVE = {0}, $C_{L,eff} \le 6$ pF.
- For XT1DRIVE = {1}, 6 pF ≤ $C_{L,eff} \le 9$ pF.
- For XT1DRIVE = {2}, 6 pF ≤ $C_{L,eff} \le 10$ pF.
- For XT1DRIVE = {3}, 6 pF ≤ $C_{L,eff} \le 12$ pF

35/ Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
36/ Measured with logic-level input frequency but also applies to operation with crystals.
37/ Includes startup counter of 4096 clock cycles.
38/ Requires external capacitors at both terminals.
39/ Values are specified by crystal manufacturers. Include parasitic bond and package capacitance (approximately 2 pF per pin). Recommended values supported are 6 pF, 9 pF, and 12 pF. Maximum shunt capacitance of 1.6 pF.
40/ Oscillation allowance is based on a safety factor of 5 for recommended crystals.
41/ Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
42/ Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF.
43/ Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
44/ Calculated using the box method: (MAX(2.0 to 3.6 V) – MIN(2.0 to 3.6 V)) / MIN(2.0 to 3.6 V) / (3.6 V – 2 V)
45/ The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

46/ The wake-up time is measured from the rising edge of the $\overline{RST}$ signal until the first instruction of the user program is executed.
47/ Meeting or exceeding this time makes sures a reset event occurs. Pulses shorter than this minimum time may or may not cause a reset event to occur.
48/ Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.
49/ $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$. For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ see the SPI parameters of the attached slave.
50/ Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagramsin FIGURE 9 and FIGURE 10.
51/ Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in FIGURE 9 and FIGURE 10.
52/ $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tLO/HI \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$. For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.
53/ Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in FIGURE 11 and FIGURE 12.
54/ Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in FIGURE 11 and FIGURE 12.
55/ $12 \times ADC10DIV \times 1/f_{ADC10CLK}$
56/ Error is dominated by the internal reference.
57/ The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, Ci, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
58/ The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
59/ The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
60/ The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
61/ Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_B.
62/ The internal reference current is supplied by terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
63/ The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.
64/ The temperature sensor offset can vary significantly. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
65/ The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
66/ The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.
67/ When using manual wait state control, see manufacturer data for recommended settings for common system frequencies.
68/ Tools accessing the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
69/ f_{TCK} may be restricted to meet the timing requirements of the module selected.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.08	1.00	D/E	5.85	6.15
A1	0.00	0.05	e	0.50 BSC	
A2	0.20 NOM		S	0.30	0.50
b	0.18	0.30			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the board for thermal and mechanical performance.
4. See the additional figure in the manufacturer data sheet for details regarding the exposed thermal pad features and dimensions.
5. Package complies to JEDEC MO-220 variation VJJD-2..

FIGURE 1. Case outline.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P1.0/TA0.1/DMAE0/RTCCLK/A0*/CD0/VeREF-	40	AVCC
2	P1.1/TA0.2/TA1CLK/CDOUT/A1*/CD1/VeREF+	39	AVSS
3	P1.2/TA1.1/TA0CLK/CDOUT/A2*/CD2	38	PJ.5/XOUT
4	P3.0/A12*/CD12	37	PJ.4/XIN
5	P3.1/A13*/CD13	36	AVSS
6	P3.2/A14*/CD14	35	P2.4/TA1.0/UCA1CLK/A7*/CD11
7	P3.3/A15*/CD15	34	P2.3/TA0.0/UCA1STE/A6*/CD10
8	P1.3/TA1.2/UCB0STE/A3*/CD3	33	P2.7
9	P1.4/TB0.1/UCA0STE/A4*/CD4	32	DVCC
10	P1.5/TB0.2/UCA0CLK/A5*/CD5	31	DVSS
11	PJ.0/TDO/TB0OUTH/SMCLK/CD6	30	VCORE
12	PJ.1/TDI/TCLK/TB1OUTH/MCLK/CD7	29	P1.7/TB1.2/UCB0SOMI/UCB0SCL/TA1.0
13	PJ.2/TMS/TB2OUTH/ACLK/CD8	28	P1.6/TB1.1/UCB0SIMO/UCB0SDA/TA0.0
14	PJ.3/TCK/CD9	27	P3.7/TB2.2
15	P4.0/TB2.0	26	P3.6/TB2.1/TB1CLK
16	P4.1	25	P3.5/TB1.2/CDOUT
17	P2.5/TB0.0/UCA1TXD/UCA1SIMO	24	P3.4/TB1.1/TB2CLK/SMCLK
18	P2.6/TB1.0/UCA1RXD/UCA1SOMI	23	P2.2/TB2.2/UCB0CLK/TB1.0
19	TEST/SBWTCK	22	P2.1/TB2.1/UCA0RXD/UCA0SOMI/TB0.0
20	$\overline{\text{RST}}$/NMI/SBWTDIO	21	P2.0/TB2.0/UCA0TXD/UCA0SIMO/TB0CLK/ACLK

NOTES:

* Not available on MSP430FR5739-EP

Exposed thermal pad connection to VSS recommended.

FIGURE 2. Terminal connections.

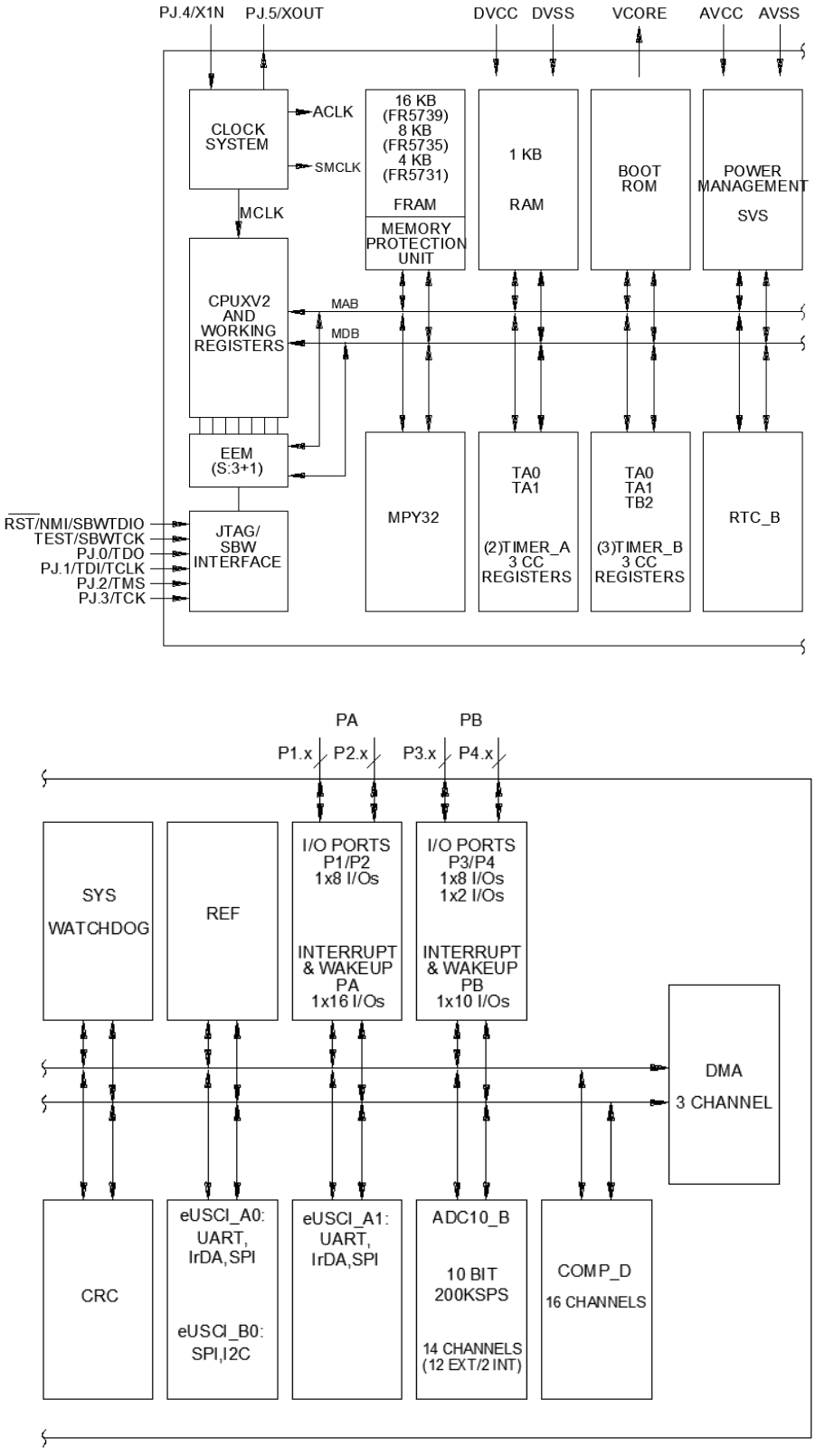


FIGURE 3. Functional block diagram.

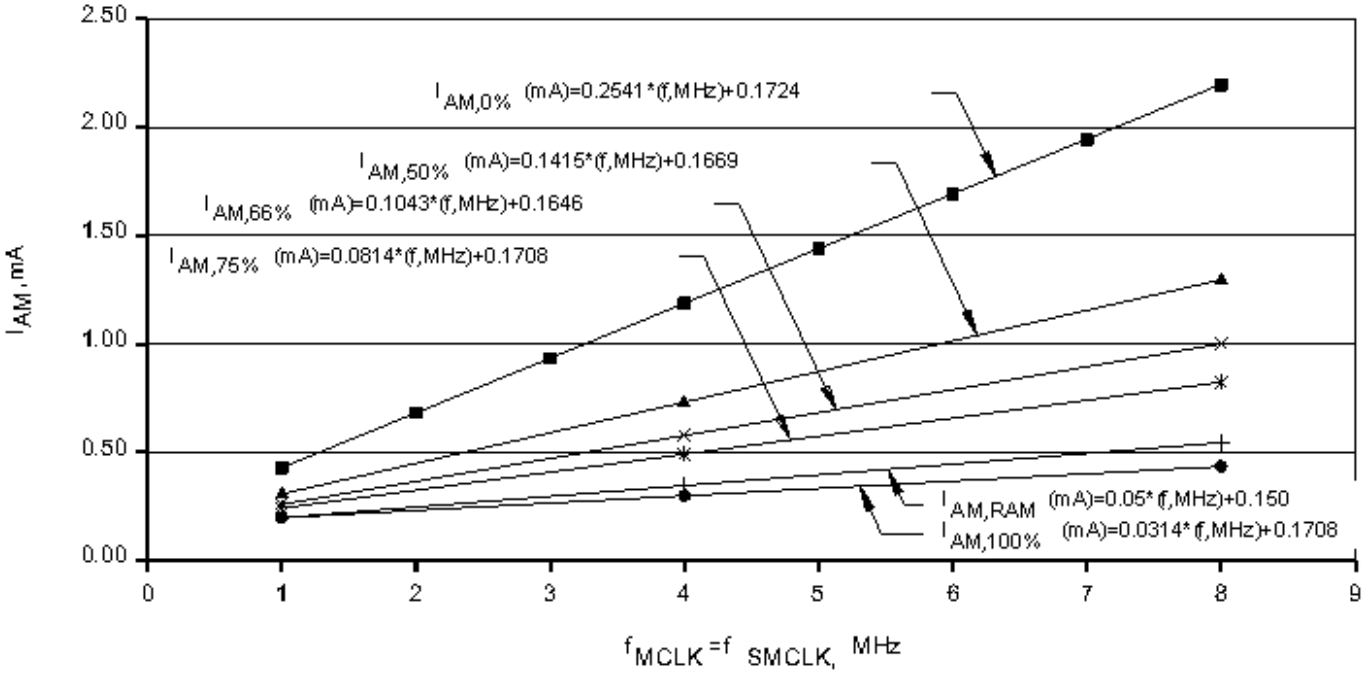


FIGURE 4. Typical Active mode supply currents, No Wait states.

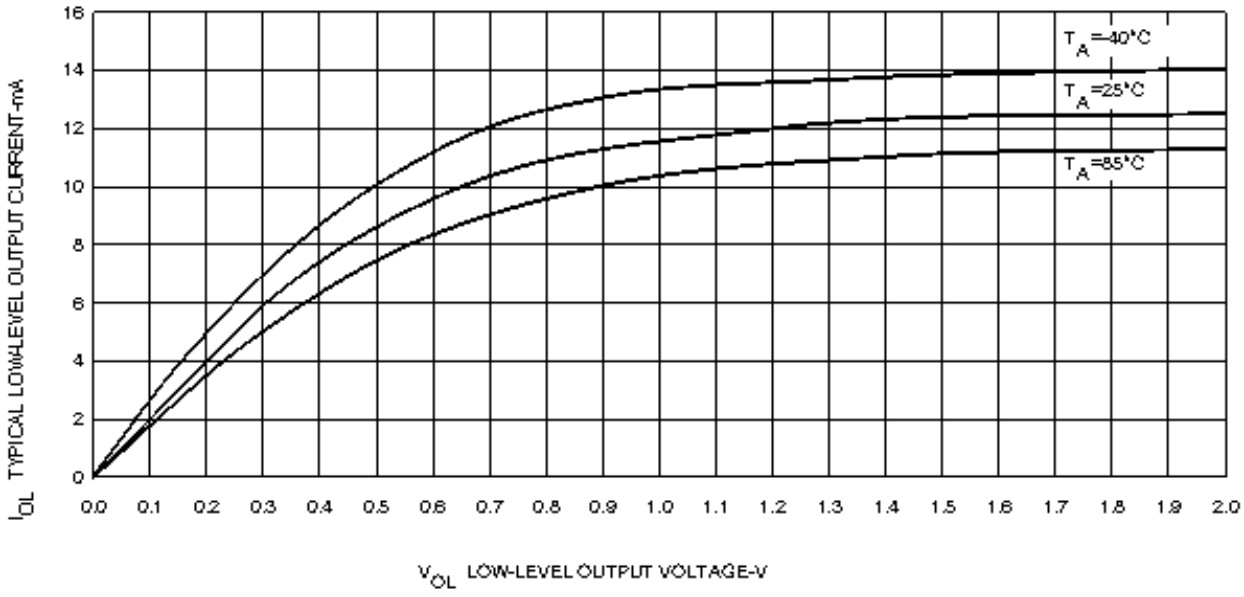


FIGURE 5. Typical Low-Level Output Current vs Low-Level Output Voltage, V_{CC} = 2.0 V.

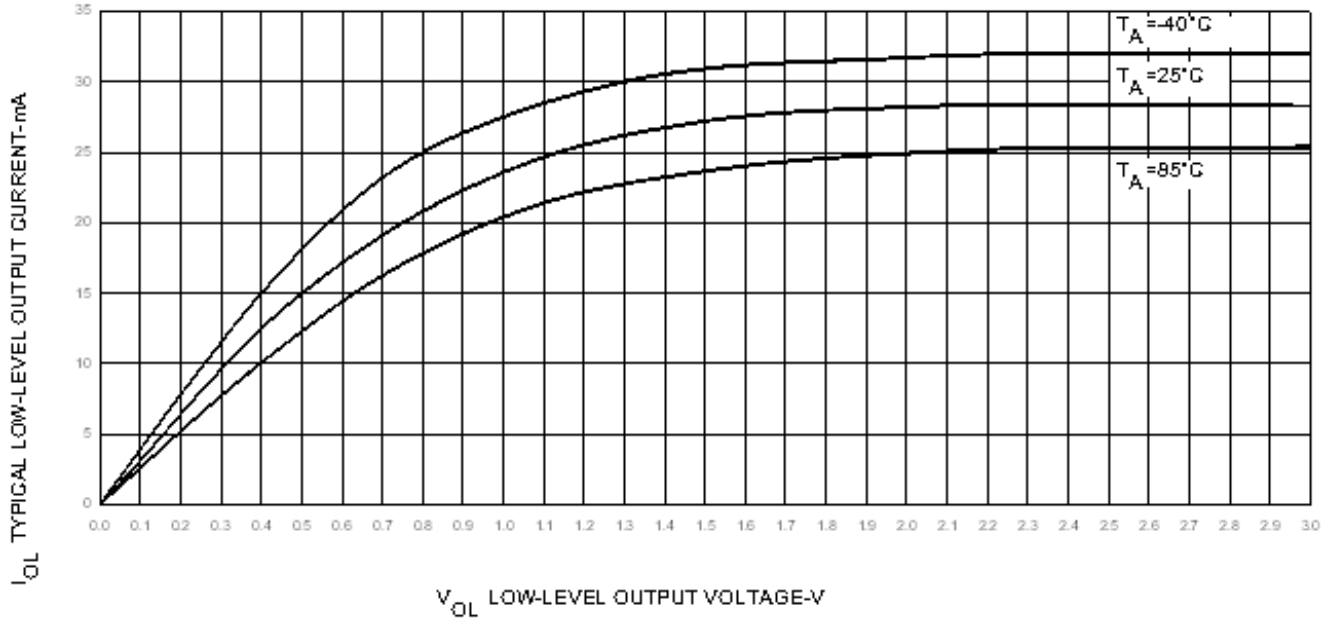


FIGURE 6. Typical Low-Level Output Current vs Low-Level Output Voltage V_{CC} = 3.0 V.

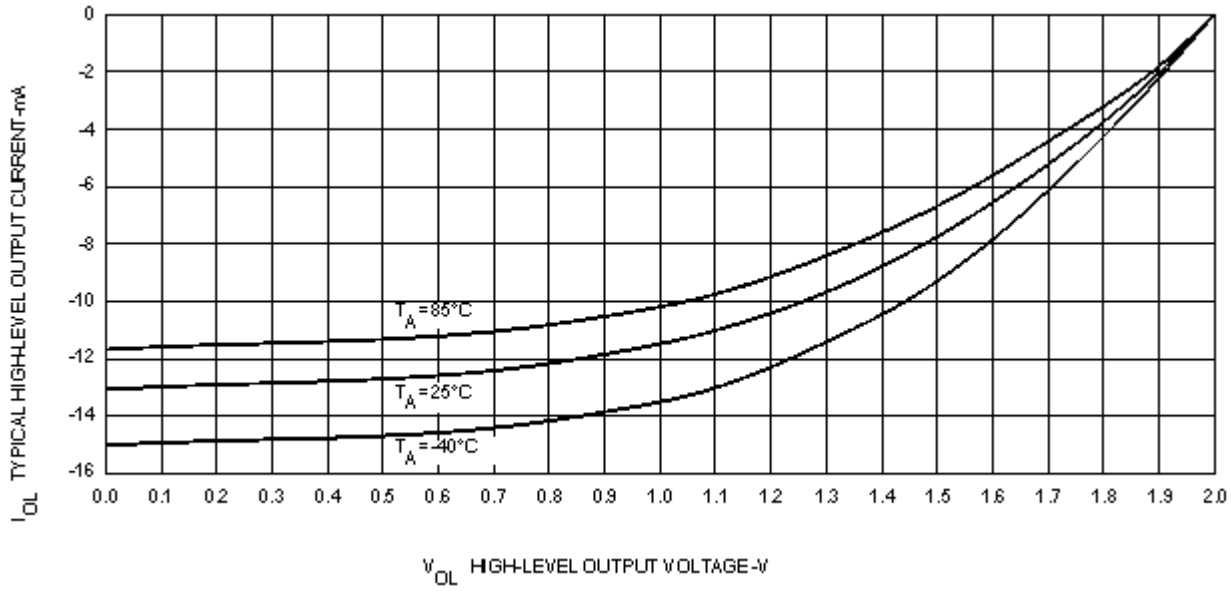


FIGURE 7. Typical High-Level Output Current vs High-Level Output Voltage, V_{CC} = 2.0 V.

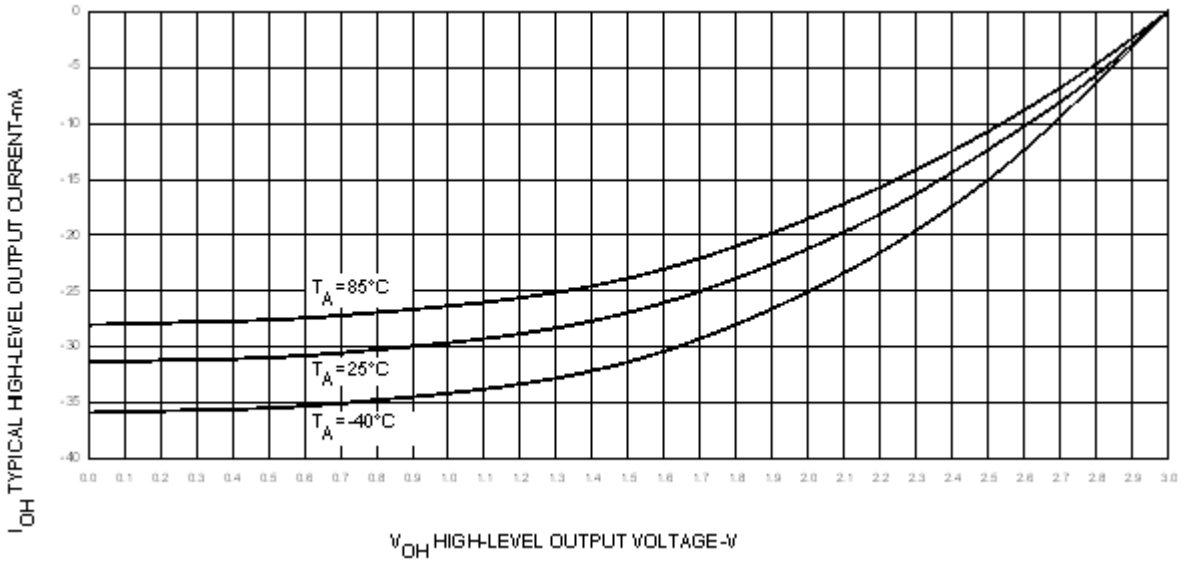


FIGURE 8. Typical High-Level Output Current vs High-Level Output Voltage, V_{CC} = 3.0 V.

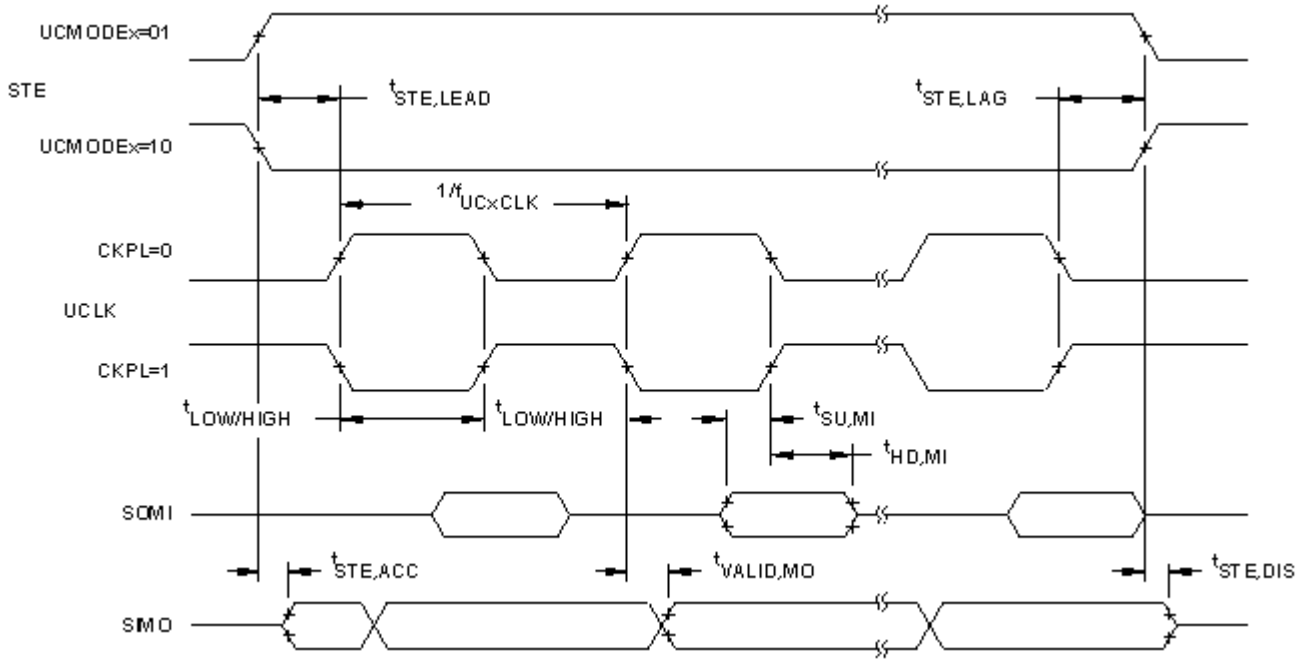


FIGURE 9. SPI Master mode, CKPH = 0.

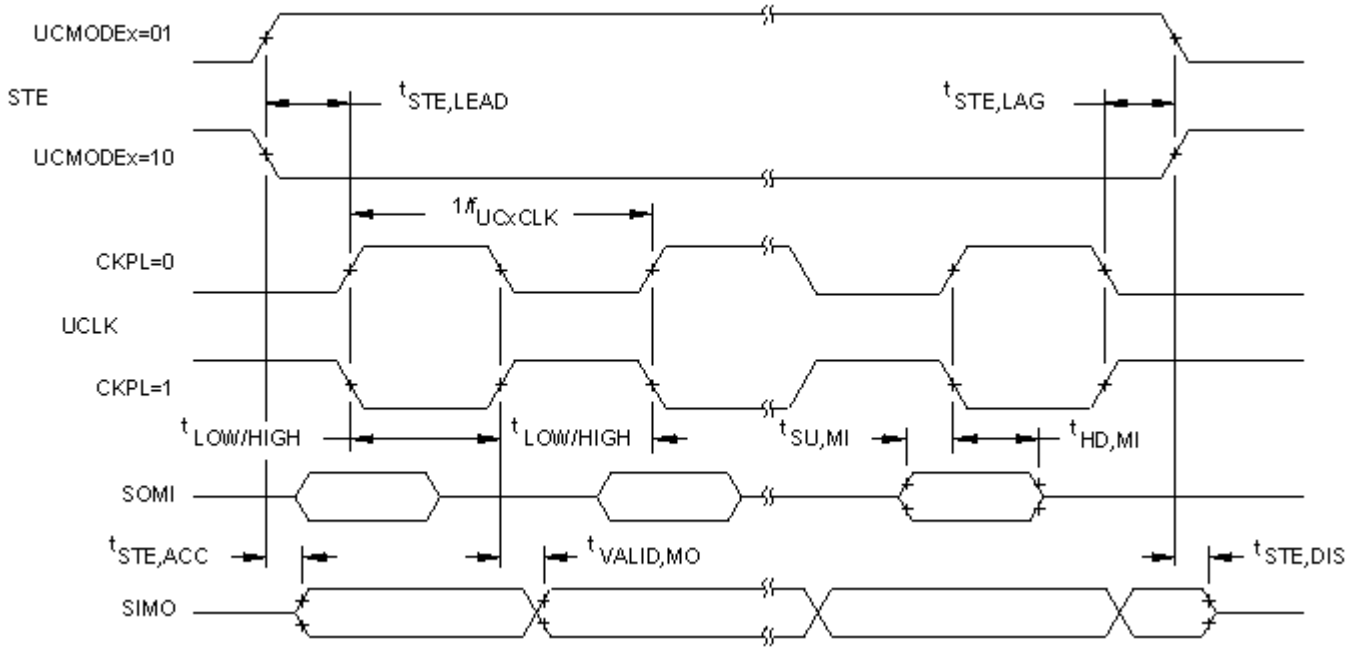


FIGURE 10. SPI Master mode, CKPH = 1.

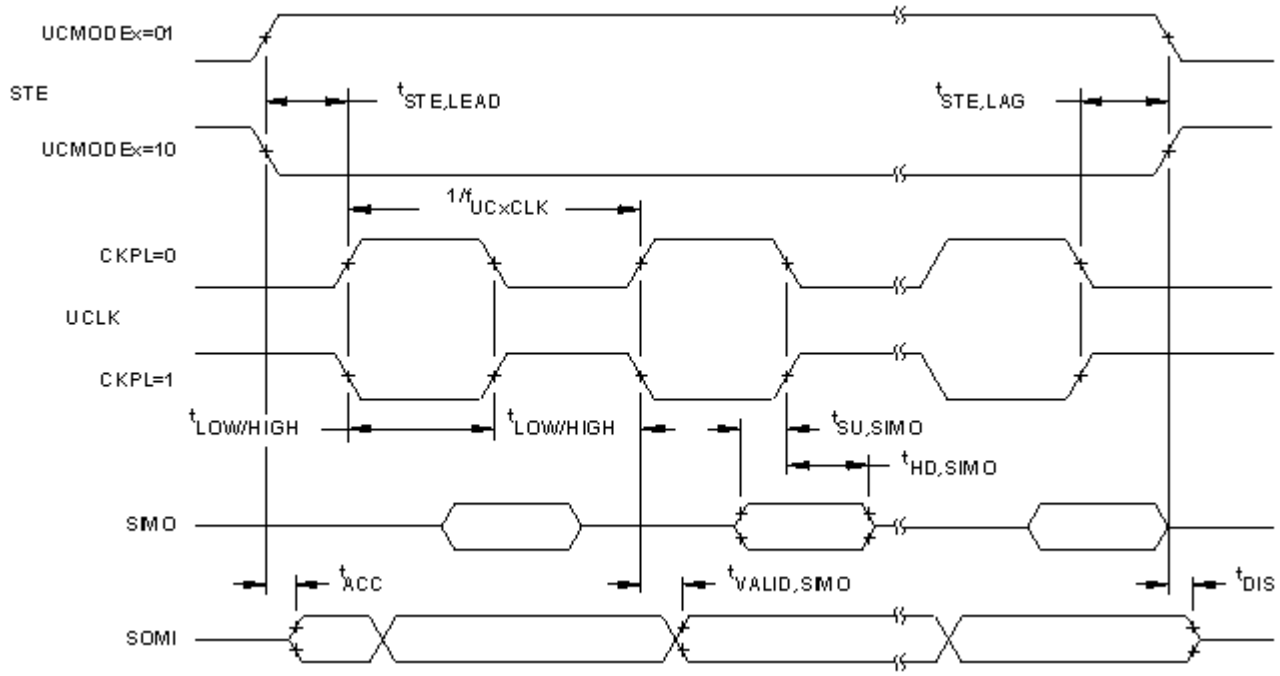


FIGURE 11. SPI Slave mode, CKPH = 0.

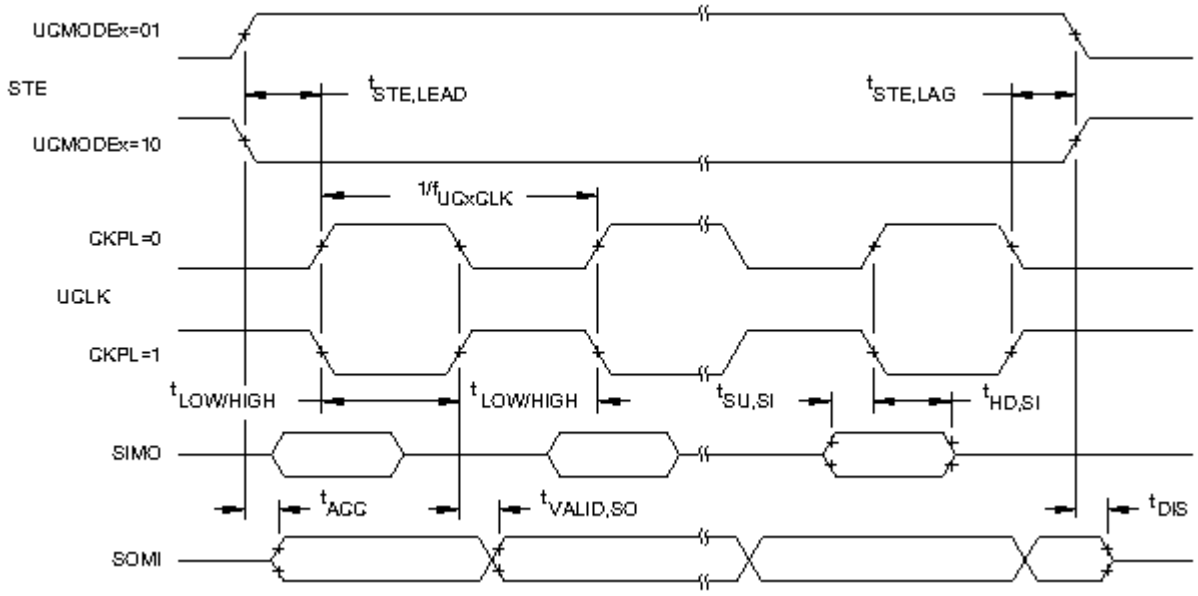


FIGURE 12. SPI Slave mode, CKPH = 1.

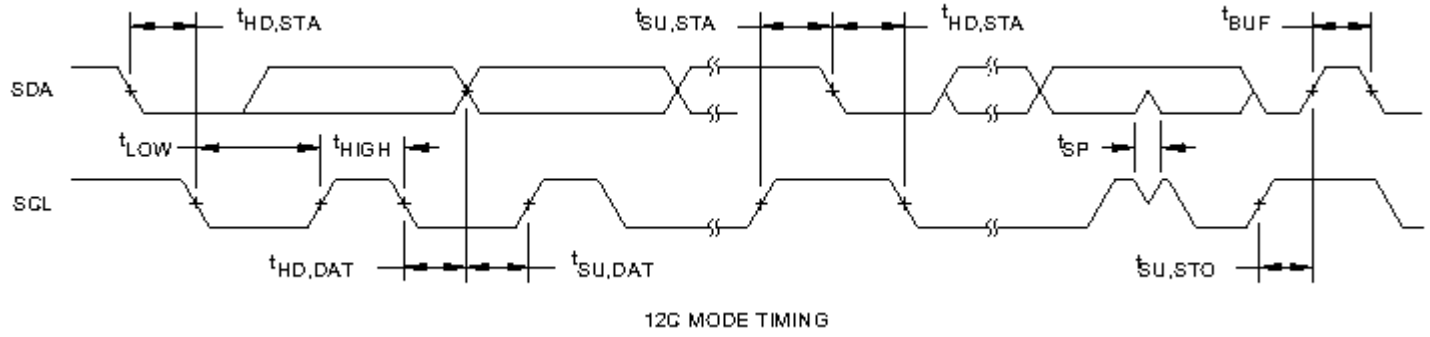


FIGURE 13. I2C mode timing.

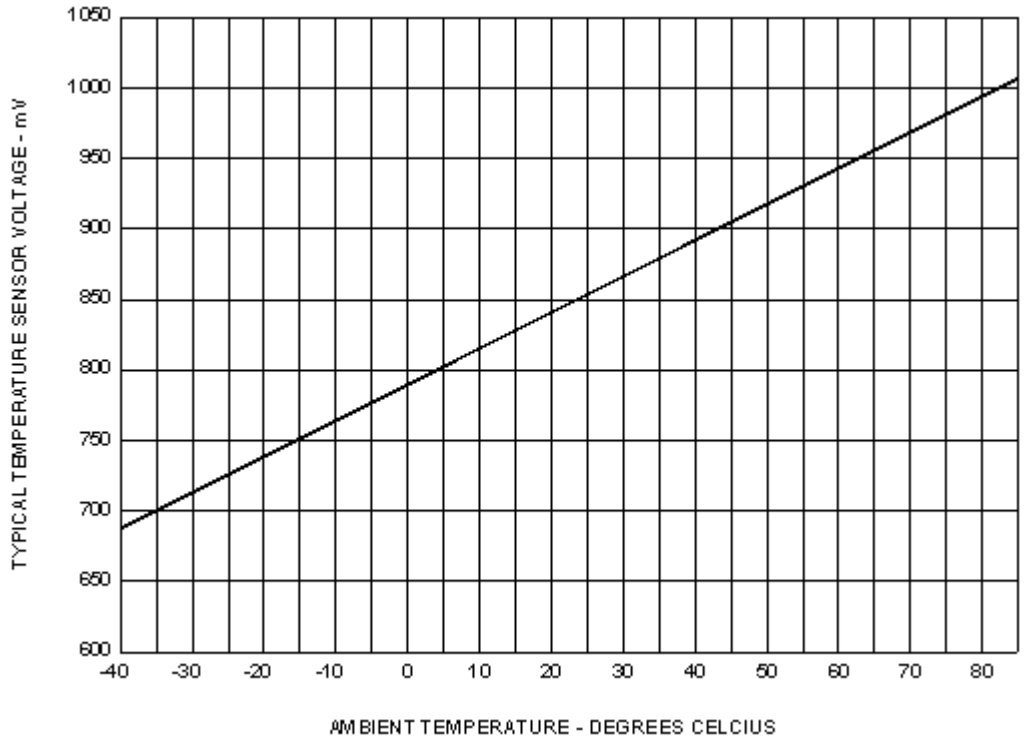


FIGURE 14. Typical temperature sensor voltage.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/14644-01XE	01295	M430FR5739SRHATEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243