



1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal, 14 bit, 65 million samples per second (MSPS), serial low voltage differential signaling (LVDS), 1.8 V analog to digital converter (ADC) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/14637</u>	-	<u>01</u>	X	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	AD9257-EP	Octal, 14 bit, 65 MSPS, serial LVDS, 1.8 V analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	64	MO-220-WMMD	Lead frame chip scale package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		<b>REV</b>	<b>PAGE 2</b>

1.3 Absolute maximum ratings. 1/

Analog supply (AVDD) to analog ground (AGND) .....	-0.3 V to +2.0 V
Digital output driver supply (DRVDD) to AGND .....	-0.3 V to +2.0 V
Digital outputs (D±x, DCO+, DCO-, FCO+, FCO-) to AGND .....	-0.3 V to +2.0 V
Input clock true (CLK+), input clock complement (CLK-) to AGND .....	-0.3 V to +2.0 V
Analog input true (VIN+x), analog input complement (VIN-x) to AGND .....	-0.3 V to +2.0 V
Serial clock (SCLK) / digital test pattern (DTP), serial data input/output (SDIO) / data select format (DFS), chip select bar (CSB) to AGND .....	-0.3 V to +2.0 V
Digital input (SYNC), power down (PDWN) to AGND .....	-0.3 V to +2.0 V
Analog current bias setting (RBIAS), VIN to AGND .....	-0.3 V to +2.0 V
Voltage reference input/output (VREF), reference mode selection (SENSE) to AGND .....	-0.3 V to +2.0 V
Maximum junction temperature (T <sub>J</sub> ) .....	150°C
Lead temperature (soldering, 10 seconds) .....	300°C
Storage temperature range (T <sub>STG</sub> ) .....	-65°C to +150°C

1.4 Recommended operating conditions. 2/

Operating ambient temperature range (T <sub>A</sub> ) .....	-55°C to +125°C
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1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient 3/ 4/	θ <sub>JA</sub>	22.3	°C/W
Thermal resistance, junction-to-case 3/ 5/	θ <sub>JC</sub>	1.4	°C/W
Thermal resistance, junction-to-board 3/ 6/	θ <sub>JB</sub>	N/A	°C/W
Characterization parameter, junction-to-top 3/ 4/	ψ <sub>JT</sub>	0.1	°C/W

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 3/ Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
- 4/ Per JEDEC JESD 51-2 (still air) or JEDEC JESD 51-6 (moving air).
- 5/ Per MIL-STD-883, method 1012.1.
- 6/ Per JEDEC JESD 51-8 (still air).

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		<b>REV</b>	<b>PAGE 3</b>

## 2. APPLICABLE DOCUMENTS

### JEDEC Solid State Technology Association

- EIA/JEDEC 25-5 - Test board.
- EIA/JESD 51-2 - Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
- EIA/JEDEC 51-6 - Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)
- EIA/JEDEC 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- EIA/JESD 51-8 - Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
- JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

### DEPARTMENT OF DEFENSE STANDARDS

- MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figures 3, 4, 5, and 6.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		<b>REV</b>	<b>PAGE 4</b>

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
DC characteristics <u>2/</u>							
Resolution			+25°C	01	14		Bits
Accuracy							
No missing codes			-55°C to +125°C	01	Guaranteed		
Offset error	OE		-55°C to +125°C	01	-0.7	+0.1	%FSR
					-0.3 typical		
Offset matching	OM		-55°C to +125°C	01	0	0.6	%FSR
					0.23 typical		
Gain error	GE		-55°C to +125°C	01	-7.0	+1.0	%FSR
					-2.9 typical		
Gain matching	GM		-55°C to +125°C	01	-1.0	+5.0	%FSR
					+1.6 typical		
Differential nonlinearity	DNL		-55°C to +125°C	01	-0.95	+1.6	LSB
					±0.6 typical		
Integral nonlinearity	INL		-55°C to +125°C	01	-4.5	+4.5	LSB
					±1.1 typical		
Temperature drift offset error			-55°C to +125°C	01	±2 typical		ppm / °C
Internal voltage reference							
Output voltage (1 V mode)			-55°C to +125°C	01	0.98	1.01	V
					0.99 typical		
Load regulation at 1.0 mA		V <sub>REF</sub> = 1 V	-55°C to +125°C	01	2 typical		mV
Input resistance	R <sub>IN</sub>		-55°C to +125°C	01	7.5 typical		kΩ
Input referred noise		V <sub>REF</sub> = 1.0 V	+25°C	01	0.94 typical		LSB rms

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		<b>REV</b>	<b>PAGE 5</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
DC characteristics – continued. 2/							
Analog inputs							
Differential input voltage		V <sub>REF</sub> = 1 V	-55°C to +125°C	01	2 typical		Vp-p
Common mode voltage			-55°C to +125°C	01	0.9 typical		V
Common mode voltage range			-55°C to +125°C	01	0.5	1.3	V
Differential input resistance	RIN		+25°C	01	5.2 typical		kΩ
Differential input capacitance	CIN		-55°C to +125°C	01	3.5 typical		pF
Power supply							
1.8 V analog supply voltage	AVDD		-55°C to +125°C	01	1.7	1.9	V
					1.8 typical		
1.8 V digital output driver supply voltage	DRVDD		-55°C to +125°C	01	1.7	1.9	V
					1.8 typical		
Analog supply current	I <sub>AVDD</sub>		-55°C to +125°C	01		211	mA
					198 typical		
Digital output driver supply current (ANSI-644 mode)	IDRVDD		-55°C to +125°C	01		93	mA
					60 typical		
Digital output driver supply current (reduce range mode)	IDRVDD		+25°C	01	45 typical		mA
Total power consumption							
Total power dissipation		Eight channels, ANSI-644 mode	-55°C to +125°C	01		547	mW
					464 typical		
Total power dissipation		Eight channels, reduce range mode	+25°C	01	437 typical		mW
Power down dissipation			+25°C	01	1 typical		mW
Standby dissipation		Can be controlled via SPI	+25°C	01	92 typical		mW

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 6

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
AC specifications <u>3/</u>							
Signal to noise ratio	SNR	f <sub>IN</sub> = 9.7 MHz	+25°C	01	75.7 typical		dBFS
		f <sub>IN</sub> = 19.7 MHz	-55°C to +125°C		72.8		
					75.6 typical		
		f <sub>IN</sub> = 30.5 MHz	+25°C		75.5 typical		
		f <sub>IN</sub> = 63.5 MHz	+25°C		74.9 typical		
		f <sub>IN</sub> = 123.4 MHz	+25°C		73.2 typical		
Signal to noise and distortion ratio	SINAD	f <sub>IN</sub> = 9.7 MHz	+25°C	01	75.6 typical		dBFS
		f <sub>IN</sub> = 19.7 MHz	-55°C to +125°C		70.9		
					75.6 typical		
		f <sub>IN</sub> = 30.5 MHz	+25°C		75.4 typical		
		f <sub>IN</sub> = 63.5 MHz	+25°C		74.8 typical		
		f <sub>IN</sub> = 123.4 MHz	+25°C		72.8 typical		
Effective number of bits	ENOB	f <sub>IN</sub> = 9.7 MHz	+25°C	01	12.3 typical		Bits
		f <sub>IN</sub> = 19.7 MHz	-55°C to +125°C		11.5		
					12.3 typical		
		f <sub>IN</sub> = 30.5 MHz	+25°C		12.2 typical		
		f <sub>IN</sub> = 63.5 MHz	+25°C		12.1 typical		
		f <sub>IN</sub> = 123.4 MHz	+25°C		11.8 typical		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 7

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
AC specifications – continued. <u>3/</u>							
Spurious free dynamic range	SFDR	f <sub>IN</sub> = 9.7 MHz	+25°C	01	96 typical		dBc
		f <sub>IN</sub> = 19.7 MHz	-55°C to +125°C		78		
					96 typical		
		f <sub>IN</sub> = 30.5 MHz	+25°C		91 typical		
		f <sub>IN</sub> = 63.5 MHz	+25°C		95 typical		
		f <sub>IN</sub> = 123.4 MHz	+25°C		83 typical		
Worst harmonic (second or third)	SFDR	f <sub>IN</sub> = 9.7 MHz	+25°C	01	-99 typical		dBc
		f <sub>IN</sub> = 19.7 MHz	-55°C to +125°C			-78	
					-98 typical		
		f <sub>IN</sub> = 30.5 MHz	+25°C		-91 typical		
		f <sub>IN</sub> = 63.5 MHz	+25°C		-98 typical		
		f <sub>IN</sub> = 123.4 MHz	+25°C		-83 typical		
Worst other (excluding second or third)	SFDR	f <sub>IN</sub> = 9.7 MHz	+25°C	01	-96 typical		dBc
		f <sub>IN</sub> = 19.7 MHz	-55°C to +125°C			-86	
					-96 typical		
		f <sub>IN</sub> = 30.5 MHz	+25°C		-98 typical		
		f <sub>IN</sub> = 63.5 MHz	+25°C		-95 typical		
		f <sub>IN</sub> = 123.4 MHz	+25°C		-94 typical		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		<b>REV</b>	<b>PAGE 8</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
AC specifications – continued. <u>3/</u>							
Two tone intermodulation distortion (IMD) A <sub>IN1</sub> and A <sub>IN2</sub> = -7.0 dBFS		f <sub>IN1</sub> = 30 MHz, f <sub>IN2</sub> = 32 MHz	+25°C	01	92 typical		dBc
Crosstalk <u>4/</u>			+25°C	01	-98 typical		dB
Crosstalk <u>5/</u> (overrange condition)			+25°C	01	-94 typical		dB
Power supply <u>6/</u> rejection ratio	PSRR	AVDD	+25°C	01	52 typical		dB
		DRVDD			71 typical		
Analog input bandwidth, full power			+25°C	01	650 typical		MHz

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 9

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Digital specifications <u>2/</u> <u>7/</u>							
Clock inputs (CLK+, CLK-)							
Logic compliance		CMOS / LVDS / LVPECL					
Differential input <u>8/</u> voltage			-55°C to +125°C	01	0.2	3.6	V <sub>p-p</sub>
Input voltage range			-55°C to +125°C	01	AGND - 0.2	AVDD + 0.2	V
Input common mode voltage			-55°C to +125°C	01	0.9 typical		V
Input resistance (differential)	RIN		+25°C	01	15 typical		kΩ
Input capacitance	CIN		+25°C	01	4 typical		pF
Logic inputs (PDWN, SYNC, SCLK)							
Logic 1 voltage			-55°C to +125°C	01	1.2	AVDD + 0.2	V
Logic 0 voltage			-55°C to +125°C	01	0	0.8	V
Input resistance	RIN		+25°C	01	30 typical		kΩ
Input capacitance	CIN		+25°C	01	2 typical		pF
Logic inputs (CSB)							
Logic 1 voltage			-55°C to +125°C	01	1.2	AVDD + 0.2	V
Logic 0 voltage			-55°C to +125°C	01	0	0.8	V
Input resistance	RIN		+25°C	01	26 typical		kΩ
Input capacitance	CIN		+25°C	01	2 typical		pF
Logic input (SDIO)							
Logic 1 voltage			-55°C to +125°C	01	1.2	AVDD + 0.2	V
Logic 0 voltage			-55°C to +125°C	01	0	0.8	V
Input resistance	RIN		+25°C	01	26 typical		kΩ
Input capacitance	CIN		+25°C	01	5 typical		pF

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		<b>REV</b>	<b>PAGE 10</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Digital specifications – continued. <u>2/ 7/</u>							
Logic output (SDIO) <u>9/</u>							
Logic 1 voltage		I <sub>OH</sub> = 800 μA	-55°C to +125°C	01	1.79 typical		V
Logic 0 voltage		I <sub>OL</sub> = 50 μA	-55°C to +125°C	01		0.05	V
Digital outputs (D± x), ANSI-644							
Logic compliance					LVDS typical		
Differential output voltage	V <sub>OD</sub>		-55°C to +125°C	01	247	454	mV
					350 typical		
Output offset voltage	V <sub>OS</sub>		-55°C to +125°C	01	1.13	1.38	V
					1.21 typical		
Output coding (default)				01	Twos complement		
Digital outputs (D± x), low power, reduced signal option							
Logic compliance					LVDS typical		
Differential output voltage	V <sub>OD</sub>		-55°C to +125°C	01	150	250	mV
					200 typical		
Output offset voltage	V <sub>OS</sub>		-55°C to +125°C	01	1.13	1.38	V
					1.21 typical		
Output coding (default)				01	Twos complement		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 11

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Switching specifications <u>2/</u>							
Clock <u>10/ 11/</u>							
Input clock rate			-55°C to +125°C	01	10	520	MHz
Conversion rate			-55°C to +125°C	01	10	65	MSPS
Clock pulse width high	t <sub>HE</sub>		-55°C to +125°C	01	7.69 typical		ns
Clock pulse width low	t <sub>LE</sub>		-55°C to +125°C	01	7.69 typical		ns
Output parameters		Can be adjusted via the SPI.					
Propagation delay	t <sub>PD</sub>		-55°C to +125°C	01	1.5	3.1	ns
					2.3 typical		
Rise time	t <sub>R</sub>	(20% to 80%)	-55°C to +125°C	01	300 typical		ps
Fall time	t <sub>F</sub>	(20% to 80%)	-55°C to +125°C	01	300 typical		ps
FCO propagation delay	t <sub>FCO</sub>		-55°C to +125°C	01	1.5	3.1	ns
					2.3 typical		
DCO propagation <u>11/</u> delay	t <sub>CPD</sub>		-55°C to +125°C	01	t <sub>FCO</sub> + (t <sub>SAMPLE</sub> /28) typical		ns
DCO to data delay <u>11/</u>	t <sub>DATA</sub>		-55°C to +125°C	01	(t <sub>SAMPLE</sub> /28) - 300	(t <sub>SAMPLE</sub> /28) + 300	ps
					(t <sub>SAMPLE</sub> /28) typical		
DCO to FCO delay <u>11/</u>	t <sub>FRAME</sub>		-55°C to +125°C	01	(t <sub>SAMPLE</sub> /28) - 300	(t <sub>SAMPLE</sub> /28) + 300	ps
					(t <sub>SAMPLE</sub> /28) typical		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 12

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Switching specifications – continued. <u>2/</u>							
Output parameters – continued. Can be adjusted via the SPI.							
Data to data skew		t <sub>DATA-MAX</sub> – t <sub>DATA-MIN</sub>	-55°C to +125°C	01		±200	ps
					±50 typical		
Wake up time (standby)			+25°C	01	35 typical		μs
Wake up time <u>12/</u> (power down)			+25°C	01	375 typical		μs
Pipeline latency			-55°C to +125°C	01	16 typical		Clock cycles
Aperture							
Aperture delay	t <sub>A</sub>		+25°C	01	1 typical		ns
Aperture uncertainty (jitter)			+25°C	01	0.1 typical		ps rms
Out of range recovery time			+25°C	01	1 typical		Clock cycles

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 13

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Timing specifications							
SYNC timing requirements							
SYNC to rising edge of CLK+ setup time	t <sub>SSYNC</sub>		+25°C	01	0.24 typical		ns
SYNC to rising edge of CLK+ hold time	t <sub>HSYNC</sub>		+25°C	01	0.40 typical		ns
SPI timing requirements <u>13/</u> See figure 5							
Setup time between the data and the rising edge of SCLK	t <sub>DS</sub>		-55°C to +125°C	01	2		ns
Hold time between the data and the rising edge of SCLK	t <sub>DH</sub>		-55°C to +125°C	01	2		ns
Period of the SCLK	t <sub>CLK</sub>		-55°C to +125°C	01	40		ns
Setup time between CSB and SCLK	t <sub>S</sub>		-55°C to +125°C	01	2		ns
Hold time between CSB and SCLK	t <sub>H</sub>		-55°C to +125°C	01	2		ns
SCLK pulse width high	t <sub>HIGH</sub>		-55°C to +125°C	01	10		ns
SCLK pulse width low	t <sub>LOW</sub>		-55°C to +125°C	01	10		ns
Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	t <sub>EN_SDIO</sub>	Not shown in figure 5	-55°C to +125°C	01	10		ns
Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	t <sub>DIS_SDIO</sub>	Not shown in figure 5	-55°C to +125°C	01	10		ns

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 14

TABLE I. Electrical performance characteristics – Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, AVDD = 1.8 V, DRVDD = 1.8 V, 2 V Vp-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS.
- 3/ Unless otherwise specified, AVDD = 1.8 V, DRVDD = 1.8 V, 2 V Vp-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS. CLK divider = 8 used for typical characteristics at input frequency  $\geq$  19.7 MHz.
- 4/ Crosstalk is measured at 10 MHz with -1.0 dBFS analog input on one channel and no input on the adjacent channel.
- 5/ Overrange condition is 3 dB above the full scale input range.
- 6/ PSRR is measured by injecting a sinusoidal signal at 10 MHz to the power supply pin and measuring the output spur on the FFT. PSRR is calculated as the ratio of the amplitudes of the spur voltage over the pin voltage, expressed in decibels.
- 7/ When referencing a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
- 8/ This is specified for LVDS and LVPECL only.
- 9/ This is specified for 13 SDIO/DFS pins sharing the same connection.
- 10/ Measured on standard FR-4 material.
- 11/  $t_{SAMPLE}/28$  is based on the number of bits divided by 2 because the delays are based on half duty cycles.  $t_{SAMPLE} = 1/f_S$ .
- 12/ Wake up time is defined as the time required to return to normal operation from power down mode.
- 13/ When referencing a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 15

Case X

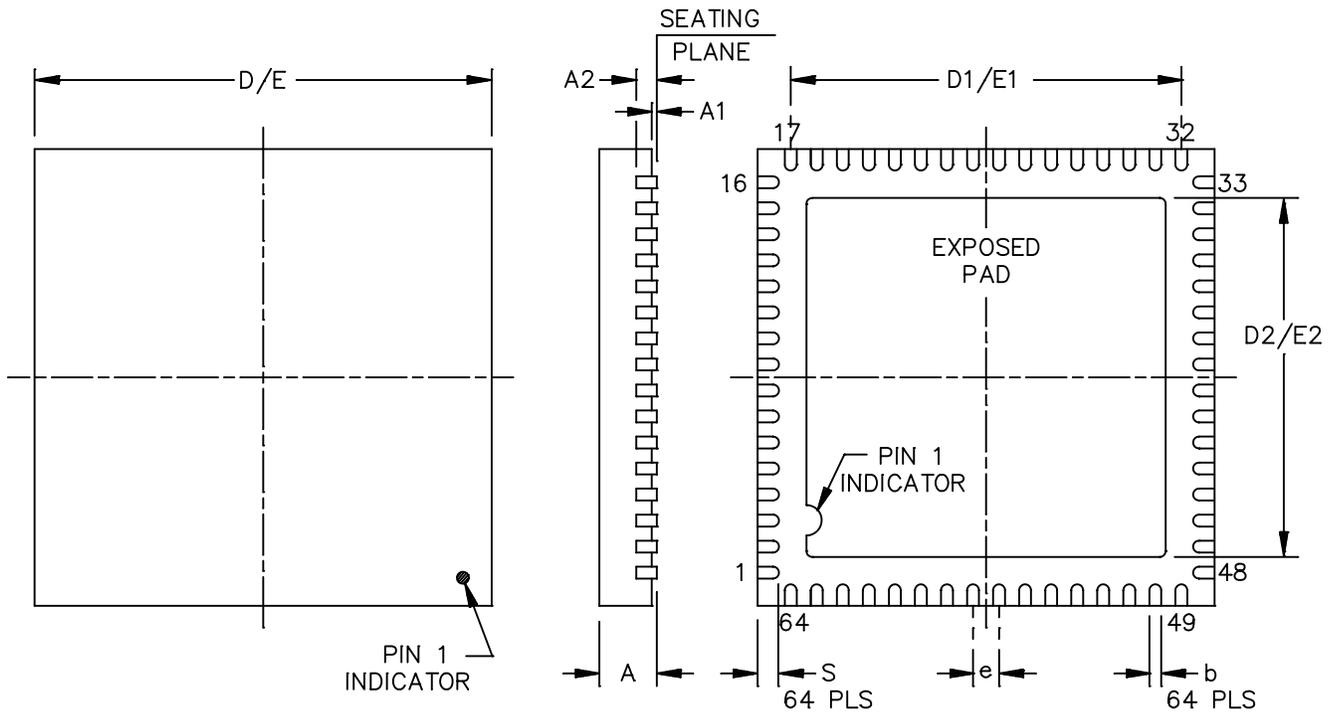


FIGURE 1. Case outline.

<p><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/14637</b></p>
		<p>REV</p>	<p>PAGE 16</p>

Case X – continued.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Medium	Maximum	Minimum	Medium	Maximum
A	0.027	0.029	0.031`	0.70	0.75	0.80
A1	0.003 COPLANARITY	0.0007 NOM	0.0019	0.08 COPLANARITY	0.02 NOM	0.05
A2	0.0079 REF			0.203 REF		
b	0.0070	0.009	0.011	0.18	0.25	0.30
D/E	0.350	0.354	0.358	8.90	9.00	9.10
D1/E1	0.295 REF			7.50 REF		
D2/E2	0.240	0.244	0.248	6.10	6.20	6.30
e	0.019 BSC			0.50 BSC		
S	0.013	0.015	0.017	0.35	0.40	0.45

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
3. Falls within reference to JEDEC MO-220-WMMD.

FIGURE 1. Case outline - Continued.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 17

Device type	01						
Case outline	X						
Terminal number	Terminal symbol						
1	AVDD	17	D- G	33	D- A	49	VIN+ C
2	VIN+ G	18	D+ G	34	D+ A	50	VIN- C
3	VIN- G	19	D- F	35	DRVDD	51	AVDD
4	AVDD	20	D+ F	36	NIC	52	VIN- D
5	VIN- H	21	D- E	37	AVDD	53	VIN+ D
6	VIN+ H	22	D+ E	38	SCLK/DTP	54	RBIAS
7	AVDD	23	DCO-	39	SDIO/DFS	55	SENSE
8	AVDD	24	DCO+	40	CSB	56	VREF
9	CLK-	25	FCO-	41	PDWN	57	VCM
10	CLK+	26	FCO+	42	AVDD	58	SYNC
11	AVDD	27	D- D	43	VIN+ A	59	AVDD
12	AVDD	28	D+ D	44	VIN- A	60	VIN+ E
13	NIC	29	D- C	45	AVDD	61	VIN- E
14	DRVDD	30	D+ C	46	VIN- B	62	AVDD
15	D- H	31	D- B	47	VIN+ B	63	VIN- F
16	D+ H	32	D+ B	48	AVDD	64	VIN+ F

NOTES:

1. NIC = not internally connected. These pins can be connected to ground.
2. The exposed pad must be connected to analog ground.

FIGURE 2. Terminal connections.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 18

Terminal symbol	Description
AGND, EP	Analog ground, exposed pad. The exposed thermal pad on the bottom of the package provides the analog ground for the device. This exposed pad must be connected to ground for proper operation.
AVDD	1.8 V analog supply.
NIC	Not internally connected. These pins can be connected to ground.
DRVDD	1.8 V digital output driver supply.
VIN+ G, VIN- G	ADC G analog input true, ADC G analog input complement.
VIN- H, VIN+ H	ADC H analog input complement, ADC H analog input true.
CLK-, CLK+	Input clock complement, input clock true.
D- H, D+ H	ADC H digital output complement, ADC H digital output true.
D- G, D+ G	ADC G digital output complement, ADC G digital output true.
D- F, D+ F	ADC F digital output complement, ADC F digital output true.
D- E, D+ E	ADC E digital output complement, ADC E digital output true.
DCO-, DCO+	Data clock digital output complement, data clock digital output true.
FCO-, FCO+	Frame clock digital output complement, frame clock digital output true.
D- D, D+ D	ADC D digital output complement, ADC D digital output true.
D- C, D+ C	ADC C digital output complement, ADC C digital output true.
D- B, D+ B	ADC B digital output complement, ADC B digital output true.
D- A, D+ A	ADC A digital output complement, ADC A digital output true.
SCLK/DTP	Serial clock (SCLK)/digital test pattern (DTP).
SDIO/DFS	Serial data input/output (SDIO)/data format select (DFS)

FIGURE 2. Terminal connections - continued.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 19

Terminal symbol	Description
CSB	Chip select bar.
PDWN	Power down.
VIN+ A, VIN- A	ADC A analog time input true, ADC A analog input complement.
VIN- B, VIN+ B	ADC B analog input complement, ADC B analog time input true.
VIN+ C, VIN- C	ADC C analog time input true, ADC C analog input complement.
VIN- D, VIN+ D	ADC D analog input complement, ADC D analog time input true.
RBIAS	Analog current bias setting. Connect to 10 k $\Omega$ (1 % tolerance) resistor to ground.
SENSE	Reference mode selection.
VREF	Voltage reference input/output.
VCM	Analog output voltage at midsupply. This pin sets the common mode of the analog inputs.
SYNC	Digital input. SYNC input to clock divider. 30 k $\Omega$ internal pull down resistor.
VIN+ E, VIN- E	ADC E analog time input true, ADC E analog input complement.
VIN- F, VIN+ F	ADC F analog input complement, ADC F analog time input true.

FIGURE 2. Terminal connections - continued.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		REV	PAGE 20

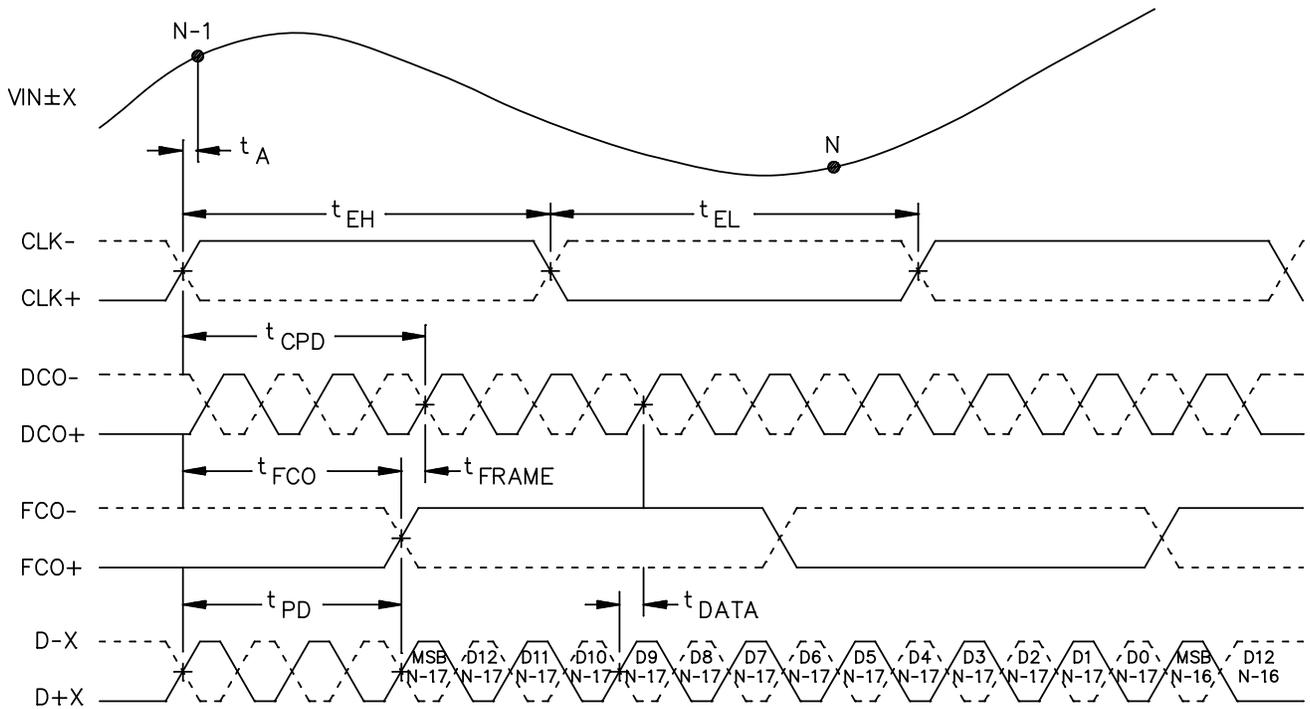


FIGURE 3. Word wise DRR, 1 x frame, 14 bit output mode (default).

<p align="center"><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p align="center"><b>SIZE A</b></p>	<p align="center"><b>CODE IDENT NO. 16236</b></p>	<p align="center"><b>DWG NO. V62/14637</b></p>
		<p align="center">REV</p>	<p align="center">PAGE 21</p>



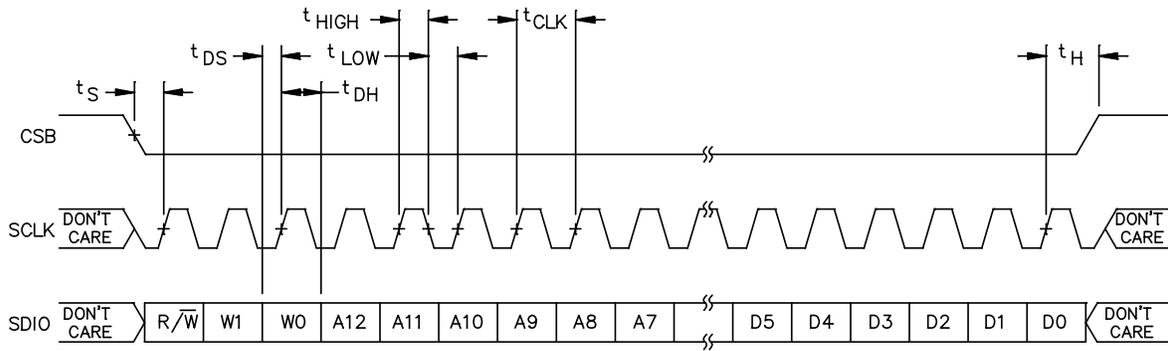


FIGURE 5. Serial port interface timing diagram.

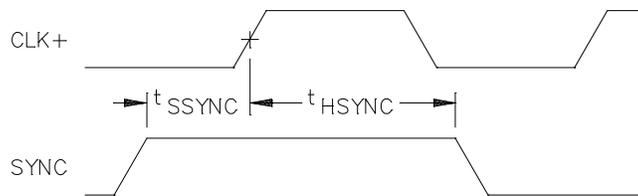


FIGURE 6. SYNC input timing requirements.

<p align="center"><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p align="center"><b>SIZE A</b></p>	<p align="center"><b>CODE IDENT NO. 16236</b></p>	<p align="center"><b>DWG NO. V62/14637</b></p>
		<p align="center">REV</p>	<p align="center">PAGE 23</p>

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/14637-01XA	24355	AD9257TCPZ-65-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices  
 Route 1 Industrial Park  
 P.O. Box 9106  
 Norwood, MA 02062  
 Point of contact: Raheen Business Park  
 Limerick, Ireland

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14637</b>
		<b>REV</b>	<b>PAGE 24</b>