REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17			

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 17-01-09	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, DUAL, 16-BIT NANODAC+ WITH 4 ppm/°C REFERENCE, SPI INTERFACE, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/14634**
	REV	**PAGE** 1 **OF** 17

AMSC N/A

5962-V002-17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Dual, 16-Bit nanoDAC+ with 4 ppm/°C Reference, SPI interface microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14634	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5689R –EP	Dual, 16-Bit nanoDAC+ with 4 ppm/°C Reference, SPI interface

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-220-WEED-6	Lead Frame Chip Scale Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to GND	-0.3 V to +7 V
V_{LOGIC} to GND	-0.3 V to +7 V
V_{OUT} to GND	-0.3 V to V_{DD} + 0.3 V
VREF to GND	-0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	-0.3 V to V_{LOGIC} + 0.3 V
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	135°C
Case outline X, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	70°C/W
Reflow Soldering Peak Temperature, Pb Free (J-STD-020)	260°C
Electrostatic Discharge Sensitivity (ESDS):	
HBM	4 kV
FICDM	1.25 kV

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC J-STD-020	–	Standard for moisture/reflow sensitivity classification for nonhermetric solid state surface mount devices. For electrostatic discharge sensitivity test Human Body Model (HBM) – component level.
JESD22-C101	–	Field-Induced Charged-Device Model (FIDCM) Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Serial Write Operation. The Serial Write Operation shall be as shown in figure 5.

3.5.6 Load Circuit for Digital Output (SDO) Timing Specification. The Load Circuit for Digital Output (SDO) Timing Specification shall be as shown in figure 6.

3.5.7 Daisy-Chain Timing Diagram. The Daisy-Chain Timing Diagram shall be as shown in figure 7.

3.5.8 Readback Timing Diagram. The Readback Timing Diagram shall be as shown in figure 8.

3.5.9 Headroom/Footroom vs Load Current. The Headroom/Footroom vs Load Current shall be as shown in figure 9.

TABLE I. Electrical performance characteristics. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
Static Performance 3/					
Resolution		16			Bits
Relative Accuracy	Gain = 2		±1	±4	LSB
	Gain = 1		±1	±5	LSB
Differential Nonlinearity (DNL)	Guaranteed monotonic by design			±1	LSB
Zero-Code Error	All zeros loaded to DAC register		0.4	1.5	mV
Offset Error			±0.1	±0.5	mV
Full-Scale Error	All ones loaded to DAC register		+0.01	+0.1	% of FSR
Gain Error	Gain = 2		±0.02	±0.1	% of FSR
	Gain = 1		±0.02	±0.15	% of FSR
Total Unadjusted Error	External reference; gain = 2		±0.01	±0.1	% of FSR
	Internal reference; gain = 1			±0.2	% of FSR
Offset Error Drift 4/			±1		µV/°C
Gain Temperature Coefficient (TC) 4/	Of FSR/°C		±1		ppm
DC Power Supply Rejection Ratio 4/	DAC code = midscale, V_{DD} = 5 V ± 10%		0.15		mV/V
DC Crosstalk	Due to single channel, full-scale output change		±2		µV
	Due to load current change		±3		µV/mA
	Due to powering down (per channel)		±2		µV
Output Characteristics 4/					
Output Voltage Range	Gain = 1	0		V_{REF}	V
	Gain = 2, see Figure 9	0		2 × V_{REF}	V
Capacitive Load Stability	R_L = ∞		2		nF
	R_L = 1 kΩ		10		nF
Resistive Load 5/		1			kΩ
Load Regulation	5 V ± 10%, DAC code = midscale; −30 mA ≤ I_{OUT} ≤ 30 mA		80		µV/mA
	3 V ± 10%, DAC code = midscale; −20 mA ≤ I_{OUT} ≤ 20 mA		80		µV/mA
Short-Circuit Current 6/			40		mA
Load Impedance at Rails 7/	See Figure 9		25		Ω
Power-Up Time	Coming out of power-down mode; V_{DD} = 5 V		2.5		µs
Reference Output					
Output Voltage 8/	At ambient	2.4975		2.5025	V
Reference TC 9/ 10/			4	13	ppm/°C
Output Impedance 4/			0.04		Ω
Output Voltage Noise 4/	0.1 Hz to 10 Hz		12		µV p-p
Output Voltage Noise Density	At ambient; f = 10 kHz, C_L = 10 nF		240		nV/√Hz
Load Regulation Sourcing 4/	At ambient		20		µV/mA
Load Regulation Sinking 4/	At ambient		40		µV/mA
Output Current Load Capability	V_{DD} ≥ 3 V		±5		mA
Line Regulation	At ambient		100		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
Reference Output (Continued)					
Thermal Hysteresis 4/	First cycle		125		ppm
	Additional cycles		25		ppm
Logic Inputs 4/					
Input Current	Per pin			±2	µA
Input Voltage Low (V_{IN}) High (V_{INH})		 0.7 × V_{LOGIC}		 0.3 × V_{LOGIC}	 V V
Pin Capacitance			2		pF
Logic Outputs (SDO) 4/					
Output Voltage Low (V_{OL}) High (V_{OH})	 I_{SINK} = 200 µA I_{SOURCE} = 200 µA	 V_{LOGIC} − 0.4		 0.4	 V V
Floating State Output Capacitance			4		pF
Power Requirements					
V_{LOGIC}		1.62		5.5	V
I_{LOGIC}				3	µA
V_{DD}	Gain = 1	2.7		5.5	V
V_{DD}	Gain = 2	V_{REF} + 1.5		5.5	V
I_{DD}	V_{IH} = V_{DD}, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V				
Normal Mode 11/	Internal reference off		0.59	0.7	mA
	Internal reference on at full scale		1.1	1.3	mA
All Power-Down Modes 12/	−40°C to +85°C		1	4	µA
	−55°C to +125°C			6	µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
AC Characteristics 13/ 14/ 15/					
Output Voltage Settling Time	¼ to ¾ scale settling to ±2 LSB		5	8	µs
Slew Rate			0.8		V/µs
Digital-to-Analog Glitch Impulse	1 LSB change around major carry		0.5		nV-sec
Digital Feedthrough			0.13		nV-sec
Digital Crosstalk			0.1		nV-sec
Analog Crosstalk			0.2		nV-sec
DAC-to-DAC Crosstalk			0.3		nV-sec
Total Harmonic Distortion (THD) 16/	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		-80		dB
Output Noise Spectral Density (NSD)	DAC code = midscale, 10 kHz; gain = 2		300		nV/√Hz
Output Noise	0.1 Hz to 10 Hz		6		µV p-p
Signal-to-Noise Ratio (SNR)	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		90		dB
Spurious Free Dynamic Range (SFDR)	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		83		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		80		dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits				Unit
			1.62 V ≤ V_{LOGIC} ≤ 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		
			Min	Max	Min	Max	
Timing Characteristics 17/ 18/ (See Figure 5)							
SCLK Cycle Time	t_1		20		20		ns
SCLK High Time	t_2		10		10		ns
SCLK Low Time	t_3		10		10		ns
$\overline{SYNC}$ to SCLK Falling Edge Setup Time	t_4		15		10		ns
Data Setup Time	t_5		5		5		ns
Data Hold Time	t_6		5		5		ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7		10		10		ns
Minimum $\overline{SYNC}$ High Time	t_8		20		20		ns
$\overline{SYNC}$ Rising Edge to $\overline{SYNC}$ Rising Edge (DAC Register Update/s)	t_9		870		830		ns
$\overline{SYNC}$ falling Edge to SCLK Fall Ignore	t_{10}		16		10		ns
$\overline{LDAC}$ Pulse width low	t_{11}		15		15		ns
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Rising Edge	t_{12}		20		20		ns
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Falling Edge	t_{13}		30		30		ns
$\overline{LDAC}$ Falling Edge to $\overline{SYNC}$ Rising Edge	t_{14}		840		800		ns
Minimum Pulse Width Low	t_{15}		30		30		ns
Pulse Activation time	t_{16}		30		30		ns
Power-Up Time 19/			4.5		4.5		µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 20/	Limits				Unit
			1.8 V ≤ V_{LOGIC} ≤ 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		
			Min	Max	Min	Max	
Daisy-Chain and Readback Timing Characteristics 21/ (See Figure 6-8)							
SCLK Cycle Time	t_1		66		40		ns
SCLK High Time	t_2		33		20		ns
SCLK Low Time	t_3		33		20		ns
$\overline{SYNC}$ to SCLK Falling Edge	t_4		33		20		ns
Data Setup Time	t_5		5		5		ns
Data Hold Time	t_6		5		5		ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7		15		10		ns
Minimum $\overline{SYNC}$ High Time	t_8		60		30		ns
SDO Data Valid from SCLK Rising Edge	t_9			40		30	ns
$\overline{SYNC}$ Rising Edge to SCLK Rising Edge	t_{10}		15		10		ns
$\overline{SYNC}$ Rising Edge to SDO Disable	t_{11}		60		60		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 2.7 V to 5.5 V; 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. R_L = 2 kΩ; C_L = 200 pF.

3/ DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when V_{REF} = V_{DD} with gain = 1 or when $V_{REF}/2$ = V_{DD} with gain = 2. Linearity is calculated using a reduced code range of 256 to 65,280.

4/ Guaranteed by design, not subject to production test.

5/ Channel A can have an output current of up to 15 mA. Similarly, Channel B can have an output current of up to 15 mA, up to a junction temperature of 135°C.

6/ V_{DD} = 5 V. The device includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature may be exceeded during current limit, but operation above the specified maximum operation junction temperature can impair device reliability.

7/ When drawing a load current at either rail, the output voltage headroom, with respect to that rail, is limited by the 25 Ω typical channel resistance of the output device. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 9).

8/ Initial accuracy presolder reflow is ±750 µV; output voltage includes the effects of preconditioning drift. See manufacturer data sheet AD5689R/AD5687R for more information.

9/ Reference is trimmed and tested at two temperatures and is characterized from −55°C to +125°C.

10/ Reference temperature coefficient is calculated as per the box method. See manufacturer data sheet AD5689R/AD5687R for more information.

11/ Interface inactive. Both DACs active. DAC outputs unloaded.

12/ Both DACs powered down.

13/ V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Guaranteed by design and characterization; not production tested.

14/ Temperature range is −55°C to +125°C, typical at 25°C.

15/ See manufacturer data sheet AD5689R/AD5687R

16/ Digitally generated sine wave at 1 kHz.

17/ All input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 5. V_{DD} = 2.7 V to 5.5 V, 1.8 V ≤ V_{LOGIC} ≤ 5.5 V; V_{REF} = 2.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

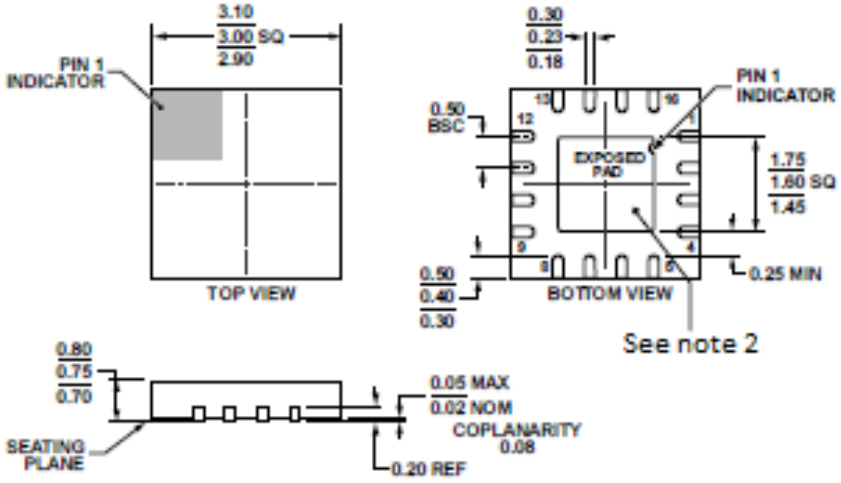
18/ Maximum SCLK frequency is 50 MHz at V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ V_{DD}. Guaranteed by design and characterization; not production tested.

19/ Time to exit power-down to normal mode of AD5689R-EP operation, 32nd clock edge to 90% of DAC midscale value, with output unloaded.

20/ All input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 7 and Figure 8. V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; V_{REF} = 2.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. V_{DD} = 2.7 V to 5.5 V.

21/ Guaranteed by design and characterization; not production tested.

Case X



NOTES:
1. All linear dimensions are in millimeters.
2. For proper connection of the exposed PAD, refer to the pin configuration and function descriptions section on Figure 3.
3. Falls within JEDEC MO-220-WEED-6.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$V_{OUT}A$	16	NC
2	GND	15	V_{REF}
3	V_{DD}	14	RSTSEL
4	NC	13	$\overline{RESET}$
5	$V_{OUT}B$	12	SDIN
6	SDO	11	$\overline{SYNC}$
7	$\overline{LDAC}$	10	SCLK
8	GAIN	9	V_{LOGIC}

NOTES:
1. The exposed PAD must be tied to GND.
2. NC = No Connect. Do not Connect to this PIN.

FIGURE 2. Terminal connections.

Terminal Number	Terminal Symbol	**Description**
1	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
2	GND	Ground Reference Point for All Circuitry on the AD5689R-EP.
3	V_{DD}	Power Supply Input. The AD5689R-EP can be operated from 2.7 V to 5.5 V. Decouple the supply with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	NC	No Connect. Do not connect to this pin.
5	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
6	SDO	Serial Data Output. SDO can be used to daisy-chain a number of AD5689R-EP devices together, or it can be used for readback. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
7	$\overline{\text{LDAC}}$	$\overline{\text{LDAC}}$ can be operated in two modes: asynchronously and synchronously. Pulsing this pin low allows either or both DAC registers to be updated if the input registers have new data; both DAC outputs can be updated simultaneously. This pin can also be tied permanently low.
8	GAIN	Gain Select. When this pin is tied to GND, both DACs output a span from 0 V to V_{REF}. If this pin is tied to V_{LOGIC}, both DACs output a span of 0 V to 2 × V_{REF}.
9	V_{LOGIC}	Digital Power Supply. Voltage ranges from 1.8 V to 5.5 V.
10	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
11	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data is transferred in on the falling edges of the next 24 clocks.
12	SDIN	Serial Data Input. This device has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	$\overline{\text{RESET}}$	Asynchronous Reset Input. The $\overline{\text{RESET}}$ input is falling edge sensitive. When $\overline{\text{RESET}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{RESET}}$ activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin.
14	RSTSEL	Power-On Reset Select. Tying this pin to GND powers up both DACs to zero scale. Tying this pin to V_{LOGIC} powers up both DACs to midscale.
15	V_{REF}	Reference Voltage. The AD5689R-EP has a common reference pin. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference output.
16	NC	No Connect. Do not connect to this pin.
17	EPAD	Exposed Pad. The exposed pad must be tied to GND.

FIGURE 3. Terminal function.

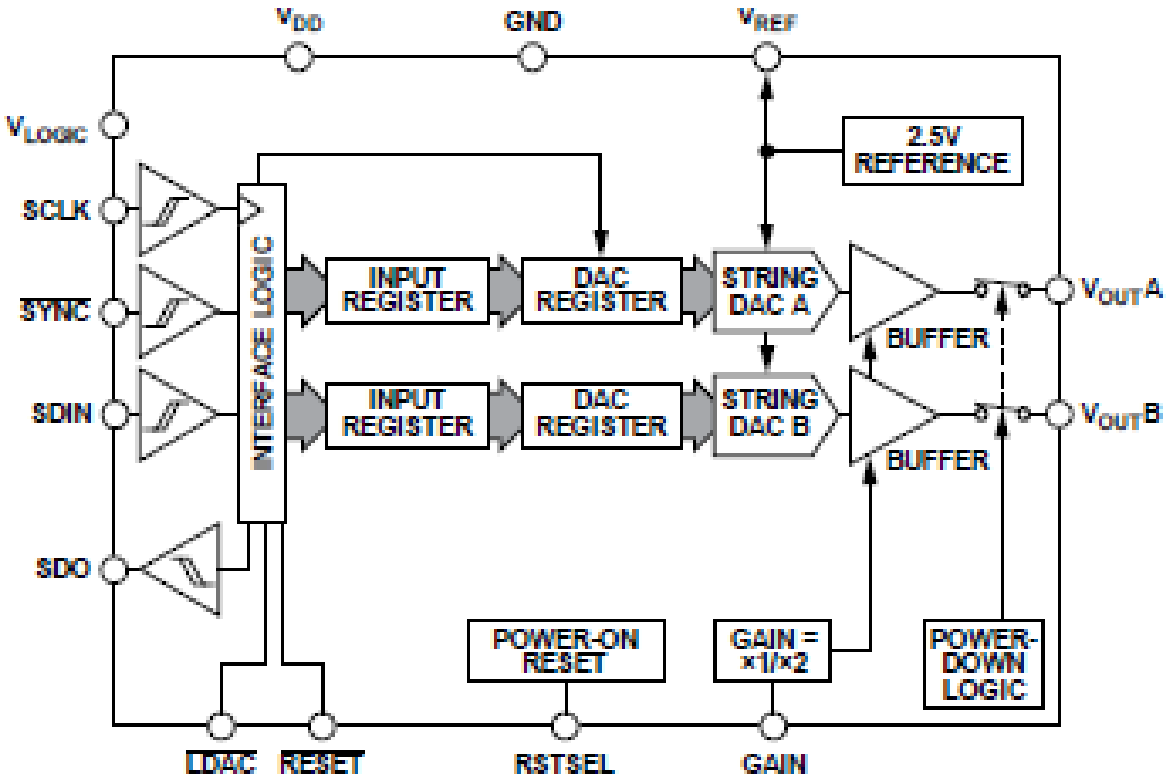


FIGURE 4. Functional block diagram.

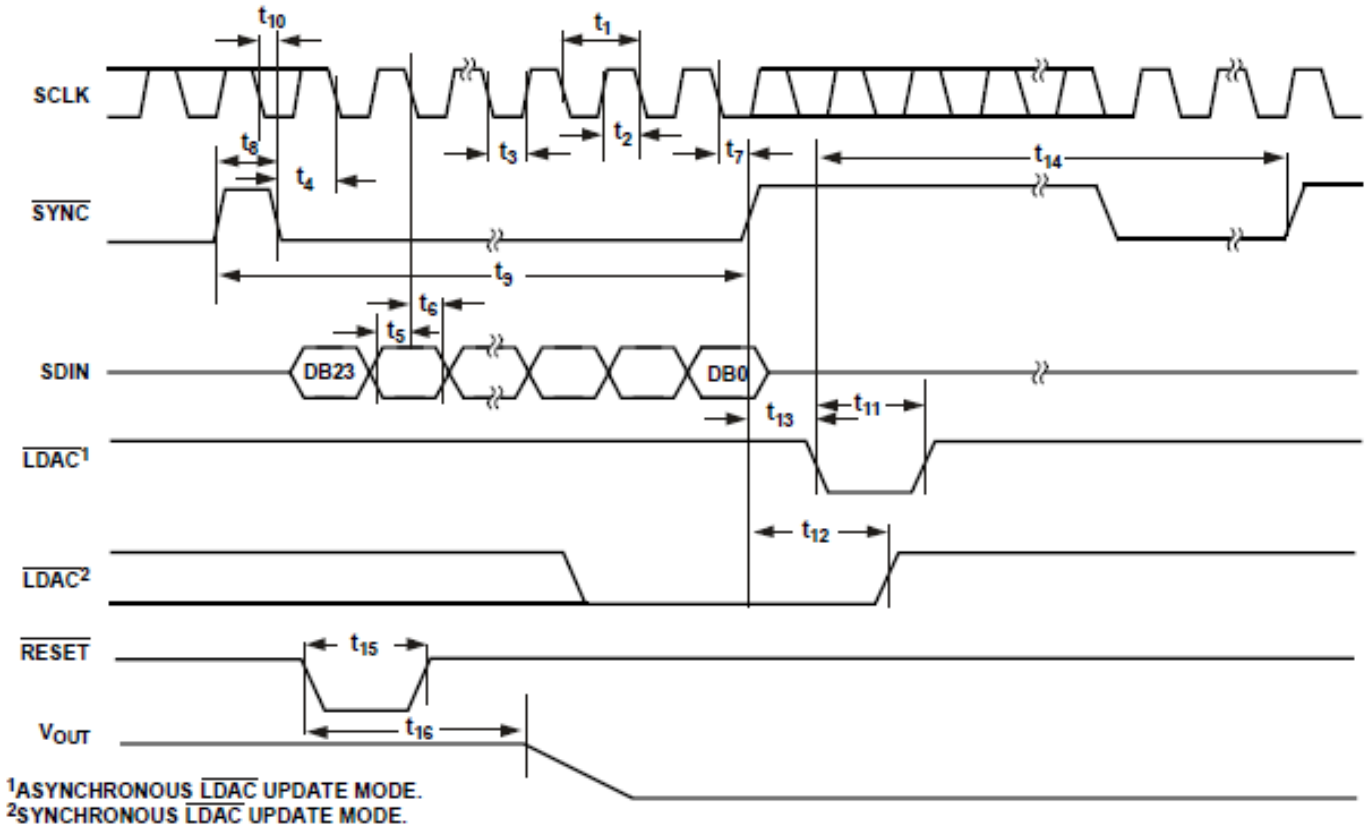


FIGURE 5. Serial Write Operation.

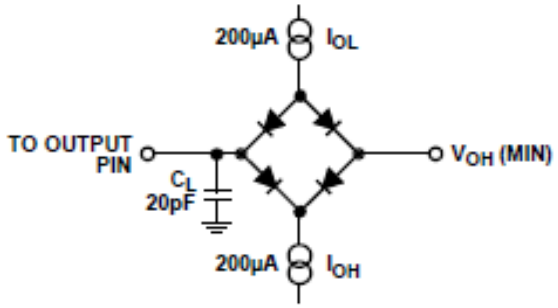


FIGURE 6. Load Circuit for Digital Output (SDO) Timing Specifications.

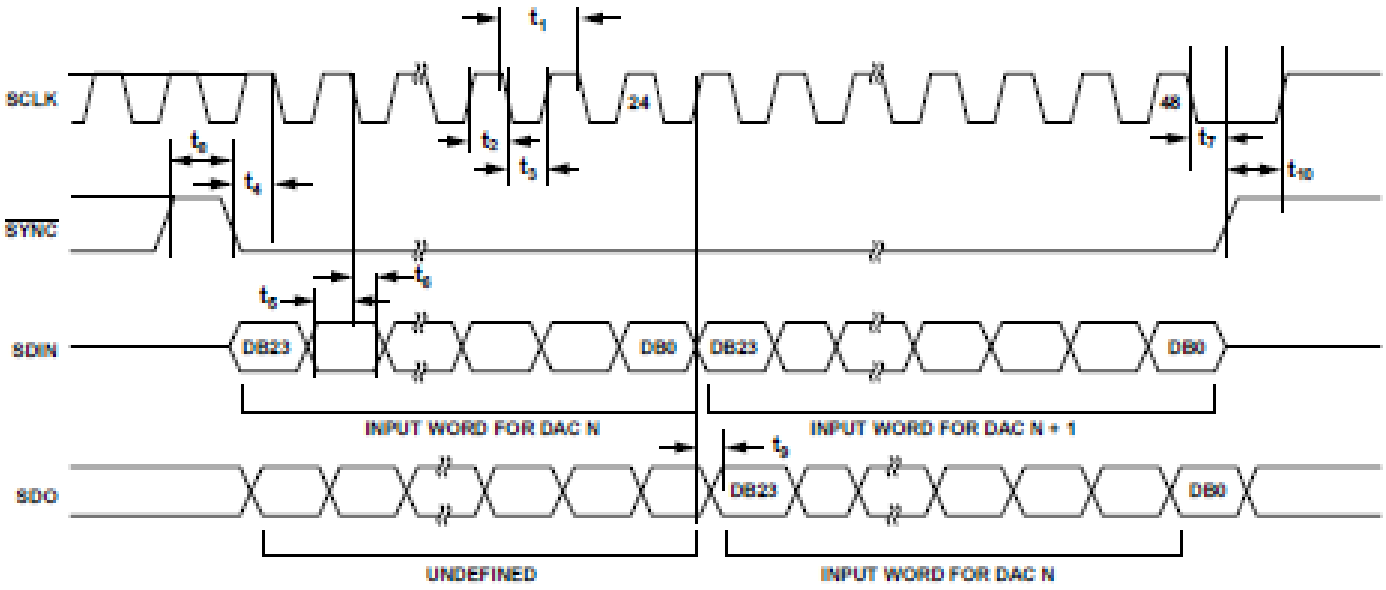


FIGURE 7. Daisy-Chain Timing Diagram.

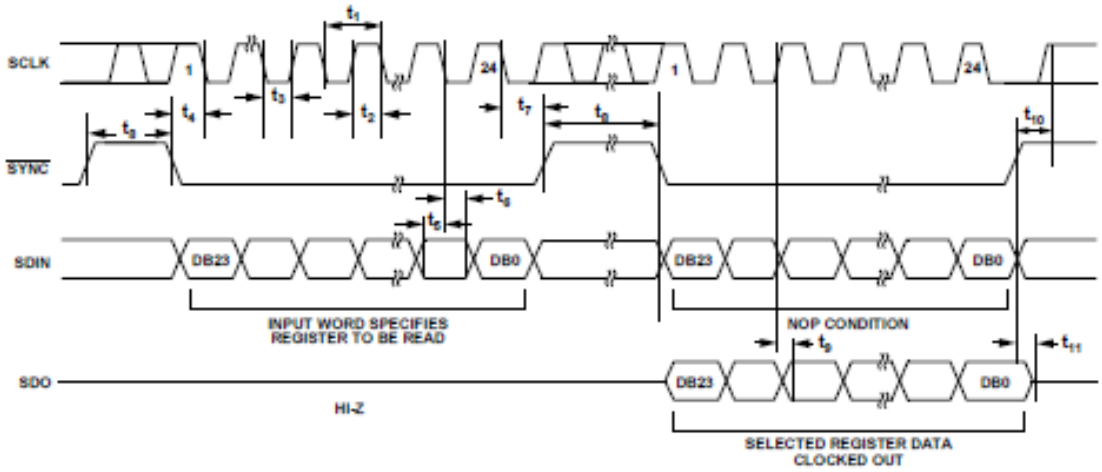


FIGURE 8. Readback Timing Diagram.

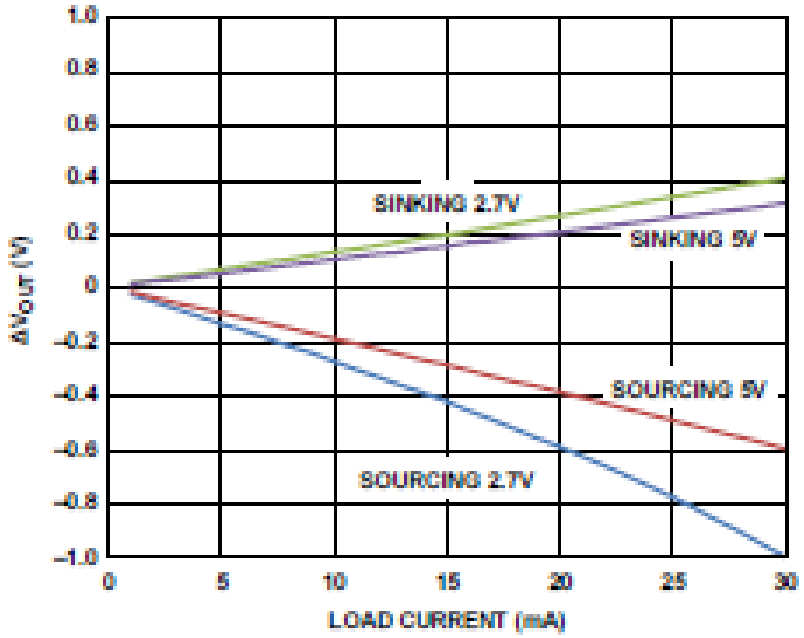


FIGURE 9. Headroom/Footroom vs Load Current.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Ordering Quantity	Vendor part number
V62/14634-01XE	24355	Tray units = Not Available	AD5689R-EP
		Reel units = 1500	AD5689RTCPZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106