

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update dimension b maximum limit from 0.33 mm to 0.30 mm. Updating document paragraphs to current requirements. - ro	20-05-06	J. ESCHMEYER



Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
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PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime
Original date of drawing YY-MM-DD 14-12-16	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, DIGITAL-LINEAR, DUAL, 12 BIT, DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	DWG NO. V62/14633
	SIZE A	CODE IDENT. NO. 16236
	REV A	PAGE 1 OF 14

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual, 12 bit digital to analog converter (DAC) microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/14633</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	AD5623R-EP	Dual, 12 bit digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	10	MO-187-BA	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

VDD to GND	-0.3 V to +7 V
VOUTx to GND	-0.3 V to VDD + 0.3 V
VREFIN / VREFOUT to GND	-0.3 V to VDD + 0.3 V
Digital input voltage to GND	-0.3 V to VDD + 0.3 V
Storage temperature range (TSTG)	-65°C to +150°C
Junction temperature range (TJ)	+150°C
Power dissipation (PD) equation	(TJ max – TA) / θ_{JA}
Thermal impedance, junction to case (θ_{JC})	43.7°C/W
Thermal impedance, junction to ambient (θ_{JA})	142°C/W
Reflow soldering peak temperature lead (Pb) free	260 (+0/-5) °C

1.4 Recommended operating conditions. 2/

Operating free-air temperature range (TA)	-55°C to +105°C
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- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Serial write operation waveforms. The serial write operation waveforms shall be as shown in figure 3.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Static performance <u>3/ 4/</u>							
Resolution			-55°C to +105°C	01	12		Bits
Relative accuracy	INL		-55°C to +105°C	01		±1.5	LSB
			+25°C		±1 typical		
Differential nonlinearity	DNL	Guaranteed monotonic by design	-55°C to +105°C	01		±1	LSB
Zero scale error		All 0s loaded to DAC register	-55°C to +105°C	01		+12	mV
			+25°C		+2 typical		
Offset error			-55°C to +105°C	01		±12	mV
			+25°C		±1 typical		
Full scale error		All 1s loaded to DAC register	-55°C to +105°C	01		±1	% of FSR
			+25°C		-0.1 typical		
Gain error			-55°C to +105°C	01		±1.5	% of FSR
Zero scale error drift			+25°C	01	±2 typical		µV/°C
Gain temperature coefficient		Of FSR/°C	+25°C	01	±2.5 typical		ppm
DC power supply rejection ratio		DAC code = midscale, VDD = 5 V ±10%	+25°C	01	-100 typical		dB
DC crosstalk							
External reference		Due to full scale output change, RL = 2 kΩ to GND or VDD	+25°C	01	10 typical		µV
		Due to load current change	+25°C		10 typical		µV/mA
		Due to powering down (per channel)	+25°C		5 typical		µV
Internal reference		Due to full scale output change, RL = 2 kΩ to GND or VDD	+25°C	01	25 typical		µV
		Due to load current change	+25°C		20 typical		µV/mA
		Due to powering down (per channel)	+25°C		10 typical		µV

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Output characteristics <u>5/</u>							
Output voltage range			-55°C to +105°C	01	0	V _{DD}	V
Capacitive load stability		R _L = ∞	+25°C	01	2 typical		nF
		R _L = 2 kΩ			10 typical		
DC output impedance			+25°C	01	0.5 typical		Ω
Short circuit current		V _{DD} = 5 V	+25°C	01	30 typical		mA
Power up time		Coming out of power down mode, V _{DD} = 5 V	+25°C	01	4 typical		μs
Reference inputs							
Reference current		V _{REFIN} / V _{REFOUT} = V _{DD} = 5.5 V	-55°C to +105°C	01		200	μA
			+25°C		170 typical		
Reference input range			-55°C to +105°C	01	0.75	V _{DD}	V
Reference input impedance			+25°C	01	26 typical		kΩ
Reference output							
Output voltage		At ambient	-55°C to +105°C	01	2.495	2.505	V
Reference <u>5/</u> temperature coefficient			+25°C	01	±10 typical		ppm/ °C
Output impedance			+25°C	01	7.5 typical		kΩ
Logic inputs <u>5/</u>							
Input current		All digital inputs	-55°C to +105°C	01		±2	μA
Input low voltage	V _{INL}	V _{DD} = 5 V	-55°C to +105°C	01		0.8	V
Input high voltage	V _{INH}	V _{DD} = 5 V	-55°C to +105°C	01	2		V
Pin capacitance		DIN, SCLK, and $\overline{\text{SYNC}}$	+25°C	01	3 typical		pF
		$\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$			19 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Power requirements							
Power supply input	V _{DD}		-55°C to +105°C	01	4.5	5.5	V
Power supply current (normal mode) <u>6/</u>	I _{DD}	V _{INH} = V _{DD} and V _{INL} = GND					
Internal reference off		V _{DD} = 4.5 V to 5.5 V	-55°C to +105°C	01		0.45	mA
			+25°C		0.25 typical		
Internal reference on		V _{DD} = 4.5 V to 5.5 V	-55°C to +105°C	01		1	mA
			+25°C		0.8 typical		
Power supply <u>7/</u> current (all power down modes)	I _{DD}	V _{DD} = 4.5 V to 5.5 V, V _{INH} = V _{DD} and V _{INL} = GND	-55°C to +105°C	01		1	μA
			+25°C		0.48 typical		
AC characteristics <u>4/ 5/</u>							
Slew rate	SR		+25°C	01	1.8 typical		V/μs
Feedthrough							
Digital feedthrough			+25°C	01	0.1 typical		nV-sec
Reference feedthrough		V _{REFIN} / V _{REFOUT} = 2 V ± 0.1 VP-P, frequency 10 Hz to 20 MHz	+25°C	01	-90 typical		dB
Crosstalk							
Digital crosstalk			+25°C	01	0.1 typical		nV-sec
Analog crosstalk		External reference	+25°C	01	1 typical		nV-sec
		Internal reference			4 typical		
DAC to DAC crosstalk		External reference	+25°C	01	1 typical		nV-sec
		Internal reference			4 typical		
Multiplying bandwidth		V _{REFIN} / V _{REFOUT} = 2 V ± 0.1 VP-P,	+25°C	01	340 typical		kHz

See footnotes at end of table.

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TABLE 1. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, TA	Device type	Limits		Unit
					Min	Max	

AC characteristics – continued. 4/ 5/

Total harmonic distortion		VREFIN / VREFOUT = 2 V ± 0.1 VP-P, frequency = 10 kHz	+25°C	01	-80 typical		dB
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Output characteristics

Digital to analog glitch impulse		1 LSB change around major carry	+25°C	01	10 typical		nV-sec
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Output voltage settling time		1/4 to 3/4 scale settling to ±0.5 LSB	-55°C to +105°C	01	4.5		µs
					3 typical		

Output noise spectral density		DAC code = midscale, 1 kHz	+25°C	01	120 typical		nV / √Hz
					100 typical		

Output noise		0.1 Hz to 10 Hz	+25°C	01	15 typical		µVp-p
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Timing characteristics. 5/ 8/ See figure 3.

SCLK cycle time 9/	t1		-55°C to +105°C	01	20		ns
SCLK high time	t2		-55°C to +105°C	01	9		ns
SCLK low time	t3		-55°C to +105°C	01	9		ns
S $\overline{\text{YNC}}$ to SCLK falling edge setup time	t4		-55°C to +105°C	01	13		ns
Data setup time	t5		-55°C to +105°C	01	5		ns
Data hold time	t6		-55°C to +105°C	01	5		ns
SCLK falling edge to S $\overline{\text{YNC}}$ rising edge	t7		-55°C to +105°C	01	0		ns
Minimum S $\overline{\text{YNC}}$ high time	t8		-55°C to +105°C	01	15		ns
S $\overline{\text{YNC}}$ rising edge to SCLK falling edge to S $\overline{\text{YNC}}$ fall ignore	t9		-55°C to +105°C	01	13		ns
SCLK falling edge to S $\overline{\text{YNC}}$ fall ignore	t10		-55°C to +105°C	01	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Timing characteristics – continued. <u>5/ 8/</u> See figure 3.							
$\overline{\text{LDAC}}$ pulse width low	t11		-55°C to +105°C	01	10		ns
SCLK falling edge to $\overline{\text{LDAC}}$ rising edge	t12		-55°C to +105°C	01	15		ns
$\overline{\text{CLR}}$ pulse width low	t13		-55°C to +105°C	01	5		ns
SCLK falling edge to $\overline{\text{LDAC}}$ falling edge	t14		-55°C to +105°C	01	0		ns
$\overline{\text{CLR}}$ pulse activation time	t15		-55°C to +105°C	01		300	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = 4.5 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REFIN} / V_{REFOUT} = V_{DD}, all specifications at -55°C to +105°C and typical at +25°C.

3/ Linearity calculated using a reduced code range: code 32 to code 4064. Output unloaded.

4/ See terminology section in the manufacturer's data sheet.

5/ Guaranteed by design and characterization, but not production tested.

6/ Interface inactive. All DACs active. DAC outputs unloaded.

7/ Both DACs powered down.

8/ All input signals are specified, with t_R = t_F = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{INL} + V_{INH}) / 2. Unless otherwise specified, V_{DD} = 4.5 V to 5.5 V and all specifications at -55°C to +105°C.

9/ Maximum SCLK frequency is 50 MHz at V_{DD} = 2.7 V to 5.5 V.

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Case X

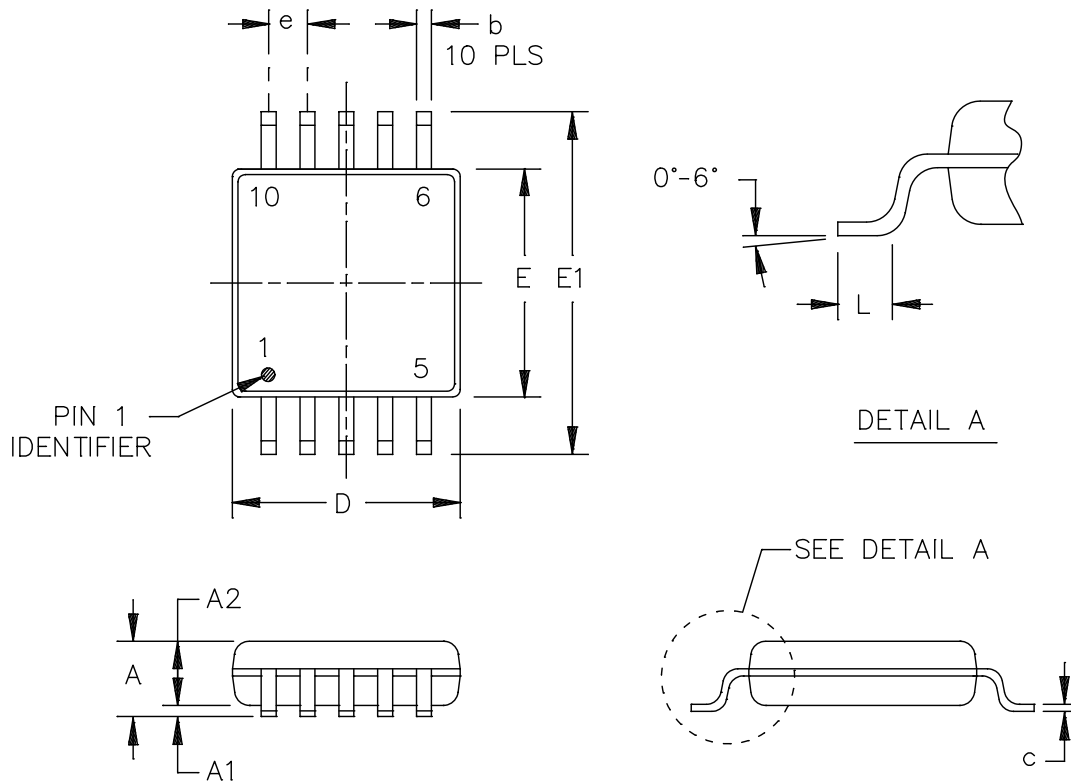


FIGURE 1. Case outline.

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Case X - continued

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Medium	Maximum	Minimum	Medium	Maximum
A	---	---	0.043	---	---	1.10
A1	0.0019	---	0.0059	0.05	---	0.15
A2	0.029	0.033	0.037	0.75	0.85	0.95
b	0.0059	---	0.012	0.15	---	0.30
c	0.0051	---	0.009	0.13	---	0.23
D	0.114	0.118	0.122	2.90	3.00	3.10
E	0.114	0.118	0.122	2.90	3.00	3.10
E1	0.183	0.192	0.202	4.65	4.90	5.15
e	0.019 BSC			0.050 BSC		
L	0.015	0.021	0.027	0.40	0.55	0.70

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-187-BA.

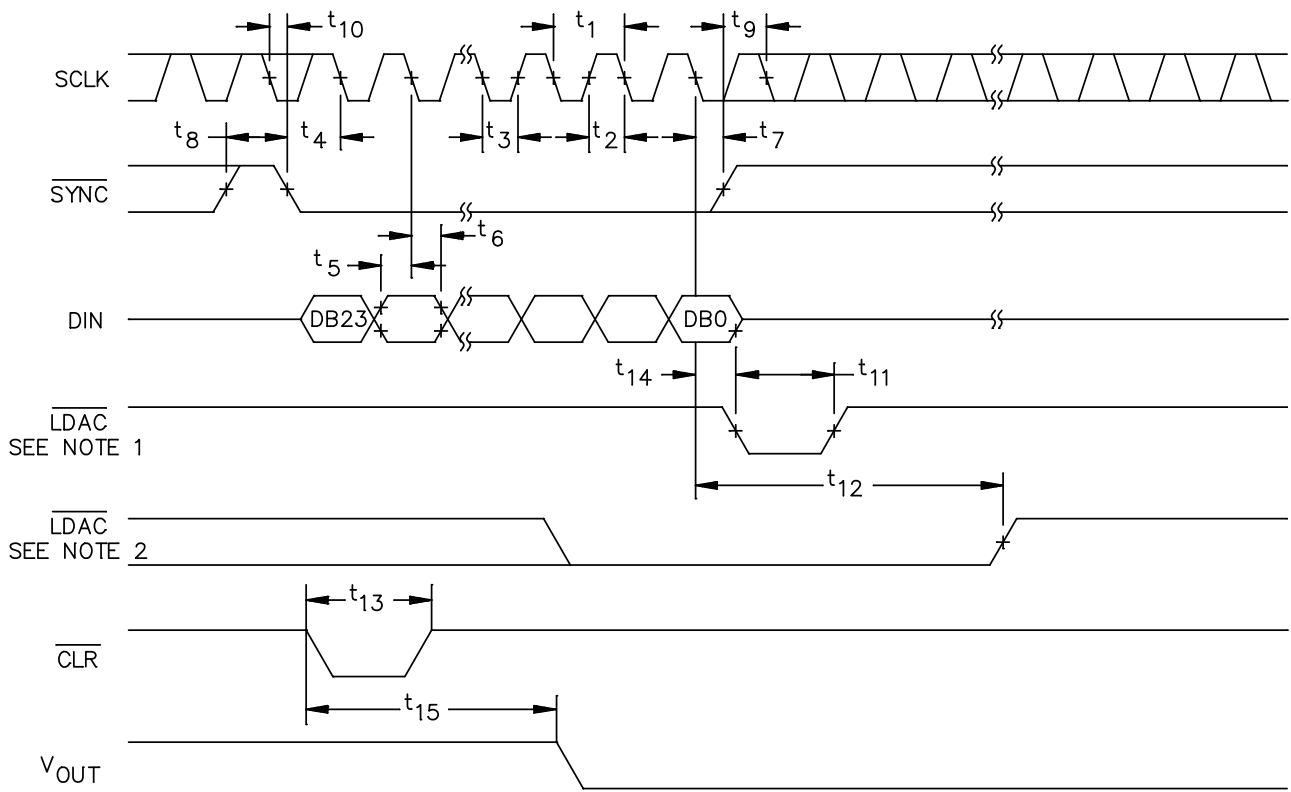
FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	VOUTA	Analog output voltage from DAC A. The output amplifier has rail to rail operation.
2	VOUTB	Analog output voltage from DAC B. The output amplifier has rail to rail operation.
3	GND	Ground. Reference point for all circuitry on the device.
4	$\overline{\text{LDAC}}$	Load DAC. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively, this pin can be tied permanently low.
5	$\overline{\text{CLR}}$	Asynchronous clear input. The $\overline{\text{CLR}}$ input is falling edge sensitive. While $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The device exits clear code mode on the 24th falling edge of the next write to the device. If $\overline{\text{CLR}}$ is activated during a write sequence, the write is aborted.
6	$\overline{\text{SYNC}}$	Level triggered control input (active low). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register, and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle unless $\overline{\text{SYNC}}$ is taken high before this edge, in which case the rising edge of $\overline{\text{SYNC}}$ act as an interrupt and the write sequence is ignored by the DAC.
7	SCLK	Serial clock input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
8	DIN	Serial data input. This device has a 24 bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
9	VDD	Power supply input. This device can be operated from 4.5 V to 5.5 V. Decouple the supply with a 10 μF capacitor in parallel with a 0.1 μF capacitor to GND.
10	VREFIN / VREFOUT	Common reference input/reference output. When the internal reference is selected, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is a reference input.

FIGURE 2. Terminal connections.

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NOTES:

1. Asynchronous $\overline{\text{LDAC}}$ update mode.
2. Synchronous $\overline{\text{LDAC}}$ update mode.

FIGURE 3. Serial write operation waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/14633-01XE	24355	DN9	AD5623RSRMZ-EP-5R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 Route 1 Industrial Park
 P.O. Box 9106
 Norwood, MA 02062
 Point of contact: 20 Alpha Road
 Chelmsford, MA 01824-4123

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