REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 14-12-16	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 18 BIT, 250 kSPS DIFFERENTIAL ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/14632**
	REV	**PAGE** 1 **OF** 17

AMSC N/A

5962-V012-15

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 18 bit, 250 kilo samples per second (kSPS) differential analog to digital converter microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14632	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7691-EP	18 bit, 250 kSPS differential analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	10	MO-187-BA	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Analog inputs (+INPUT, -INPUT)	GND – 0.3 V to V_{DD} + 0.3 V or ±130 mA
Reference (REF) input voltage (V_{REF})	GND – 0.3 V to V_{DD} + 0.3 V
Supply voltages:	
Power supply (V_{DD}), input/output interface digital power (V_{IO}) to ground (GND)	-0.3 V to +7 V
V_{DD} to V_{IO}	±7 V
Digital inputs to GND	-0.3 V to V_{IO} + 0.3 V
Digital outputs to GND	-0.3 V to V_{IO} + 0.3 V
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature range (T_J)	+150°C
Lead temperature range	See JEDEC J-STD-20
Thermal resistance, junction to ambient (θ_{JC})	44°C/W
Thermal resistance, junction to ambient (θ_{JA})	200°C/W

1.4 Recommended operating conditions. 2/

Operating free-air temperature range (T_A)	-55°C to +105°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC J STD-020 - Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices
JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Load circuit for digital interface timing. The load circuit for digital interface timing shall be as shown in figure 3.

3.5.4 Voltage levels for timing waveforms. The voltage levels for timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Resolution			-55°C to +105°C	01	18		Bits
Analog input							
Voltage range	V_{IN}	+INPUT – (-INPUT)	-55°C to +105°C	01	$-V_{REF}$	$+V_{REF}$	V
Absolute input voltage range		+INPUT, -INPUT	-55°C to +105°C	01	-0.1	V_{REF} + 0.1	V
Common mode input range		+INPUT, -INPUT	-55°C to +105°C	01	$V_{REF}/2$ – 0.1	$V_{REF}/2$ + 0.1	V
					$V_{REF}/2$ typical		
Analog input common mode rejection ratio	CMRR	f_{IN} = 250 kHz	-55°C to +105°C	01	65 typical		dB
Leakage current		Acquisition phase	+25°C	01	1 typical		nA
Throughput							
Conversion rate		V_{DD} = 4.5 V to 5.25 V	-55°C to +105°C	01	0	250	kSPS
		V_{DD} = 2.3 V to 4.5 V			0	180	
Transient response		Full scale step	-55°C to +105°C	01		1.8	µs
Accuracy							
No missing codes			-55°C to +105°C	01	18		Bits
Integral linearity error			-55°C to +105°C	01	-2.7	+2	LSB 3/
					±0.75 typical		
			-40°C to +85°C		-1.5	+1.5	
					±0.75 typical		
Differential linearity error			-55°C to +105°C	01	-1	+1.25	LSB 3/
					±0.5 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Accuracy – continued.							
Transition noise		REF = V_{DD} = 5 V	-55°C to +105°C	01	0.75 typical		LSB 3/
Gain error 4/		V_{DD} = 4.5 V to 5.25 V	-55°C to +105°C	01	-40	+40	LSB 3/
					±2 typical		
		V_{DD} = 2.3 V to 4.5 V			-80	+80	
					±2 typical		
Gain error temperature drift			-55°C to +105°C	01	±0.3 typical		ppm/°C
Zero error 4/		V_{DD} = 4.5 V to 5.25 V	-55°C to +105°C	01	-0.8	+0.8	mV
					±0.1 typical		
		V_{DD} = 2.3 V to 4.5 V			-3.5	+3.5	
					±0.7 typical		
Zero error temperature drift			-55°C to +105°C	01	±0.3 typical		ppm/°C
Power supply sensitivity		V_{DD} = 5 V ±5%	-55°C to +105°C	01	±0.25 typical		LSB 3/
AC Accuracy 5/							
Dynamic range		V_{REF} = 5 V	-55°C to +105°C	01	101		dB
					102 typical		
Oversampled 6/ dynamic range		f_{IN} = 1 kSPS	-55°C to +105°C	01	125 typical		dB
Signal to noise		f_{IN} = 1 kHz, V_{REF} = 5 V	-55°C to +105°C	01	98.5		dB
					101 typical		
			-40°C to +85°C		100		
					101.5 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC Accuracy – continued. 5/							
Signal to noise		f_{IN} = 1 kHz, V_{REF} = 2.5 V	-55°C to +105°C	01	94		dB
					96 typical		
			-40°C to +85°C		95		
					96.5 typical		
Spurious free dynamic range		f_{IN} = 1 kHz, V_{REF} = 5 V	-55°C to +105°C	01	-125 typical		dB
Total harmonic distortion	THD	f_{IN} = 1 kHz, V_{REF} = 5 V	-55°C to +105°C	01	-118 typical		dB
Signal to noise and distortion ratio	SINAD	f_{IN} = 1 kHz, V_{REF} = 5 V	-55°C to +105°C	01	98.5		dB
					101 typical		
			-40°C to +85°C		100		
					101.5 typical		
		f_{IN} = 1 kHz, V_{REF} = 2.5 V	-55°C to +105°C		94		
					96 typical		
			-40°C to +85°C		95		
					96.5 typical		
Intermodulation 7/ distortion			-55°C to +105°C	01	115 typical		dB
Reference							
Voltage range			-55°C to +105°C	01	0.5	V_{DD} + 0.3	V
Load current		250 kSPS, REF = 5 V	-55°C to +105°C	01	60 typical		µA
Sampling dynamics							
-3 dB input bandwidth			-55°C to +105°C	01	2 typical		MHz
Aperture delay		V_{DD} = 5 V	-55°C to +105°C	01	2.5 typical		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital inputs							
Low level input voltage	V_{IL}		-55°C to +105°C	01	-0.3	+0.3 x V_{IO}	V
High level input voltage	V_{IH}		-55°C to +105°C	01	0.7 x V_{IO}	V_{IO} + 0.3	V
Low level input current	I_{IL}		-55°C to +105°C	01	-1	+1	µA
High level input current	I_{IH}		-55°C to +105°C	01	-1	+1	µA
Digital outputs							
Data format		Serial 18 bit, twos complement					
Pipeline delay 8/							
Low level output voltage	V_{OL}	I_{SINK} = +500 µA	-55°C to +105°C	01		0.4	V
High level output voltage	V_{OH}	I_{SOURCE} = -500 µA	-55°C to +105°C	01	V_{IO} – 0.3		V
Power supplies							
V_{DD} range		Specified performance	-55°C to +105°C	01	2.3	5.25	V
V_{IO} range		Specified performance	-55°C to +105°C	01	2.3	V_{DD} + 0.3	V
V_{IO} range		Functional operation	-55°C to +105°C	01	1.8	V_{DD} + 0.3	V
Standby current 9/ 10/		V_{DD} and V_{IO} = 5 V	+25°C	01		50	nA
					1 typical		
Power dissipation	PD	V_{DD} = 2.5 V, 100 SPS throughput	-55°C to +105°C	01	1.4 typical		µW
		V_{DD} = 2.5 V, 100 kSPS throughput			1.35 typical		mW
		V_{DD} = 2.5 V, 180 kSPS throughput			2.4 typical		
		V_{DD} = 5 V, 100 kSPS throughput				5	
					4.24 typical		
		V_{DD} = 5 V, 250 kSPS throughput				12.5	
					10.6 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supplies – continued.							
Energy per conversion			-55°C to +105°C	01	50 typical		nJ / sample
Timing specifications		See figures 3 and 4.					
Conversion time	t_{CONV}	CNV rising edge to data available	-55°C to +105°C	01	0.5	2.2	µs
Acquisition time	t_{ACQ}		-55°C to +105°C	01	1.8		µs
Time between conversions	t_{CYC}		-55°C to +105°C	01	4		µs
CNV pulse width ($\overline{CS}$ mode)	t_{CNVH}		-55°C to +105°C	01	10		ns
SCK period ($\overline{CS}$ mode)	t_{SCK}		-55°C to +105°C	01	15		ns
SCK period (chain mode)	t_{SCK}	V_{IO} above 4.5 V	-55°C to +105°C	01	17		ns
		V_{IO} above 3 V			18		
		V_{IO} above 2.7 V			19		
		V_{IO} above 2.3 V			20		
SCK low time	t_{SCKL}		-55°C to +105°C	01	7		ns
SCK high time	t_{SCKH}		-55°C to +105°C	01	7		ns
SCK falling edge to data remains valid	t_{HSDO}		-55°C to +105°C	01	4		ns
SCK falling edge to data valid delay	t_{DSDO}	V_{IO} above 4.5 V	-55°C to +105°C	01		14	ns
		V_{IO} above 3 V				15	
		V_{IO} above 2.7 V				16	
		V_{IO} above 2.3 V				17	
CNV or SDI low to SDO D17 MSB valid ($\overline{CS}$ mode)	t_{EN}	V_{IO} above 4.5 V	-55°C to +105°C	01		15	ns
		V_{IO} above 2.7 V				18	
		V_{IO} above 2.3 V				23	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications – continued.		See figures 3 and 4.					
CNV or SDI high or last SCK falling edge to SDO high impedance ($\overline{CS}$ mode)	t_{DIS}		-55°C to +105°C	01		25	ns
SDI valid setup time from CNV rising edge ($\overline{CS}$ mode)	$t_{SSDICNV}$		-55°C to +105°C	01	15		ns
SDI valid hold time from CNV rising edge ($\overline{CS}$ mode)	$t_{HSDICNV}$		-55°C to +105°C	01	0		ns
SCK valid setup time from CNV rising edge (chain mode)	$t_{SSCKCNV}$		-55°C to +105°C	01	5		ns
SCK valid hold time from CNV rising edge (chain mode)	$t_{HSCKCNV}$		-55°C to +105°C	01	10		ns
SDI valid setup time from SCK falling edge (chain mode)	$t_{SSDISCK}$		-55°C to +105°C	01	3		ns
SDI valid hold time from SCK falling edge (chain mode)	$t_{HSDISCK}$		-55°C to +105°C	01	4		ns
SDI high to SDO high (chain mode with busy indicator)	$t_{DSDOSDI}$	V_{IO} above 4.5 V	-55°C to +105°C	01		15	ns
		V_{IO} above 2.3 V				26	
Conversion time	t_{CONV}	CNV rising edge to data available	-55°C to +105°C	01	0.5	3.7	µs
Acquisition time	t_{ACQ}		-55°C to +105°C	01	1.8		µs
Time between conversions	t_{CYC}		-55°C to +105°C	01	5.5		µs
CNV pulse width ($\overline{CS}$ mode)	t_{CNVH}		-55°C to +105°C	01	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications – continued.		See figures 3 and 4.					
SCK period ($\overline{CS}$ mode)	t_{SCK}		-55°C to +105°C	01	25		ns
SCK period (chain mode)	t_{SCK}	V_{IO} above 3 V	-55°C to +105°C	01	29		ns
		V_{IO} above 2.7 V			35		
		V_{IO} above 2.3 V			40		
SCK low time	t_{SCKL}		-55°C to +105°C	01	12		ns
SCK high time	t_{SCKH}		-55°C to +105°C	01	12		ns
SCK falling edge to data remains valid	t_{HSDO}		-55°C to +105°C	01	5		ns
SCK falling edge to data valid delay	t_{DSDO}	V_{IO} above 3 V	-55°C to +105°C	01		24	ns
		V_{IO} above 2.7 V				30	
		V_{IO} above 2.3 V				35	
CNV or SDI low to SDO D17 MSB valid ($\overline{CS}$ mode)	t_{EN}	V_{IO} above 2.7 V	-55°C to +105°C	01		18	ns
		V_{IO} above 2.3 V				22	
CNV or SDI high or last SCK falling edge to SDO high impedance ($\overline{CS}$ mode)	t_{DIS}		-55°C to +105°C	01		25	ns
SDI valid setup time from CNV rising edge ($\overline{CS}$ mode)	$t_{SSDICNV}$		-55°C to +105°C	01	30		ns
SDI valid hold time from CNV rising edge ($\overline{CS}$ mode)	$t_{HSDICNV}$		-55°C to +105°C	01	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications – continued.		See figures 3 and 4.					
SCK valid setup time from CNV rising edge (chain mode)	$t_{SSCKCNV}$		-55°C to +105°C	01	5		ns
SCK valid hold time from CNV rising edge (chain mode)	$t_{HSCKCNV}$		-55°C to +105°C	01	8		ns
SDI valid setup time from SCK falling edge (chain mode)	$t_{SSDISCK}$		-55°C to +105°C	01	8		ns
SDI valid hold time from SCK falling edge (chain mode)	$t_{HSDISCK}$		-55°C to +105°C	01	10		ns
SDI high to SDO high (chain mode with busy indicator)	$t_{DSDOSDI}$		-55°C to +105°C	01		36	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = 2.3 V to 5.25 V, V_{IO} = 2.3 V to V_{DD}, V_{REF} = V_{DD}, and all specifications -55°C to 105°C.

3/ LSB means least significant bit. With the ±5 V input range, one LSB = 38.15 μV.

4/ See terminology section of the manufacturer's data sheet. These specifications include full temperature range variation but, not the error contribution from the external reference.

5/ Unless otherwise specified, all ac accuracy specifications in dB are referred to a full scale input FSR. Tested with an input signal at 0.5 dB below full scale.

6/ Dynamic range obtained by oversampling the ADC running at a throughput f_S of 250 kSPS, followed by post digital filtering with an output word rate f_O.

7/ fI_{N1} = 21.4 kHz and f_{IN2} = 18.8 kHz, with each tone at -7 dB below full scale.

8/ Conversion results are available immediately after completed conversion.

9/ With all digital inputs forced to V_{IO} or GND as required.

10/ During acquisition phase.

Case X

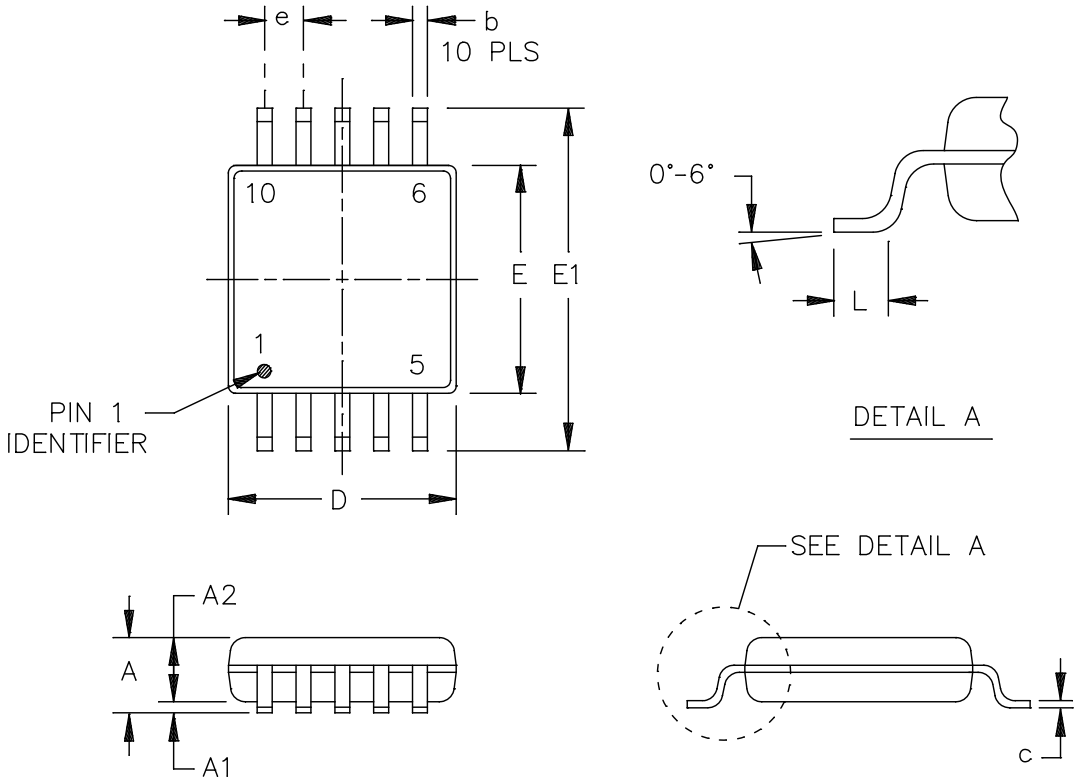

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14632
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Symbol	Dimensions					
	Inches			Millimeters		
	Min	Med	Max	Min	Med	Max
A	---	---	0.043	---	---	1.10
A1	0.0019	---	0.0059	0.05	---	0.15
A2	0.029	0.033	0.037	0.75	0.85	0.95
b	0.0059	---	0.012	0.15	---	0.33
c	0.0051	---	0.009	0.13	---	0.23
D	0.114	0.118	0.122	2.90	3.00	3.10
E	0.114	0.118	0.122	2.90	3.00	3.10
E1	0.183	0.192	0.202	4.65	4.90	5.15
e	0.019 BSC			0.050 BSC		
L	0.015	0.021	0.027	0.40	0.55	0.70

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-187-BA.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
1	REF	AI	Reference input voltage. The REF range is from 0.5 V to V_{DD}. It is referred to the GND pin. Decouple this pin closely with a 10 µF capacitor.
2	V_{DD}	P	Power supply.
3	+INPUT	AI	Differential positive analog input. Referenced to –INPUT. The input range for +INPUT is between 0 V and V_{REF}, centered about $V_{REF}/2$ and must be driven 180° out of phase with –INPUT.
4	-INPUT	AI	Differential negative analog input. Referenced to +INPUT. The input range for –INPUT is between 0 V and V_{REF}, centered about $V_{REF}/2$ and must be driven 180° out of phase with +INPUT.
5	GND	P	Power supply ground.
6	CNV	DI	Convert input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the device, either chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial data output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial data clock input. When the device is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial data input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 18 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low, and if SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	VIO	P	Input/output interface digital power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).

AI = analog input, DI = digital input, DO = digital output, and P = power.

FIGURE 2. Terminal connections.

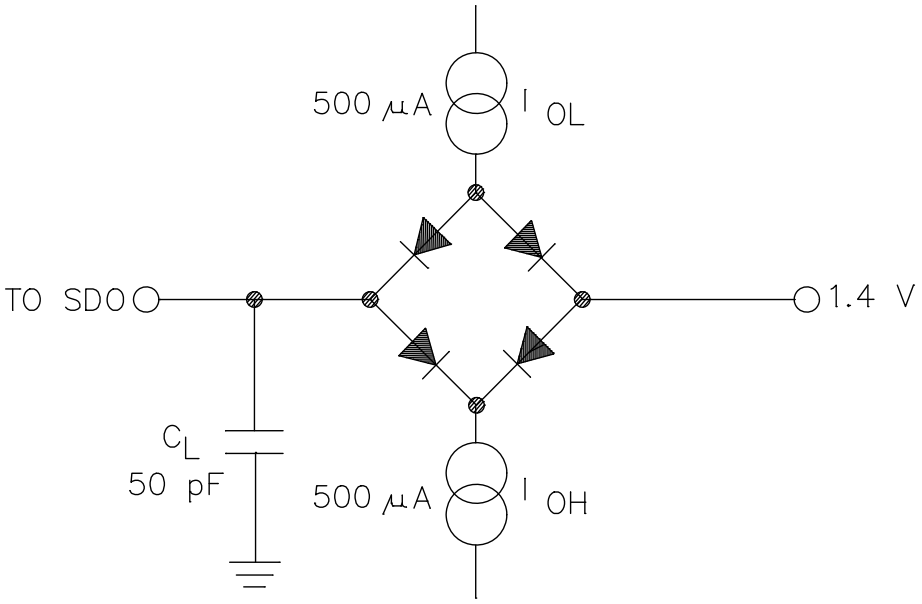
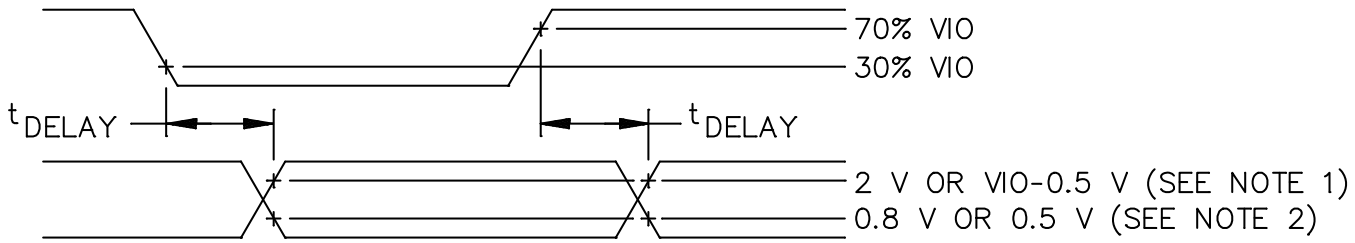


FIGURE 3. Load circuit for digital interface timing.



NOTES:

1. 2 V if V_{IO} above 2.5 V, V_{IO} – 0.5 V if V_{IO} below 2.5 V
2. 0.8 V if V_{IO} above 2.5 V, 0.5 V if V_{IO} below 2.5 V.

FIGURE 4. Voltage levels for timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/14632-01XE	24355	C82	AD7691SRMZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland