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<th>LTR</th>
<th>DESCRIPTION</th>
<th>DATE</th>
<th>APPROVED</th>
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</thead>
</table>

Prepared in accordance with ASME Y14.24

**Vendor item drawing**

<table>
<thead>
<tr>
<th>REV</th>
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<th>REV</th>
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<table>
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<th>REV STATUS OF PAGES</th>
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<tr>
<td>REV</td>
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<tr>
<td>PAGE</td>
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<td>1</td>
</tr>
</tbody>
</table>

Original date of drawing: YY-MM-DD

**PMIC N/A**

**PREPARED BY**

RICK OFFICER

**CHECKED BY**

RAJESH PITHADIA

**APPROVED BY**

CHARLES F. SAFFLE

**TITLE**

MICROCIRCUIT, LINEAR, QUAD CHANNEL DIGITAL ISOLATOR, MONOLITHIC SILICON

**SIZE**

A

**CODE IDENT. NO.**

16236

**DWG NO.**

V62/14631

**PAGE**

1 OF 25
1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quad channel, digital isolator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer’s PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<table>
<thead>
<tr>
<th>Drawing number</th>
<th>Device type</th>
<th>Case outline</th>
<th>Lead finish</th>
</tr>
</thead>
<tbody>
<tr>
<td>V62/14631</td>
<td>- 01 X E</td>
<td>(See 1.2.1)</td>
<td>(See 1.2.2)</td>
</tr>
</tbody>
</table>

1.2.1 Device type(s).

Device type | Generic | Circuit function
---|---|---
01 | ADUM3402 | Quad channel, digital isolator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<table>
<thead>
<tr>
<th>Outline letter</th>
<th>Number of pins</th>
<th>JEDEC PUB 95</th>
<th>Package style</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>16</td>
<td>MS-013-AA</td>
<td>Small outline surface mount</td>
</tr>
</tbody>
</table>

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<table>
<thead>
<tr>
<th>Finish designator</th>
<th>Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Hot solder dip</td>
</tr>
<tr>
<td>B</td>
<td>Tin-lead plate</td>
</tr>
<tr>
<td>C</td>
<td>Gold plate</td>
</tr>
<tr>
<td>D</td>
<td>Palladium</td>
</tr>
<tr>
<td>E</td>
<td>Gold flash palladium</td>
</tr>
<tr>
<td>Z</td>
<td>Other</td>
</tr>
</tbody>
</table>
1.3 Absolute maximum ratings. 1/

Supply voltages (V_{DD1}, V_{DD2}) ................................................................. -0.5 V to +7.0 V 2/
Input voltages (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2}) ........................................... -0.5 V to V_{DDI} + 0.5 V 2/ 3/
Output voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD}) .......................................................... -0.5 V to V_{DDO} + 0.5 V 2/ 3/
Average output current per pin: 4/
   Side 1 (I_{O1}) .................................................................................................... -18 mA to +18 mA
   Side 2 (I_{O2}) .................................................................................................... -22 mA to +22 mA
Common mode transients (CM_H, CM_L) ................................................................. -100 kV/\mu s to +100 kV/\mu s 5/
Storage temperature range (T_{STG}) ...................................................................... -65^\circ C to +150^\circ C

1.4 Recommended operating conditions. 6/

Supply voltages (V_{DD1}, V_{DD2}) ................................................................. 3.135 V to 5.5 V 2/
Input signal rise and fall times ............................................................................ 1.0 ms
Operating temperature range (T_A) ........................................................................ -55^\circ C to +125^\circ C

1.5 Package characteristics.

Resistance (input to output) (R_{IO}) ........................................................................ 10^{12} \Omega typical 7/
Capacitance (input to output) (C_{IO}) with f = 1 MHz ............................................ 2.2 pF typical 7/
Input capacitance (C_I) .......................................................................................... 4.0 pF typical 8/
Integrated circuit junction to case thermal resistance:
   Thermocouple located at center of package underside.
   Side 1 (\theta_{JCI}) .................................................................................................. 33^\circ C/W typical
   Side 2 (\theta_{JCO}) ............................................................................................... 28^\circ C/W typical

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltages are relative to their respective ground.
3/ V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
4/ See figure 5 for maximum rated current values for various temperatures.
5/ Refers to common mode transients across the insulation barrier. Common mode transients exceeding the absolute maximum ratings can cause latch up or permanent damage.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
7/ Device considered a 2 terminal device; V_{DD1} pin to GND1 pin are shorted together, and GND2 pin to V_{DD2} pin are shorted together.
8/ Input capacitance is from any input data pin to ground.
2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 — Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

   A. Manufacturer's name, CAGE code, or logo
   B. Pin 1 identifier
   C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Thermal derating curve. The thermal derating curve shall be as shown in figure 5.

3.5.6 Data rate graphs. The data rate graphs shall be as shown in figures 6 through 9.
TABLE I. Electrical performance characteristics. 1/

<table>
<thead>
<tr>
<th>Test</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Temperature, $T_A$</th>
<th>Device type</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>5 V operation 2/</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC specifications</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input supply current per channel, quiescent</td>
<td>$I_{DDI(Q)}$</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>0.83</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td></td>
<td>0.57 typical</td>
<td></td>
</tr>
<tr>
<td>Output supply current per channel, quiescent</td>
<td>$I_{DDO(Q)}$</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>0.35</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td></td>
<td>0.29 typical</td>
<td></td>
</tr>
<tr>
<td>Total supply current 3/</td>
<td>DC to 2 Mbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD1}$ or $V_{DD2}$ supply current</td>
<td>$I_{DD1(Q)}$, $I_{DD2(Q)}$</td>
<td>DC to 1 MHz logical signal frequency</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>2.8</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td></td>
<td>2.0 typical</td>
<td></td>
</tr>
<tr>
<td>Total supply current 3/</td>
<td>10 Mbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD1}$ or $V_{DD2}$ supply current</td>
<td>$I_{DD1(10)}$, $I_{DD2(10)}$</td>
<td>5 MHz logical signal frequency</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>7.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td></td>
<td>6.0 typical</td>
<td></td>
</tr>
<tr>
<td>DC specifications</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input leakage per channel</td>
<td>$I_I$</td>
<td>$0 \leq V_{IX} \leq V_{DDX}$</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>-10</td>
<td>+10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td></td>
<td>+0.01 typical</td>
<td></td>
</tr>
<tr>
<td>$V_{EX}$ input pull up current</td>
<td>$I_{PU}$</td>
<td>$V_{EX} = 0$ V</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>-10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td></td>
<td>-3 typical</td>
<td></td>
</tr>
<tr>
<td>Tristate leakage current per channel</td>
<td>$I_{OZ}$</td>
<td></td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>-10</td>
<td>+10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td></td>
<td>+0.01 typical</td>
<td></td>
</tr>
<tr>
<td>Logic high input threshold</td>
<td>$V_{IH}$, $V_{EH}$</td>
<td></td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>Logic low input threshold</td>
<td>$V_{IL}$, $V_{EL}$</td>
<td></td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>0.8</td>
<td></td>
</tr>
</tbody>
</table>

See footnotes at end of table.
### TABLE I. Electrical performance characteristics – Continued. 1/

<table>
<thead>
<tr>
<th>Test Conditions</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Temperature, TA</th>
<th>Device type</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 V operation 2/</td>
<td>VOAHV, VOBH</td>
<td>IOX = -20 µA, VIX = VIXH</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>(VDD1 or VDD2) - 0.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>5.0 typical</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VOCH, VODH</td>
<td>IOX = -4 mA, VIX = VIXH</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>(VDD1 or VDD2) - 0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>4.8 typical</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VOAL, VOABL</td>
<td>IOX = 20 µA, VIX = VIXL</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>0.0 typical</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VOCL, VODL</td>
<td>IOX = 400 µA, VIX = VIXL</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>0.04 typical</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>IOX = 4 mA, VIX = VIXL</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>0.2 typical</td>
<td></td>
</tr>
</tbody>
</table>

Switching specifications.

| Minimum pulse width | PW | C_L = 15 pF, CMOS signal levels | -55°C to +125°C | 01 | 100 | ns |
| Maximum data rate | C_L = 15 pF, CMOS signal levels | -55°C to +125°C | 01 | 10 | Mbps |
| Propagation delay | tPHL, tPLH | C_L = 15 pF, CMOS signal levels | -55°C to +125°C | 01 | 20 | 50 | ns |
|         |             |            | +25°C          |             | 32 typical |      |
| Pulse width distortion | | C_L = 15 pF, CMOS signal levels | -55°C to +125°C | 01 | 3 | ns |
| Pulse width distortion | | C_L = 15 pF, CMOS signal levels | +25°C          |             | 5 typical | ps/°C |
|         | | change versus temperature |            |             |            |      |
| Propagation delay skew | tPSK | C_L = 15 pF, CMOS signal levels | -55°C to +125°C | 01 | 15 | ns |

See footnotes at end of table.
TABLE I. Electrical performance characteristics – Continued. 1/

<table>
<thead>
<tr>
<th>Test</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Temperature, $T_A$</th>
<th>Device type</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching specifications – continued.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel to channel matching, codirectional channels</td>
<td>$t_{PSKCD}$</td>
<td>$C_L = 15 \text{ pF}, \text{CMOS signal levels}$</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>3</td>
<td>ns</td>
</tr>
<tr>
<td>Channel to channel matching, opposing directional channels</td>
<td>$t_{PSKOD}$</td>
<td>$C_L = 15 \text{ pF}, \text{CMOS signal levels}$</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>Output propagation delay, disable (high/low to high impedance)</td>
<td>$t_{PHZ}$, $t_{PLZ}$</td>
<td>$C_L = 15 \text{ pF}, \text{CMOS signal levels}$</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>6 typical</td>
<td></td>
</tr>
<tr>
<td>Output propagation delay, enable (high impedance to high/low)</td>
<td>$t_{PHZ}$, $t_{PLZ}$</td>
<td>$C_L = 15 \text{ pF}, \text{CMOS signal levels}$</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>6 typical</td>
<td></td>
</tr>
<tr>
<td>Output rise/fall time (10% to 90%)</td>
<td>$t_{R}$ / $t_{F}$</td>
<td>$C_L = 15 \text{ pF}, \text{CMOS signal levels}$</td>
<td>+25°C</td>
<td>01</td>
<td>2.5 typical</td>
<td>ns</td>
</tr>
<tr>
<td>Common mode transient immunity logic high output</td>
<td>$</td>
<td>CM_H</td>
<td>$</td>
<td>$V_IX = V_{DD1}/V_{DD2}, V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V</td>
<td>-55°C to +125°C</td>
<td>01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>35 typical</td>
<td></td>
</tr>
<tr>
<td>Common mode transient immunity logic low output</td>
<td>$</td>
<td>CM_L</td>
<td>$</td>
<td>$V_IX = 0 \text{ V}, V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V</td>
<td>-55°C to +125°C</td>
<td>01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>35 typical</td>
<td></td>
</tr>
<tr>
<td>Refresh rate</td>
<td>$fr$</td>
<td></td>
<td>+25°C</td>
<td>01</td>
<td>1.2 typical</td>
<td>Mbps</td>
</tr>
<tr>
<td>Dynamic supply current per channel, input</td>
<td>$I_{DDI(D)}$</td>
<td>8/</td>
<td>+25°C</td>
<td>01</td>
<td>0.20 typical</td>
<td>mA/Mbps</td>
</tr>
<tr>
<td>Dynamic supply current per channel, output</td>
<td>$I_{DDO(D)}$</td>
<td>8/</td>
<td>+25°C</td>
<td>01</td>
<td>0.05 typical</td>
<td>mA/Mbps</td>
</tr>
</tbody>
</table>

See footnotes at end of table.
<table>
<thead>
<tr>
<th>Test</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Temperature, $T_A$</th>
<th>Device type</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC specifications</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input supply current per channel, quiescent</td>
<td>$I_{DDI}(Q)$</td>
<td>$3.3$ V operation $9/\text{D}$</td>
<td>$-55^\circ \text{C}$ to $+125^\circ \text{C}$</td>
<td>01</td>
<td>0.49</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>+25$^\circ\text{C}$</td>
<td></td>
<td></td>
<td></td>
<td>0.31 typical</td>
<td></td>
</tr>
<tr>
<td>Output supply current per channel, quiescent</td>
<td>$I_{DDO}(Q)$</td>
<td>$3.3$ V operation $9/\text{D}$</td>
<td>$-55^\circ \text{C}$ to $+125^\circ \text{C}$</td>
<td>01</td>
<td>0.27</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>+25$^\circ\text{C}$</td>
<td></td>
<td></td>
<td></td>
<td>0.19 typical</td>
<td></td>
</tr>
<tr>
<td>Total supply current</td>
<td>$3/\text{D}$</td>
<td>DC to 2 Mbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD1}$ or $V_{DD2}$ supply current</td>
<td>$I_{DD1(Q)}$, $I_{DD2(Q)}$</td>
<td>DC to 1 MHz logical signal frequency</td>
<td>$-55^\circ \text{C}$ to $+125^\circ \text{C}$</td>
<td>01</td>
<td>1.7</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>+25$^\circ\text{C}$</td>
<td></td>
<td></td>
<td></td>
<td>1.2 typical</td>
<td></td>
</tr>
<tr>
<td>Total supply current</td>
<td>$3/\text{D}$</td>
<td>10 Mbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD1}$ or $V_{DD2}$ supply current</td>
<td>$I_{DD1(10)}$, $I_{DD2(10)}$</td>
<td>5 MHz logical signal frequency</td>
<td>$-55^\circ \text{C}$ to $+125^\circ \text{C}$</td>
<td>01</td>
<td>4.4</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>+25$^\circ\text{C}$</td>
<td></td>
<td></td>
<td></td>
<td>3.4 typical</td>
<td></td>
</tr>
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<td>DC specifications</td>
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<td>Logic low input threshold</td>
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TABLE I. Electrical performance characteristics – Continued. 1/

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Switching specifications

| | | | | | | |
| Minimum pulse width | $PW$ | $C_L = 15 \mu F$, CMOS signal levels | -55°C to +125°C | 01 | 100 | ns |
| Maximum data rate | | | -55°C to +125°C | 01 | 10 | Mbps |
| Propagation delay | $t_{PHL}$, $t_{PLH}$ | $C_L = 15 \mu F$, CMOS signal levels | -55°C to +125°C | 01 | 20 | 50 | ns |
| | | | +25°C | | 38 typical |
| Pulse width distortion | $|t_{PLH} - t_{PHL}|$ | $C_L = 15 \mu F$, CMOS signal levels | -55°C to +125°C | 01 | 3 | ns |
| Pulse width distortion | $|t_{PLH} - t_{PHL}|$ change versus temperature | $C_L = 15 \mu F$, CMOS signal levels | +25°C | 01 | 5 typical | ps°C |
| Propagation delay skew | $t_{PSK}$ | $C_L = 15 \mu F$, CMOS signal levels | -55°C to +125°C | 01 | 22 | ns |

See footnotes at end of table.
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<td>$t_{PSKCD}$</td>
<td>$C_L = 15 , \text{pF}, , \text{CMOS signal levels}$</td>
<td>-55°C to +125°C</td>
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<td>ns</td>
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<td>Channel to channel matching, opposing directional channels</td>
<td>$t_{PSKOD}$</td>
<td>$C_L = 15 , \text{pF}, , \text{CMOS signal levels}$</td>
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<td>ns</td>
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<td>Output propagation delay, disable (high/low to high impedance)</td>
<td>$t_{PHZ}$, $t_{PLZ}$</td>
<td>$C_L = 15 , \text{pF}, , \text{CMOS signal levels}$</td>
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<td>8</td>
<td>ns</td>
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<td>Output propagation delay, enable (high impedance to high/low)</td>
<td>$t_{PZH}$, $t_{PZL}$</td>
<td>$C_L = 15 , \text{pF}, , \text{CMOS signal levels}$</td>
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<td>ns</td>
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<td>Output rise/fall time (10% to 90%)</td>
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<td>CM_H</td>
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<td>$V_{IX} = V_{DD1}/V_{DD2}, , V_{CM} = 1000 , \text{V}$, transient magnitude = 800 V</td>
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<td>Common mode transient immunity logic low output</td>
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<td>CM_L</td>
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<td>$V_{IX} = 0 , \text{V}, , V_{CM} = 1000 , \text{V}$, transient magnitude = 800 V</td>
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<td>Refresh rate</td>
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### TABLE I. Electrical performance characteristics – Continued. 1/

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<td>$V_{DD2}$ supply current</td>
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<td>01</td>
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<td>+10</td>
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<td>$V_{EX} = 0$ V</td>
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<td>Tristate leakage current per channel</td>
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<td>$V_{IH}$, $V_{EH}$</td>
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<td>(VDD1 or VDD2) – 0.1</td>
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<td>+25°C</td>
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<td>(VDD1 or VDD2) typical</td>
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<td>$V_{OCH}$, $V_{ODH}$</td>
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<td>(VDD1 or VDD2) – 0.4</td>
<td>V</td>
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<td>(VDD1 or VDD2) – 0.2 typical</td>
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<td>$V_{OAL}$, $V_{OBL}$</td>
<td>$I_{OX} = 20 \mu A$, $V_{IX} = V_{IXL}$ 4/6</td>
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<td>01</td>
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<td>V</td>
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<td>+25°C</td>
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<td>0.0 typical</td>
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<td>$V_{OCL}$, $V_{ODL}$</td>
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<td>+25°C</td>
<td></td>
<td>0.04 typical</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{OX} = 4 mA$, $V_{IX} = V_{IXL}$ 4/6</td>
<td>-55°C to +125°C</td>
<td></td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>0.2 typical</td>
<td></td>
</tr>
<tr>
<td>Switching specifications</td>
<td>Minimum pulse width</td>
<td>PW</td>
<td>$C_L = 15$ pF, CMOS signal levels</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>Maximum data rate</td>
<td></td>
<td></td>
<td></td>
<td>01</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Propagation delay</td>
<td>$t_{PHL}$, $t_{PLH}$</td>
<td>$C_L = 15$ pF, CMOS signal levels</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td></td>
<td>35 typical</td>
</tr>
<tr>
<td></td>
<td>Pulse width distortion</td>
<td>$</td>
<td>t_{PLH} – t_{PHL}</td>
<td>$</td>
<td>$C_L = 15$ pF, CMOS signal levels</td>
<td>-55°C to +125°C</td>
</tr>
<tr>
<td></td>
<td>Pulse width distortion</td>
<td></td>
<td>$</td>
<td>t_{PLH} – t_{PHL}</td>
<td>$ change versus temperature</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Propagation delay skew</td>
<td>$t_{PSK}$</td>
<td>$C_L = 15$ pF, CMOS signal levels</td>
<td>-55°C to +125°C</td>
<td>01</td>
<td>22</td>
</tr>
</tbody>
</table>

See footnotes at end of table.
TABLE I. Electrical performance characteristics – Continued. 1/

<table>
<thead>
<tr>
<th>Test</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Temperature, $T_A$</th>
<th>Device type</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching specifications – continued.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel to channel matching, codirectional channels</td>
<td>$t_{PSKCD}$</td>
<td>$C_L = 15$ pF, CMOS signal levels</td>
<td>$-55^\circ$C to $+125^\circ$C</td>
<td>01</td>
<td>3</td>
<td>ns</td>
</tr>
<tr>
<td>Channel to channel matching, opposing directional channels</td>
<td>$t_{PSKOD}$</td>
<td>$C_L = 15$ pF, CMOS signal levels</td>
<td>$-55^\circ$C to $+125^\circ$C</td>
<td>01</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>Output propagation delay, disable (high/low to high impedance)</td>
<td>$t_{PHZ}$, $t_{PLZ}$</td>
<td>$C_L = 15$ pF, CMOS signal levels</td>
<td>$-55^\circ$C to $+125^\circ$C</td>
<td>01</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$+25^\circ$C</td>
<td></td>
<td>6 typical</td>
<td></td>
</tr>
<tr>
<td>Output propagation delay, enable (high impedance to high/low)</td>
<td>$t_{PZH}$, $t_{PZL}$</td>
<td>$C_L = 15$ pF, CMOS signal levels</td>
<td>$-55^\circ$C to $+125^\circ$C</td>
<td>01</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$+25^\circ$C</td>
<td></td>
<td>6 typical</td>
<td></td>
</tr>
<tr>
<td>Output rise/fall time (10% to 90%)</td>
<td>$t_R$ / $t_F$</td>
<td>$C_L = 15$ pF, CMOS signal levels, 5 V / 3.3 V operation</td>
<td>$+25^\circ$C</td>
<td>01</td>
<td>3 typical</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$C_L = 15$ pF, CMOS signal levels, 3.3 V / 5 V operation</td>
<td></td>
<td>2.5 typical</td>
<td></td>
</tr>
<tr>
<td>Common mode transient immunity logic high output</td>
<td>$</td>
<td>CM_H</td>
<td>$</td>
<td>$V_{IX} = V_{DD1/VDD2}$, $V_{CM} = 1000$ V, transient magnitude = 800 V</td>
<td>$-55^\circ$C to $+125^\circ$C</td>
<td>01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$+25^\circ$C</td>
<td></td>
<td>35 typical</td>
<td></td>
</tr>
<tr>
<td>Common mode transient immunity logic low output</td>
<td>$</td>
<td>CM_L</td>
<td>$</td>
<td>$V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V</td>
<td>$-55^\circ$C to $+125^\circ$C</td>
<td>01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$+25^\circ$C</td>
<td></td>
<td>35 typical</td>
<td></td>
</tr>
<tr>
<td>Refresh rate</td>
<td>$fr$</td>
<td></td>
<td></td>
<td>01</td>
<td>1.2 typical</td>
<td>Mbps</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.1 typical</td>
<td></td>
</tr>
</tbody>
</table>

See footnotes at end of table.
### TABLE I. Electrical performance characteristics – Continued. 1/

<table>
<thead>
<tr>
<th>Test</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Temperature, $T_A$</th>
<th>Device type</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic supply current per channel, input</td>
<td>$I_{DDI}(D)$</td>
<td>5 V / 3.3 V operation 8/</td>
<td>+25°C</td>
<td>01</td>
<td>0.20 typical</td>
<td>mA/ Mbps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3 V / 5 V operation 8/</td>
<td></td>
<td></td>
<td>0.10 typical</td>
<td></td>
</tr>
<tr>
<td>Dynamic supply current per channel, output</td>
<td>$I_{DDO}(D)$</td>
<td>5 V / 3.3 V operation 8/</td>
<td>+25°C</td>
<td>01</td>
<td>0.03 typical</td>
<td>mA/ Mbps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3 V / 5 V operation 8/</td>
<td></td>
<td></td>
<td>0.05 typical</td>
<td></td>
</tr>
</tbody>
</table>

See footnotes at end of table.
TABLE I. Electrical performance characteristics – Continued. 1/  

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All voltages are relative to their respective ground. $4.5 \text{ V} \leq V_{DD1} \leq 5.5 \text{ V}$ and $4.5 \text{ V} \leq V_{DD2} \leq 5.5 \text{ V}$. Unless otherwise specified, all minimum / maximum specifications apply over the entire recommended operation range. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5 \text{ V}$.

3/ The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. See figures 6 through 8 for information on per channel supply current as a function of data rate for unloaded and loaded conditions. See figures 9 and 10 for total $V_{DD1}$ and $V_{DD2}$ supply currents as a function of data rate for device channel configurations.

4/ $I_{OX}$ is the channel X output current, where $X = A$, $B$, $C$, or $D$.

5/ $V_{IXH}$ is the input side logic high.

6/ $V_{IXL}$ is the input side logic low.

7/ $CM_H$ is the maximum common mode voltage slew rate that can be sustained while maintaining the $(V_{OUT}) > 0.8 \text{ V}_{DD2}$. $CM_L$ is the maximum common mode voltage slew rate that can be sustained while maintain $V_{OUT} < 0.8 \text{ V}$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

8/ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See figures 6 through 8 for information on per channel supply current for unloaded and loaded conditions.

9/ All voltages are relative to their respective ground. $3.135 \text{ V} \leq V_{DD1} \leq 3.6 \text{ V}$ and $3.135 \text{ V} \leq V_{DD2} \leq 3.6 \text{ V}$. Unless otherwise specified, all minimum / maximum specifications apply over the entire recommended operation range. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.3 \text{ V}$.

10/ All voltages are relative to their respective ground. For 5 V / 3.3 V operation, $4.5 \text{ V} \leq V_{DD1} \leq 5.5 \text{ V}$ and $3.135 \text{ V} \leq V_{DD2} \leq 3.6 \text{ V}$, and for 3.3 V / 5 V operation, $3.135 \text{ V} \leq V_{DD1} \leq 3.6 \text{ V}$ and $4.5 \text{ V} \leq V_{DD2} \leq 5.5 \text{ V}$. Unless otherwise specified, all minimum / maximum specifications apply over the entire recommended operation range. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 3.3 \text{ V}$, $V_{DD2} = 5 \text{ V}$ or $V_{DD1} = 5 \text{ V}$, $V_{DD2} = 3.3 \text{ V}$.
FIGURE 1. Case outline.
### Case X – continued.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions</th>
<th>Inches</th>
<th>Millimeters</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td></td>
<td>0.0925</td>
<td>0.1043</td>
</tr>
<tr>
<td>A1</td>
<td></td>
<td>0.0039</td>
<td>0.0118</td>
</tr>
<tr>
<td>b</td>
<td></td>
<td>0.0122</td>
<td>0.0201</td>
</tr>
<tr>
<td>c</td>
<td></td>
<td>0.0079</td>
<td>0.0130</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td>0.3976</td>
<td>0.4134</td>
</tr>
<tr>
<td>E</td>
<td></td>
<td>0.2913</td>
<td>0.2992</td>
</tr>
<tr>
<td>E1</td>
<td></td>
<td>0.3937</td>
<td>0.4193</td>
</tr>
<tr>
<td>e</td>
<td></td>
<td>0.0500 BSC</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td></td>
<td>0.0157</td>
<td>0.0500</td>
</tr>
<tr>
<td>n</td>
<td></td>
<td>16</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within JEDEC MS-013 variation AA.

**FIGURE 1.** Case outline - continued.
<table>
<thead>
<tr>
<th>Terminal number</th>
<th>Terminal symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD1</td>
<td>Supply voltage for isolator side 1, 3.135 V to 5.5 V.</td>
</tr>
<tr>
<td>2</td>
<td>GND1</td>
<td>Ground 1. Ground reference for isolator side 1. See note 1</td>
</tr>
<tr>
<td>3</td>
<td>V_IA</td>
<td>Logic input A.</td>
</tr>
<tr>
<td>4</td>
<td>V_IB</td>
<td>Logic input B.</td>
</tr>
<tr>
<td>5</td>
<td>VOC</td>
<td>Logic output C.</td>
</tr>
<tr>
<td>6</td>
<td>VOD</td>
<td>Logic output D.</td>
</tr>
<tr>
<td>7</td>
<td>VE1</td>
<td>Output enable 1. Active high logic input. VOC and VOD outputs are enabled when VE1 is high or disconnected. VOC and VOD outputs are disabled when VE1 is low. In noisy environments, connecting VE1 to an external logic high or low is recommended.</td>
</tr>
<tr>
<td>8</td>
<td>GND1</td>
<td>Ground 1. Ground reference for isolator side 1. See note 1</td>
</tr>
<tr>
<td>10</td>
<td>VE2</td>
<td>Output enable 2. Active high logic input. VOA and VOB outputs are enabled when VE2 is high or disconnected. VOA and VOB outputs are disabled when VE2 is low. In noisy environments, connecting VE2 to an external logic high or low is recommended.</td>
</tr>
<tr>
<td>11</td>
<td>V_ID</td>
<td>Logic input D.</td>
</tr>
<tr>
<td>12</td>
<td>V_IC</td>
<td>Logic input C.</td>
</tr>
<tr>
<td>13</td>
<td>V_OB</td>
<td>Logic output B.</td>
</tr>
<tr>
<td>14</td>
<td>V_OA</td>
<td>Logic output A.</td>
</tr>
<tr>
<td>16</td>
<td>VDD2</td>
<td>Supply voltage for isolator side 2, 3.135 V to 5.5 V.</td>
</tr>
</tbody>
</table>

NOTE:
1. Both GND1 pins are internally connected and connecting both to GND1 is recommended. Both GND2 pins are internally connected and connecting both to GND2 is recommended. In noisy environments, connecting output enables (VE1 and VE2) to an external logic high or low is recommended.

FIGURE 2. Terminal connections.
### Positive logic

<table>
<thead>
<tr>
<th>$V_{IX}$ input</th>
<th>$V_{EX}$ input</th>
<th>$V_{DDI}$ state</th>
<th>$V_{DDO}$ state</th>
<th>$V_{OX}$ output</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>H or NC</td>
<td>Powered</td>
<td>Powered</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H or NC</td>
<td>Powered</td>
<td>Powered</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>Powered</td>
<td>Powered</td>
<td>Z</td>
<td>Outputs return to the input state within 1 $\mu$s of $V_{DDI}$ power restoration.</td>
</tr>
<tr>
<td>X</td>
<td>H or NC</td>
<td>Unpowered</td>
<td>Powered</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>Unpowered</td>
<td>Powered</td>
<td>Z</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>Powered</td>
<td>Unpowered</td>
<td>Indeterminate</td>
<td>Outputs return to the input state within 1 $\mu$s of $V_{DDO}$ power restoration if $V_{EX}$ state is H or NC. Outputs return to high impedance state within 8 ns of $V_{DDO}$ power restoration if $V_{EX}$ state is L.</td>
</tr>
</tbody>
</table>

1/ $V_{IX}$ and $V_{OX}$ refer to the input and output signals of a given channel (A, B, C, or D). $V_{EX}$ refers to the output enable signal on the same side as the $V_{OX}$ outputs. $V_{DDI}$ and $V_{DDO}$ refer to the supply voltages on the input and output sides of the given channel, respectively.

2/ H is high, L is low, X is don’t care, and NC is no connect.

3/ In noisy environments, connecting $V_{EX}$ to an external logic high or low is recommended.

**FIGURE 3.** Truth table.
FIGURE 4. Logic diagram.
FIGURE 5. Thermal derating curve.
FIGURE 6. Typical input supply current per channel versus data rate (no load).

FIGURE 7. Typical output supply current per channel versus data rate (no load).
FIGURE 8. Typical output supply current per channel versus data rate (15 pF output load).

FIGURE 9. Typical VDD1 or VDD2 supply current versus data rate for 5 V and 3.3 V operation.
4. VERIFICATION

4.1 **Product assurance requirements.** The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 **Packaging.** Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 **ESDS.** Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 **Configuration control.** The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 **Suggested source(s) of supply.** Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at [http://www.landandmaritime.dla.mil/Programs/Smcr/](http://www.landandmaritime.dla.mil/Programs/Smcr/).

<table>
<thead>
<tr>
<th>Vendor item drawing administrative control number 1/</th>
<th>Device manufacturer CAGE code</th>
<th>Vendor part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>V62/14631-01XE</td>
<td>24355</td>
<td>ADUM3402TRWZ-EP</td>
</tr>
</tbody>
</table>

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

<table>
<thead>
<tr>
<th>CAGE code</th>
<th>Source of supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>24355</td>
<td>Analog Devices</td>
</tr>
<tr>
<td></td>
<td>Route 1 Industrial Park</td>
</tr>
<tr>
<td></td>
<td>P.O. Box 9106</td>
</tr>
<tr>
<td></td>
<td>Norwood, MA 02062</td>
</tr>
<tr>
<td></td>
<td>Point of contact: Raheen Business Park</td>
</tr>
<tr>
<td></td>
<td>Limerick, Ireland</td>
</tr>
</tbody>
</table>