

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Make changes to IOx conditions under all VOH and VOL tests as specified in Table I. Update document paragraphs to current requirements. - ro	20-06-04	J. ESCHMEYER



Prepared in accordance with ASME Y14.24

Vendor item drawing

<b>REV</b>																				
<b>PAGE</b>																				
<b>REV</b>	A	A	A	A																
<b>PAGE</b>	18	19	20	21																
<b>REV STATUS OF PAGES</b>	<b>REV</b>		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	<b>PAGE</b>		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

<b>PMIC N/A</b>	<b>PREPARED BY</b> RICK OFFICER	<b>DLA LAND AND MARITIME</b> <b>COLUMBUS, OHIO 43218-3990</b> <a href="https://www.dla.mil/LandandMaritime">https://www.dla.mil/LandandMaritime</a>
Original date of drawing YY-MM-DD  15-06-26	<b>CHECKED BY</b> RAJESH PITHADIA	<b>TITLE</b> MICROCIRCUIT, LINEAR, DUAL CHANNEL DIGITAL ISOLATOR, ENHANCED SYSTEM LEVEL ESD RELIABILITY, MONOLITHIC SILICON
	<b>APPROVED BY</b> CHARLES F. SAFFLE	
	<b>SIZE</b> <b>A</b>	<b>CODE IDENT. NO.</b> <b>16236</b>
	<b>REV</b> <b>A</b>	<b>PAGE 1 OF 21</b>

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a dual channel digital isolator, enhanced system level electrostatic discharge (ESD) reliability microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/14627</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
---------------------------------------	---	---	---	--

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ADUM3210TRZ-EP	Dual channel digital isolator, enhanced system level ESD reliability

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MS-012-AA	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		REV    A	PAGE    2

1.3 Absolute maximum ratings. 1/

Supply voltages range (VDD1, VDD2) .....	-0.5 V to +7.0 V 2/
Input voltage (VIA, VIB) .....	-0.5 V to VDD1 + 0.5 V 2/ 3/
Output voltage (VOA, VOB) .....	-0.5 V to VDD0 + 0.5 V 2/ 3/
Average output current per pin (IO) .....	-22 mA to +22 mA 4/
Common mode transients (CMH, CML) .....	-100 kV/μs to +100 kV/μs 5/
Storage temperature range (TSTG) .....	-55°C to +150°C

1.4 Recommended operating conditions. 6/

Supply voltages (VDD1, VDD2) .....	3 V to 5.5 V 7/
Maximum input signal rise and fall times .....	1 ms
Start-up current (IDD1, IDD2) .....	20 mA
Operating free-air temperature range (TA) .....	-55°C to +125°C

1.5 Package characteristics.

Resistance (input to output) (RI-O) .....	10 <sup>12</sup> Ω typical 8/
Capacitance (input to output) (CI-O) (f = 1 MHz) .....	1.0 pF typical 8/
Input capacitance (CI) .....	4.0 pF typical
Thermal resistance, junction to case (θJC1) side 1 .....	46°C/W typical
Thermocouple located at center of package underside	
Thermal resistance, junction to case (θJCO) side 2 .....	41°C/W typical

- 
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
  - 2/ Each voltage is relative to its respective ground.
  - 3/ VDD1 and VDD0 refer to the supply voltages on the input and output sides of a given channel, respectively.
  - 4/ See figure 4 for maximum allowable current values for various temperatures.
  - 5/ Refers to common mode transients across the insulation barrier. Common mode transients exceeding the absolute maximum rating can cause latch up or permanent damage.
  - 6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
  - 7/ All voltages are relative to their respective ground.
  - 8/ The device is considered a 2 terminal device. Pin 1 through pin 4 are shorted together, and pin 5 through pin 8 are shorted together.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		REV    A	PAGE    3

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

<p align="center"><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p align="center"><b>SIZE A</b></p>	<p align="center"><b>CODE IDENT NO. 16236</b></p>	<p align="center"><b>DWG NO. V62/14627</b></p>
		<p align="center">REV     A</p>	<p align="center">PAGE    4</p>

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u> VDD1 = VDD2 = 5 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Supply current	IDD1	1 Mbps	-55°C to +125°C	01		1.7	mA
			+25°C			1.3 typical	
		10 Mbps	-55°C to +125°C			4.8	
			+25°C			3.5 typical	
		25 Mbps	-55°C to +125°C			9.9	
			+25°C			7.6 typical	
	IDD2	1 Mbps	-55°C to +125°C			1.6	
			+25°C			1.0 typical	
		10 Mbps	-55°C to +125°C			2.8	
			+25°C			2.0 typical	
		25 Mbps	-55°C to +125°C			5.1	
			+25°C			3.8 typical	
Switching specifications.							
Data rate		Within PWD limit	-55°C to +125°C	01		25	Mbps
Propagation delay	tPHL, tPLH	50% input to 50% output	-55°C to +125°C	01	20	50	ns
Pulse width distortion	PWD	tPLH - tPHL	-55°C to +125°C	01		3	ns
Pulse width distortion change vs temperature			+25°C	01	5 typical		ps/°C
Pulse width	PW	Within PWD limit	-55°C to +125°C	01	40		ns
Propagation delay skew	tPSK	Between any two units	-55°C to +125°C	01		18	ns
Channel matching: codirectional	tPSKCD		-55°C to +125°C	01		3	ns
Channel matching: opposing directional	tPSKOD		-55°C to +125°C	01		18	ns
Output rise/fall time	tR / tF	10% to 90%	+25°C	01	2.5 typical		ns

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		REV    A	PAGE    5

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u> VDD1 = VDD2 = 5 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
DC specifications.							
Logic high input threshold	V <sub>IH</sub>		-55°C to +125°C	01	0.7 VDD <sub>x</sub>		V
Logic low input threshold	V <sub>IL</sub>		-55°C to +125°C	01		0.3 VDD <sub>x</sub>	V
Logic high output voltages	V <sub>OH</sub>	I <sub>Ox</sub> = -20 μA, V <sub>Ix</sub> = V <sub>IxH</sub>	-55°C to +125°C	01	VDD <sub>x</sub> - 0.1		V
			+25°C		VDD <sub>x</sub> typical		
		I <sub>Ox</sub> = -3.2 mA, V <sub>Ix</sub> = V <sub>IxH</sub>	-55°C to +125°C		VDD <sub>x</sub> - 0.5		
			+25°C		VDD <sub>x</sub> - 0.2 typical		
Logic low output voltages	V <sub>OL</sub>	I <sub>Ox</sub> = 20 μA, V <sub>Ix</sub> = V <sub>IxL</sub>	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
		I <sub>Ox</sub> = 3.2 mA, V <sub>Ix</sub> = V <sub>IxL</sub>	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Input current per channel	I <sub>I</sub>	0 V ≤ V <sub>Ix</sub> ≤ VDD <sub>x</sub>	-55°C to +125°C	01	-10	+10	μA
			+25°C		+0.01 typical		
Supply current per channel.							
Quiescent input supply current	IDD <sub>I(Q)</sub>		-55°C to +125°C	01		0.8	mA
			+25°C		0.4 typical		
Quiescent output supply current	IDD <sub>O(Q)</sub>		-55°C to +125°C	01		0.8	mA
			+25°C		0.4 typical		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		<b>REV A</b>	<b>PAGE 6</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u> VDD1 = VDD2 = 5 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Supply current per channel – continued.							
Dynamic input supply current	IDDI(D)		+25°C	01	0.19 typical		mA/ Mbps
Dynamic output supply current	IDDO(D)		+25°C	01	0.05 typical		mA/ Mbps
AC specifications.							
Common mode <u>3/</u> transient immunity	CM	V <sub>Ix</sub> = VDD <sub>x</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/μs
			+25°C		35 typical		
Refresh rate	fr		+25°C	01	1.2 typical		Mbps

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		REV    A	PAGE    7

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 4/ VDD1 = VDD2 = 3.3 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Supply current	IDD1	1 Mbps	-55°C to +125°C	01		1.3	mA
			+25°C		0.8 typical		
		10 Mbps	-55°C to +125°C			3.2	
			+25°C		2.1 typical		
		25 Mbps	-55°C to +125°C			6.1	
			+25°C		4.6 typical		
	IDD2	1 Mbps	-55°C to +125°C			1.0	
			+25°C		0.7 typical		
		10 Mbps	-55°C to +125°C			1.9	
			+25°C		1.3 typical		
		25 Mbps	-55°C to +125°C			3.4	
			+25°C		2.4 typical		
Switching specifications.							
Data rate		Within PWD limit	-55°C to +125°C	01		25	Mbps
Propagation delay	tPHL, tPLH	50% input to 50% output	-55°C to +125°C	01	20	60	ns
Pulse width distortion	PWD	tPLH –tPHL	-55°C to +125°C	01		4	ns
Pulse width distortion change vs temperature			+25°C	01	5 typical		ps/°C
Pulse width	PW	Within PWD limit	-55°C to +125°C	01	40		ns
Propagation delay skew	tPSK	Between any two units	-55°C to +125°C	01		22	ns
Channel matching: codirectional	tPSKCD		-55°C to +125°C	01		3	ns
Channel matching: opposing directional	tPSKOD		-55°C to +125°C	01		20	ns
Output rise/fall time	tR / tF	10% to 90%	+25°C	01	3.0 typical		ns

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		<b>REV     A</b>	<b>PAGE    8</b>



TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>4/</u> VDD1 = VDD2 = 3.3 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
DC specifications.							
Logic high input threshold	V <sub>IH</sub>		-55°C to +125°C	01	0.7 VDD <sub>x</sub>		V
Logic low input threshold	V <sub>IL</sub>		-55°C to +125°C	01		0.3 VDD <sub>x</sub>	V
Logic high output voltages	V <sub>OH</sub>	I <sub>Ox</sub> = -20 μA, V <sub>Ix</sub> = V <sub>IxH</sub>	-55°C to +125°C	01	VDD <sub>x</sub> - 0.1		V
			+25°C		VDD <sub>x</sub> typical		
		I <sub>Ox</sub> = -3.2 mA, V <sub>Ix</sub> = V <sub>IxH</sub>	-55°C to +125°C		VDD <sub>x</sub> - 0.5		
			+25°C		VDD <sub>x</sub> - 0.2 typical		
Logic low output voltages	V <sub>OL</sub>	I <sub>Ox</sub> = 20 μA, V <sub>Ix</sub> = V <sub>IxL</sub>	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
		I <sub>Ox</sub> = 3.2 mA, V <sub>Ix</sub> = V <sub>IxL</sub>	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Input current per channel	I <sub>I</sub>	0 V ≤ V <sub>Ix</sub> ≤ VDD <sub>x</sub>	-55°C to +125°C	01	-10	+10	μA
			+25°C		+0.01 typical		
Supply current per channel.							
Quiescent input supply current	I <sub>DDI(Q)</sub>		-55°C to +125°C	01		0.5	mA
			+25°C		0.3 typical		
Quiescent output supply current	I <sub>DDO(Q)</sub>		-55°C to +125°C	01		0.5	mA
			+25°C		0.3 typical		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		<b>REV A</b>	<b>PAGE 9</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>4/</u> VDD1 = VDD2 = 3.3 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Supply current per channel – continued.							
Dynamic input supply current	IDDI(D)		+25°C	01	0.10 typical		mA/ Mbps
Dynamic output supply current	IDDO(D)		+25°C	01	0.03 typical		mA/ Mbps
AC specifications.							
Common mode <u>3/</u> transient immunity	CM	V <sub>Ix</sub> = VDD <sub>x</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/μs
			+25°C		35 typical		
Refresh rate	fr		+25°C	01	1.1 typical		Mbps

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		REV    A	PAGE    10

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5/ VDD1 = 5 V, VDD2 = 3.3 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Supply current	IDD1	1 Mbps	-55°C to +125°C	01		1.7	mA
			+25°C		1.3 typical		
		10 Mbps	-55°C to +125°C			4.8	
			+25°C		3.5 typical		
		25 Mbps	-55°C to +125°C			9.9	
			+25°C		7.6 typical		
	IDD2	1 Mbps	-55°C to +125°C			1.0	
			+25°C		0.7 typical		
		10 Mbps	-55°C to +125°C			1.9	
			+25°C		1.3 typical		
		25 Mbps	-55°C to +125°C			3.4	
			+25°C		2.4 typical		
Switching specifications.							
Data rate		Within PWD limit	-55°C to +125°C	01		25	Mbps
Propagation delay	tPHL, tPLH	50% input to 50% output	-55°C to +125°C	01	15	55	ns
Pulse width distortion	PWD	tPLH – tPHL	-55°C to +125°C	01		3	ns
Pulse width distortion change vs temperature			+25°C	01	5 typical		ps/°C
Pulse width	PW	Within PWD limit	-55°C to +125°C	01	40		ns
Propagation delay skew	tPSK	Between any two units	-55°C to +125°C	01		22	ns
Channel matching: codirectional	tPSKCD		-55°C to +125°C	01		3	ns
Channel matching: opposing directional	tPSKOD		-55°C to +125°C	01		20	ns
Output rise/fall time	tR / tF	10% to 90%	+25°C	01	3.0 typical		ns

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		<b>REV     A</b>	<b>PAGE    11</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>5/</u> VDD1 = 5 V, VDD2 = 3.3 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
DC specifications.							
Logic high input threshold	V <sub>IH</sub>		-55°C to +125°C	01	0.7 VDD <sub>x</sub>		V
Logic low input threshold	V <sub>IL</sub>		-55°C to +125°C	01		0.3 VDD <sub>x</sub>	V
Logic high output voltages	V <sub>OH</sub>	I <sub>Ox</sub> = -20 μA, V <sub>Ix</sub> = V <sub>IxH</sub>	-55°C to +125°C	01	VDD <sub>x</sub> - 0.1		V
			+25°C		VDD <sub>x</sub> typical		
		I <sub>Ox</sub> = -3.2 mA, V <sub>Ix</sub> = V <sub>IxH</sub>	-55°C to +125°C		VDD <sub>x</sub> - 0.5		
			+25°C		VDD <sub>x</sub> - 0.2 typical		
Logic low output voltages	V <sub>OL</sub>	I <sub>Ox</sub> = 20 μA, V <sub>Ix</sub> = V <sub>IxL</sub>	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
		I <sub>Ox</sub> = 3.2 mA, V <sub>Ix</sub> = V <sub>IxL</sub>	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Input current per channel	I <sub>I</sub>	0 V ≤ V <sub>Ix</sub> ≤ VDD <sub>x</sub>	-55°C to +125°C	01	-10	+10	μA
			+25°C		+0.01 typical		
Supply current per channel.							
Quiescent input supply current	IDD <sub>I(Q)</sub>		-55°C to +125°C	01		0.8	mA
			+25°C		0.4 typical		
Quiescent output supply current	IDD <sub>O(Q)</sub>		-55°C to +125°C	01		0.5	mA
			+25°C		0.3 typical		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		<b>REV A</b>	<b>PAGE 12</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>5/</u> VDD1 = 5 V, VDD2 = 3.3 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Supply current per channel – continued.							
Dynamic input supply current	IDDI(D)		+25°C	01	0.19 typical		mA/ Mbps
Dynamic output supply current	IDDO(D)		+25°C	01	0.03 typical		mA/ Mbps
AC specifications.							
Common mode <u>3/</u> transient immunity	CM	V <sub>Ix</sub> = VDD <sub>x</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/μs
			+25°C		35 typical		
Refresh rate	fr		+25°C	01	1.2 typical		Mbps

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		REV A	PAGE 13

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>6/</u> VDD1 = 3.3 V, VDD2 = 5.0 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Supply current	IDD1	1 Mbps	-55°C to +125°C	01		1.3	mA
			+25°C		0.8 typical		
		10 Mbps	-55°C to +125°C			3.2	
			+25°C		2.1 typical		
		25 Mbps	-55°C to +125°C			6.1	
			+25°C		4.6 typical		
	IDD2	1 Mbps	-55°C to +125°C			1.6	
			+25°C		1.0 typical		
		10 Mbps	-55°C to +125°C			2.8	
			+25°C		2.0 typical		
		25 Mbps	-55°C to +125°C			5.1	
			+25°C		3.7 typical		
Switching specifications.							
Data rate		Within PWD limit	-55°C to +125°C	01		25	Mbps
Propagation delay	tPHL, tPLH	50% input to 50% output	-55°C to +125°C	01	15	55	ns
Pulse width distortion	PWD	tPLH – tPHL	-55°C to +125°C	01		4	ns
Pulse width distortion change vs temperature			+25°C	01	5 typical		ps/°C
Pulse width	PW	Within PWD limit	-55°C to +125°C	01	40		ns
Propagation delay skew	tPSK	Between any two units	-55°C to +125°C	01		22	ns
Channel matching: codirectional	tPSKCD		-55°C to +125°C	01		3	ns
Channel matching: opposing directional	tPSKOD		-55°C to +125°C	01		20	ns
Output rise/fall time	tR / tF	10% to 90%	+25°C	01	2.5 typical		ns

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		REV    A	PAGE    14

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>6/</u> VDD1 = 3.3 V, VDD2 = 5.0 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
DC specifications.							
Logic high input threshold	V <sub>IH</sub>		-55°C to +125°C	01	0.7 VDD <sub>x</sub>		V
Logic low input threshold	V <sub>IL</sub>		-55°C to +125°C	01		0.3 VDD <sub>x</sub>	V
Logic high output voltages	V <sub>OH</sub>	I <sub>Ox</sub> = -20 μA, V <sub>Ix</sub> = V <sub>IxH</sub>	-55°C to +125°C	01	VDD <sub>x</sub> - 0.1		V
			+25°C		VDD <sub>x</sub> typical		
		I <sub>Ox</sub> = -3.2 mA, V <sub>Ix</sub> = V <sub>IxH</sub>	-55°C to +125°C		VDD <sub>x</sub> - 0.5		
			+25°C		VDD <sub>x</sub> - 0.2 typical		
Logic low output voltages	V <sub>OL</sub>	I <sub>Ox</sub> = 20 μA, V <sub>Ix</sub> = V <sub>IxL</sub>	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
		I <sub>Ox</sub> = 3.2 mA, V <sub>Ix</sub> = V <sub>IxL</sub>	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Input current per channel	I <sub>I</sub>	0 V ≤ V <sub>Ix</sub> ≤ VDD <sub>x</sub>	-55°C to +125°C	01	-10	+10	μA
			+25°C		+0.01 typical		
Supply current per channel.							
Quiescent input supply current	IDD <sub>I(Q)</sub>		-55°C to +125°C	01		0.8	mA
			+25°C		0.4 typical		
Quiescent output supply current	IDD <sub>O(Q)</sub>		-55°C to +125°C	01		0.8	mA
			+25°C		0.5 typical		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		<b>REV A</b>	<b>PAGE 15</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>6/</u> VDD1 = 3.3 V, VDD2 = 5.0 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Supply current per channel – continued.							
Dynamic input supply current	IDDI(D)		+25°C	01	0.10 typical		mA/ Mbps
Dynamic output supply current	IDDO(D)		+25°C	01	0.05 typical		mA/ Mbps
AC specifications.							
Common mode <u>3/</u> transient immunity	CM	V <sub>Ix</sub> = VDD <sub>x</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/μs
			+25°C		35 typical		
Refresh rate	fr		+25°C	01	1.1 typical		Mbps

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, minimum/maximum specification apply over the entire recommended operation range:  $4.5\text{ V} \leq \text{VDD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq \text{VDD2} \leq 5.5\text{ V}$ , and  $-55^\circ\text{C} \leq \text{TA} \leq +125^\circ\text{C}$ .  
Unless otherwise specified, switching specifications are tested with  $\text{CL} = 15\text{ pF}$  and CMOS signal levels.

3/ |CM| is the maximum common mode voltage slew rate that can be sustained while maintaining  $\text{VO} > 0.8\text{ VDD}$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

4/ Unless otherwise specified, minimum/maximum specification apply over the entire recommended operation range:  $3.0\text{ V} \leq \text{VDD1} \leq 3.6\text{ V}$ ,  $3.0\text{ V} \leq \text{VDD2} \leq 3.6\text{ V}$ , and  $-55^\circ\text{C} \leq \text{TA} \leq +125^\circ\text{C}$ .  
Unless otherwise specified, switching specifications are tested with  $\text{CL} = 15\text{ pF}$  and CMOS signal levels.

5/ Unless otherwise specified, minimum/maximum specification apply over the entire recommended operation range:  $4.5\text{ V} \leq \text{VDD1} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq \text{VDD2} \leq 3.6\text{ V}$ , and  $-55^\circ\text{C} \leq \text{TA} \leq +125^\circ\text{C}$ .  
Unless otherwise specified, switching specifications are tested with  $\text{CL} = 15\text{ pF}$  and CMOS signal levels.

6/ Unless otherwise specified, minimum/maximum specification apply over the entire recommended operation range:  $3.0\text{ V} \leq \text{VDD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq \text{VDD2} \leq 5.5\text{ V}$ , and  $-55^\circ\text{C} \leq \text{TA} \leq +125^\circ\text{C}$ .  
Unless otherwise specified, switching specifications are tested with  $\text{CL} = 15\text{ pF}$  and CMOS signal levels.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		<b>REV A</b>	<b>PAGE 16</b>



Case X

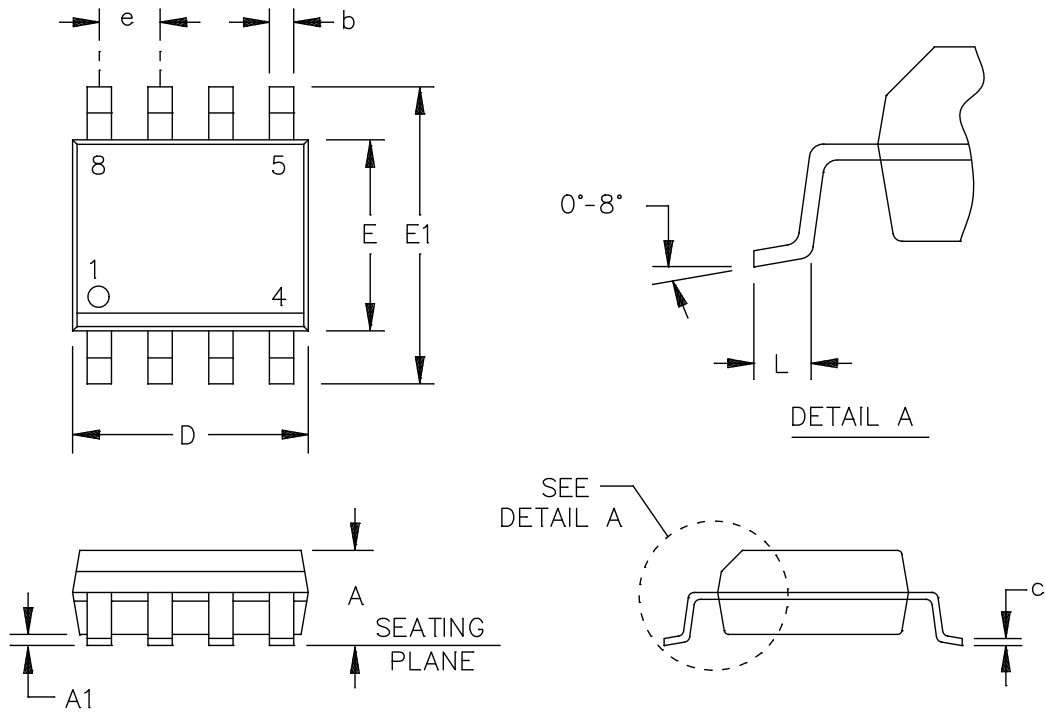


FIGURE 1. Case outline.

<p><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/14627</b></p>
		<p>REV    A</p>	<p>PAGE    17</p>

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.25
b	0.0122	0.0201	0.31	0.51
c	0.0067	0.0098	0.17	0.25
D	0.1890	0.1968	4.80	5.00
e	0.0500 BSC		1.27 BSC	
E	0.1497	0.1574	3.80	4.00
E1	0.2284	0.2441	5.80	6.20
L	0.0157	0.0500	0.40	1.27
n	8 leads		8 leads	

NOTE:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only and are not appropriate for use in design.
2. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		REV A	PAGE 18

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	VDD1	Supply voltage for isolator side 1, 3.0 V to 5.5 V
2	VIA	Logic input A.
3	VIB	Logic input B.
4	GND1	Ground 1. Ground reference for isolator side 1.
5	GND2	Ground 2. Ground reference for isolator side 2.
6	VOB	Logic output B
7	VOA	Logic output A.
8	VDD2	Supply voltage for isolator side 2, 3.0 V to 5.5 V

FIGURE 2. Terminal connections.

Positive logic

VIA input See note 1	VIB input See note 1	VDD1 state	VDD2 state	VOA output See note 1	VOB output See note 1	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	L	L	Outputs return to the input state within 1 $\mu$ s of VDDI power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 $\mu$ s of VDDO power restoration.

NOTE 1. H is logic high, L is logic low, and X is don't care.

FIGURE 3. Truth table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		REV A	PAGE 19

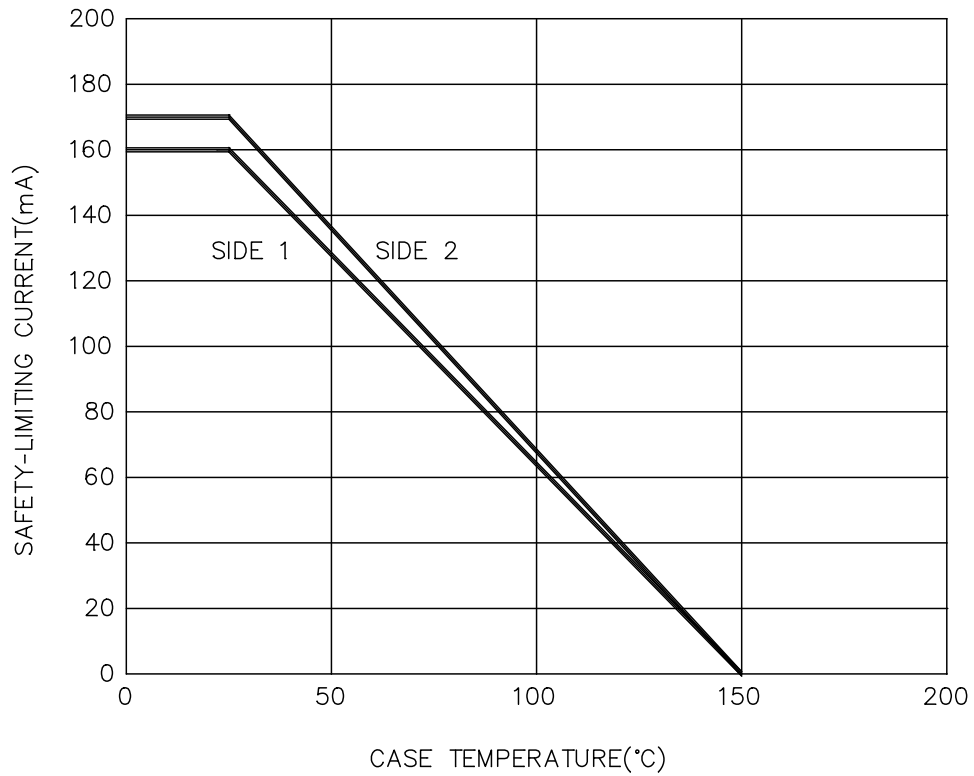


FIGURE 4. Thermal derating curve.

<p><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/14627</b></p>
		<p>REV    A</p>	<p>PAGE    20</p>

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/14627-01XE	24355	ADUM3210TRZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices  
 Route 1 Industrial Park  
 P.O. Box 9106  
 Norwood, MA 02062  
 Point of contact: 20 Alpha Road  
 Chelmsford, MA 01824-4123

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/14627</b>
		REV A	PAGE 21