

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Make correction to the vendor part number from OPA4277-EP to OPA4277MDTEP. - ro	15-08-12	C. SAFFLE



Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 <a href="http://www.landandmaritime.dla.mil/">http://www.landandmaritime.dla.mil/</a>
Original date of drawing YY-MM-DD  14-12-03	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, LINEAR, HIGH PRECISION OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE A	CODE IDENT. NO. 16236
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high precision operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/14625</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	OPA4277-EP	High speed operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	14	MS-012-AB	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage (V <sub>S</sub> ) .....	36 V maximum
Input voltage (V <sub>IN</sub> ) .....	-V <sub>S</sub> – 0.7 V to +V <sub>S</sub> + 0.7 V
Output short circuit .....	Continuous
Junction temperature (T <sub>J</sub> ) .....	150°C maximum
Lead temperature (soldering, 10 seconds) .....	+300°C maximum
Storage temperature range .....	-55°C to +125°C
Electrostatic discharge (ESD):	
Human body model (HBM) .....	-2,000 V to +2,000 V 2/
Machine model (MM) .....	-100 V to +100 V

1.4 Recommended operating conditions. 3/

Dual supply voltage range (V <sub>S</sub> ) .....	±5 V to ±15 V
Operating junction temperature range (T <sub>J</sub> ) .....	-55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ <sub>JA</sub>	66.3	°C/W
Thermal resistance, junction-to-case (top)	θ <sub>JC(TOP)</sub>	19.3	°C/W
Thermal resistance, junction-to-board	θ <sub>JB</sub>	26.8	°C/W
Characterization parameter, junction-to-top	ψ <sub>JT</sub>	2.1	°C/W
Characterization parameter, junction-to-board	ψ <sub>JB</sub>	26.2	°C/W
Thermal resistance, junction-to-case (bottom)	θ <sub>JC(BOTTOM)</sub>	Not applicable	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ JEDEC document JEP 155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices
- JEDEC JEP 155 - Recommended ESD Target Levels for HBM/MM Qualification

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $V_S = \pm 5 \text{ V to } \pm 15 \text{ V}$ and $R_L = 2 \text{ k}\Omega$ , unless otherwise specified	Temperature, $T_J$	Device type	Limits		Unit
					Min	Max	
Offset voltage							
Input offset voltage	$V_{OS}$		-55°C to +125°C	01		$\pm 140$	$\mu\text{V}$
			+25°C			$\pm 65$	
					$\pm 20$ typical		
Input offset voltage drift	$\Delta V_{OS} / \Delta T$		+25°C	01	$\pm 0.15$ typical		$\mu\text{V} / ^\circ\text{C}$
Input offset voltage	PSRR	versus time	+25°C	01	0.2 typical		$\mu\text{V} / \text{mo}$
		$V_S = \pm 2 \text{ V to } \pm 18 \text{ V}$	-55°C to +125°C			$\pm 1$	$\mu\text{V/V}$
		versus power supply, $V_S = \pm 2 \text{ V to } \pm 18 \text{ V}$	+25°C			$\pm 1$	
					$\pm 0.3$ typical		
Channel separation		dc	+25°C	01	0.1 typical		$\mu\text{V/V}$
Input bias current							
Input bias current	$I_{IB}$		-55°C to +125°C	01		7.5	nA
			+25°C			$\pm 2.8$	
					$\pm 0.5$ typical		
Input offset current	$I_{OS}$		-55°C to +125°C	01		7.5	nA
			+25°C			$\pm 2.8$	
					$\pm 0.5$ typical		
Noise							
Input voltage noise		f = 0.1 Hz to 10 Hz	+25°C	01	0.22 typical		$\mu\text{V}_{PP}$
Input voltage noise density	$e_n$	f = 10 Hz	+25°C	01	12 typical		$\text{nV} / \sqrt{\text{Hz}}$
		f = 100 Hz			8 typical		
		f = 1 kHz			8 typical		
		f = 10 kHz			8 typical		
Current noise density	$i_n$	f = 1 kHz	+25°C	01	0.2 typical		$\text{pA} / \sqrt{\text{Hz}}$

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 5 \text{ V}$ to $\pm 15 \text{ V}$ and $R_L = 2 \text{ k}\Omega$ , unless otherwise specified	Temperature, $T_J$	Device type	Limits		Unit
					Min	Max	
Input voltage							
Common mode voltage range	$V_{CM}$		+25°C	01	$-V_S + 2$	$+V_S - 2$	V
Common mode rejection ratio	CMRR	$V_{CM} = -V_S + 2 \text{ V}$ to $+V_S - 2 \text{ V}$	-55°C to +125°C	01	115		dB
			+25°C		115		
			140 typical				
Input impedance							
Differential		$\underline{2}$	+25°C	01	100  3 typical		$M\Omega    \mu F$
Common mode		$V_{CM} = -V_S + 2 \text{ V}$ to $+V_S - 2 \text{ V}$ $\underline{2}$	+25°C	01	250  3 typical		$G\Omega    \mu F$
Open loop gain							
Open loop voltage gain	AOL	$V_O = -V_S + 0.5 \text{ V}$ to $+V_S - 1.2 \text{ V}$ , $R_L = 10 \text{ k}\Omega$	+25°C	01	140 typical		dB
			-55°C to +125°C		126		
		+25°C	126				
		134 typical					
Open loop voltage gain	AOL	$V_O = -V_S + 1.5 \text{ V}$ to $+V_S - 1.5 \text{ V}$ , $R_L = 2 \text{ k}\Omega$	-55°C to +125°C	01	126		dB
			+25°C		126		
Frequency response							
Gain bandwidth product	GBW		+25°C	01	1 typical		MHz
Slew rate	SR		+25°C	01	0.8 typical		V/ $\mu$ s
Settling time	$t_s$	0.1%, $V_S = \pm 15 \text{ V}$ , $G = 1$ , 10 V step	+25°C	01	14 typical		$\mu$ s
		0.01%, $V_S = \pm 15 \text{ V}$ , $G = 1$ , 10 V step			16 typical		
Total harmonic distortion plus noise	THD + N	1 kHz, $G = 1$ , $V_O = 3.5 \text{ V}_{rms}$	+25°C	01	0.002 typical		%
Output.							
Voltage output	$V_O$	$R_L = 10 \text{ k}\Omega$	-55°C to +125°C	01	$-V_S + 0.5$	$+V_S - 1.2$	V
		$R_L = 2 \text{ k}\Omega$			$-V_S + 1.5$	$+V_S - 1.5$	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 5 \text{ V to } \pm 15 \text{ V}$ and $R_L = 2 \text{ k}\Omega$ , unless otherwise specified	Temperature, $T_J$	Device type	Limits		Unit
					Min	Max	
Output - continued.							
Short circuit current	$I_{SC}$		+25°C	01	±35 typical		mA
Power supply.							
Specified voltage	$V_S$		+25°C	01	±5	±15	V
Operating voltage			+25°C	01	±2	±18	V
Quiescent current (per amplifier)	$I_Q$	$I_O = 0$	-55°C to +125°C	01		±900	$\mu\text{A}$
			+25°C			±825	
			±790 typical				

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

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Case X

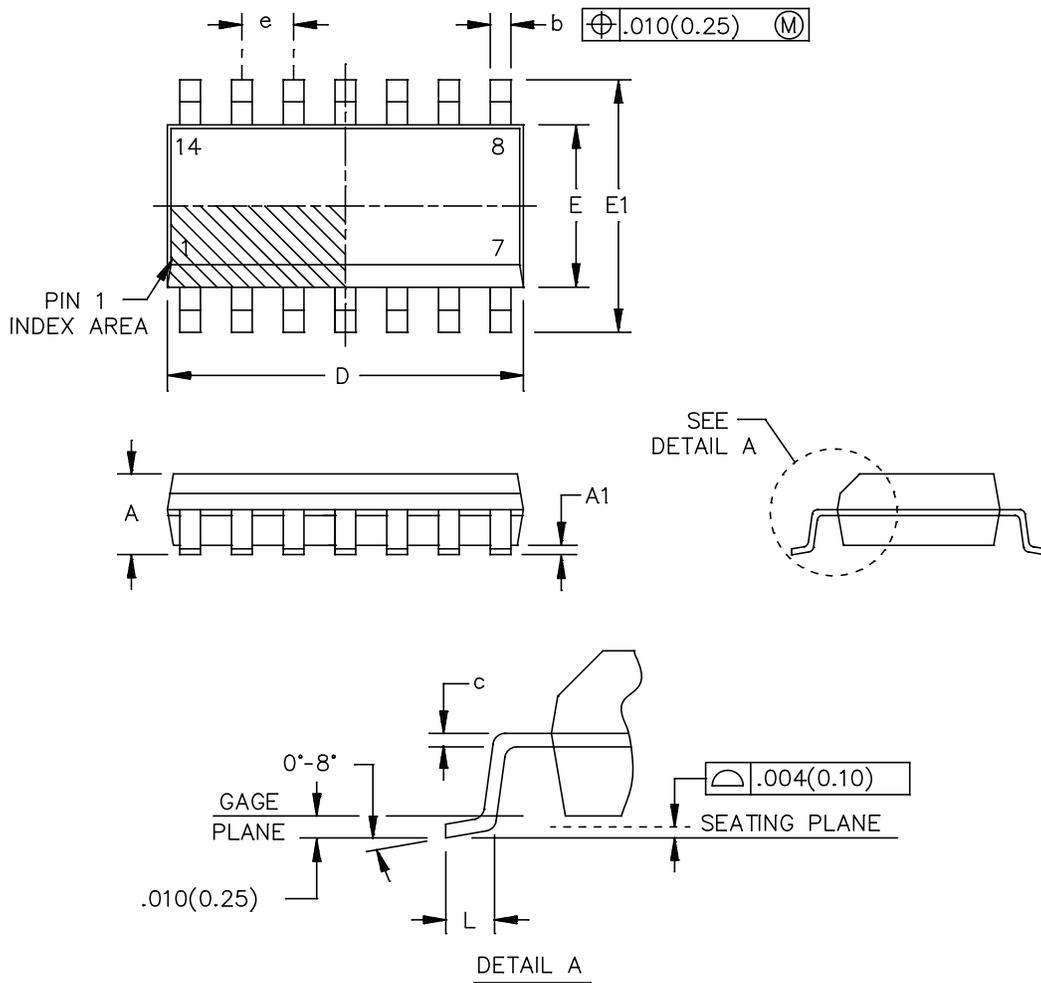


FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls within reference to JEDEC MS-012-AB.

FIGURE 1. Case outline.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUT A
2	-IN A
3	+IN A
4	+V <sub>S</sub>
5	+IN B
6	-IN B
7	OUT B
8	OUT C
9	-IN C
10	+IN C
11	-V <sub>S</sub>
12	+IN D
13	-IN D
14	OUT D

FIGURE 2. Terminal connections.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/14625-01XE	01295	OPA4277MDTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853

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