REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Under Table I, Power requirements section, DVCC test, add maximum limit of 5.25 V. Update document paragraphs to current requirements. - ro	20-10-08	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 14-05-13	**CHECKED BY** Phu H. Nguyen	TITLE MICROCIRCUIT, LINEAR-DIGITAL, COMPLETED QUAD, 16 BIT, HIGH ACCURACY, SERIAL INPUT, BIPOLAR VOLTAGE OUTPUT DAC, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/14622**
	REV **A**	**PAGE** 1 **OF** 15

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AMSC N/A

5962-V071-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance completed quad, 16-bit, high accuracy, serial input, bipolar voltage output digital to analog converter (DAC) microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14622	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5764-EP	Completed quad, 16-bit, high accuracy, serial input, bipolar voltage output DAC

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	32	JEDEC MS-026-AB A	Thin plastic quad flat package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

AV_{DD} to AGNDx, DGND	-0.3 V to +17 V
AV_{SS} to AGNDx, DGND	+0.3 V to -17 V
DV_{CC} to DGND	-0.3 V to +7 V
Digital inputs to DGND	-0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital outputs to DGND	-0.3 V to DV_{CC} + 0.3 V
REFAB, REFCD to AGNDx, PGND	-0.3 V to AV_{DD} + 0.3 V
VOUTA, VOUTB, VOUTC, VOUTD to AGNDx	AV_{SS} to AV_{DD}
AGNDx to DGND	-0.3 V to +0.3 V
Operating temperature range (Industrial)	-55°C to +105°C
Storage temperature range	-65°C to 150°C
Junction temperature (T_J max)	150°C
Case outline X:	
Thermal impedance, (θ_{JA})	65°C/W
Thermal impedance, (θ_{JC})	12°C/W
Lead temperature	JEDEC industry standard
Soldering	J-STD-020

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC J STD-020	–	Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Load circuit for SDO timing diagram. The load circuit for SDO timing diagram shall be as shown in figure 5.

3.5.6 Serial interface timing diagram. The serial interface timing diagram shall be as shown in figure 6.

3.5.7 Daisy-chain timing diagram. The daisy-chain timing diagram shall be as shown in figure 7.

3.5.8 Readback timing diagram. The readback timing diagram shall be as shown in figure 8.

3.5.9 Short circuit current versus R_{ISCC}. The Short circuit current versus R_{ISCC} shall be as shown in figure 9.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Accuracy (Outputs unloaded)						
Resolution			16			Bits
Relative Accuracy (INL)					±2	LSB
Differential Nonlinearity (DNL)		Guaranteed monotonic			±1	LSB
Bipolar Zero Error		At 25°C; error at other temperatures obtained using bipolar zero TC			±2	mV
Bipolar Zero Temperature Coefficient (TC) 3/					±2	ppm FSR/°C
Zero-Scale Error		At 25°C; error at other temperatures obtained using zero-scale TC			±3	mV
Zero-Scale TC 3/					±2	ppm FSR/°C
Gain Error		At 25°C; error at other temperatures obtained using zero-scale TC			±0.02	% FSR
Gain TC 3/					±2	ppm FSR/°C
DC Crosstalk 3/					0.5	LSB
Reference input 3/						
Reference Input Voltage		±1% for specified performance		5		V
DC Input Impedance		Typically 100 MΩ	1			MΩ
Input Current		Typically ±30 nA			±10	µA
Reference Range			1		7	V
Output characteristics 3/						
Output Voltage Range 4/		AV_{DD}/AV_{SS} = ±11.4 V, V_{REFIN} = 5 V	−10.5263		+10.5263	V
		AV_{DD}/AV_{SS} = ±16.5 V, V_{REFIN} = 7 V	−14		+14	
Output Voltage Drift vs.versus Time				±13		ppm FSR/ 500 hours
				±15		ppm FSR/ 1000 hours
Short-Circuit Current		R_{ISCC} = 6 kΩ; see Figure 9.		10		mA
Load Current		For specified performance			±1	mA
Capacitive Load Stability		R_{LOAD} = ∞			200	pF
		R_{LOAD} = 10 kΩ			1000	pF
DC Output Impedance					0.3	Ω
Digital Inputs						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current		Per pin			±1	µA
Pin Capacitance		Per Pin			10	pF

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Digital outputs (D0, D1, SDO) 3/						
Output low voltage	V_{OL}	DV_{CC} = 5 V ± 5%, sinking 200 µA			0.4	V
		DV_{CC} = 2.7 V to 3.6 V, sinking 200 µA			0.4	V
Output high voltage	V_{OH}	DV_{CC} = 5 V ± 5%, sourcing 200 µA	DV_{CC} − 1			V
		DV_{CC} = 2.7 V to 3.6 V, sourcing 200 µA	DV_{CC} − 0.5			
High Impedance Leakage Current		SDO only			±1	µA
High Impedance Output Capacitance		SDO only		5		pF
Power requirements						
AV_{DD}/AV_{SS}			±11.4		±16.5	V
DV_{CC}			2.7		5.25	V
Power Supply Sensitivity 3/	$\Delta V_{OUT}/\Delta AV_{DD}$			-85		dB
	AI_{DD}	Outputs unloaded			3.75	mA/channel
	AI_{SS}	Outputs unloaded			-3	mA/channel
DI_{CC}		V_{IH} = DV_{CC}, V_{IL} = DGND, 750 µA typical			1.4	mA
Power Dissipation		±12 V operation, output unloaded		275		mW
AC PERFORMANCE CHARACTERISTICS						
Dynamic performance 3/						
Output Voltage Settling Time		Full-scale step to ±1 LSB		8	10	µs
		512 LSB step settling		2		µs
Slew Rate				5		V/µs
Digital-to-Analog Glitch Energy				8		nV-sec
Glitch Impulse Peak Amplitude					37	mV p-p
Channel-to-Channel Isolation				80		dB
DAC-to-DAC Crosstalk				8		nV-sec
Digital Crosstalk				2		nV-sec
Digital Feed through		Effect of input bus activity on DAC outputs		2		nV-sec
Output Noise		0.1 Hz to 10 Hz		0.1		LSB p-p
		0.1 Hz to 100 kHz			45	µV rms
1/f Corner Frequency				1		kHz
Output Noise Spectral Density		Measured at 10 kHz		60		$nV/\sqrt{Hz}$
Complete System Output Noise Spectral Density 5/		Measured at 10 kHz		80		$nV/\sqrt{Hz}$

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test 3/ 6/ 7/	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
TIMING CHARACTERISTICS						
SCLK cycle time	t_1		33			ns
SCLK high time	t_2		13			ns
SCLK low time	t_3		13			ns
$\overline{SYNC}$ falling edge to SCLK falling edge setup time	t_4 8/		13			ns
24th SCLK falling edge to $\overline{SYNC}$ rising edge	t_5		13			ns
Minimum $\overline{SYNC}$ high time	t_6		90			ns
Data setup time	t_7		2			ns
Data hold time	t_8		9			ns
$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (all DACs updated)	t_9		1.7			µs
$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DACs updated)			480			ns
$\overline{LDAC}$ pulse width low	t_{10}		17			ns
$\overline{LDAC}$ falling edge to DAC output response time	t_{11}				500	ns
DAC output settling time	t_{12}				10	µs
$\overline{CLR}$ pulse width low	t_{13}		17			ns
$\overline{CLR}$ pulse activation time	t_{14}				2	µs
SCLK rising edge to SDO valid	t_{15} 9/ 10/				25	ns
$\overline{SYNC}$ rising edge to SCLK falling edge	t_{16}		13			ns
$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0)	t_{17}				2	µs
$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge	t_{18}		170			ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ AV_{DD} = 11.4 V to 16.5 V, AV_{SS} = −11.4 V to −16.5 V, AGNDx = DGND = REFGND = PGND = 0 V; REFAB = REFCD = 5 V; DV_{CC} = 2.7 V to 5.25 V, R_{LOAD} = 10 kΩ, C_{LOAD} = 200 pF. Temperature range: −55°C to +105°C; typical at +25°C.

All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

3/ Guaranteed by design and characterization; not production tested.

4/ Output amplifier headroom requirement is 1.4 V minimum.

5/ Includes noise contributions from integrated reference buffers, 16 bit DAC, and output amplifier.

6/ All input signals are specified with t_R = t_F = 5 ns (10% to 90% of DVCC) and timed from a voltage level of 1.2 V.

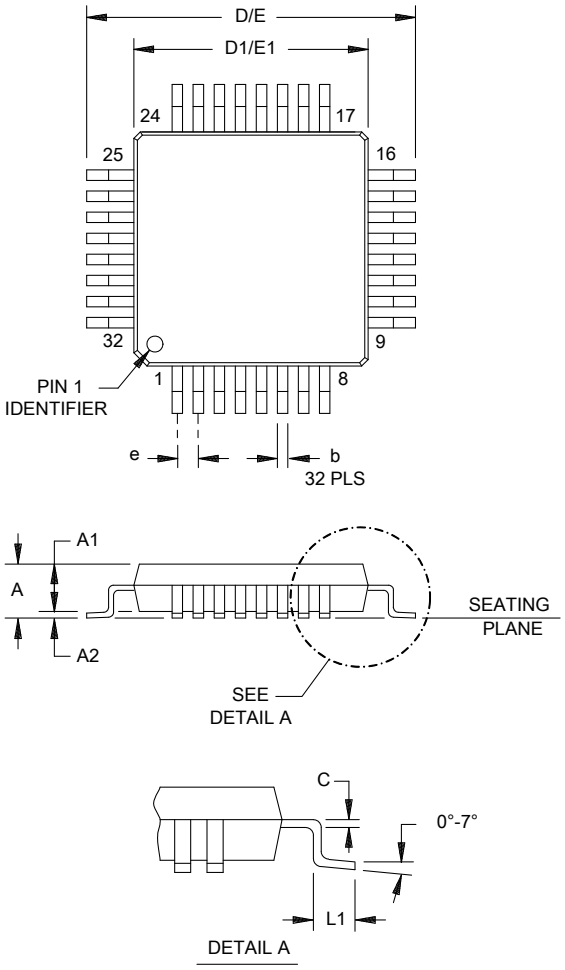
7/ See Figure 6, Figure 7, and Figure 8.

8/ Standalone mode only.

9/ Measured with the load circuit of Figure 5.

10/ Daisy-chain mode only.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	D/E	9.00 BSC SQ	
A1	0.95	1.05	D1/E1	7.00 BSC SQ	
A2	0.05	0.15	e	0.80 BSC	
b	0.30	0.45	L1	0.45	0.75
c	0.09	0.20			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MS-026-AB A.

FIGURE 1. Case outline.

Case outline X							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{\text{SYNC}}$	9	$\overline{\text{RSTOUT}}$	17	AGNDD	25	REFAB
2	SCLK	10	$\overline{\text{RSTIN}}$	18	VOUTD	26	REFCD
3	SDIN	11	DGND	19	VOUTC	27	NC
4	SDO	12	DVCC	20	AGNDC	28	REFGND
5	$\overline{\text{CLR}}$	13	AVDD	21	AGNDB	29	NC
6	$\overline{\text{LDAC}}$	14	PGND	22	VOUTB	30	AVSS
7	D0	15	AVSS	23	VOUTA	31	AVDD
8	D1	16	ISCC	24	AGVDA	32	BIN/$\overline{\text{2sCOMP}}$

FIGURE 2. Terminal connections.

Terminal No.	Mnemonic	Description
1	$\overline{\text{SYNC}}$	Active Low Input. This pin is the frame synchronization signal for the serial interface. While SYNC is low, data is transferred in on the falling edge of SCLK.
2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This input operates at clock speeds up to 30 MHz.
3	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
4	SDO	Serial Data Output. This pin is used to clock data from the serial register in daisy-chain or readback mode.
5	$\overline{\text{CLR}}$	Negative Edge Triggered Input. Asserting this pin sets the data register to 0x0000. This logic input has an internal pull-up device. Therefore, this pin can be left floating and defaults to a Logic 1 condition.
6	$\overline{\text{LDAC}}$	Load DAC. This logic input is used to update the data register and, consequently, the analog outputs. When $\overline{\text{LDAC}}$ is tied permanently low, the addressed data register is updated on the rising edge of $\overline{\text{SYNC}}$. If $\overline{\text{LDAC}}$ is held high during the write cycle, the DAC input shift register is updated, but the update of the output is delayed until the falling edge of $\overline{\text{LDAC}}$. In this mode, all analog outputs can be updated simultaneously on the falling edge of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ pin must not be left unconnected.
7, 8	D0, D1	Digital I/O Port. These pins can be inputs or outputs that are configurable and readable over the serial interface. When configured as inputs, D0 and D1 have weak internal pull-ups to DVCC. When configured as outputs, D0 and D1 are referenced by DVCC and DGND.
9	$\overline{\text{RSTOUT}}$	Reset Logic Output. This pin is the output from the on-chip voltage monitor and is used in the reset circuit. If desired, this pin can be used to control other system components.
10	$\overline{\text{RSTIN}}$	Reset Logic Input. This input allows external access to the internal reset logic. Applying a Logic 0 to this input clamps the DAC outputs to 0 V. In normal operation, $\overline{\text{RSTIN}}$should be tied to Logic 1. Register values remain unchanged.
11	DGND	Digital Ground.
12	DVCC	Digital Supply Voltage (2.7 V to 5.25 V).
13, 31	AVDD	Positive Analog Supply Voltage (11.4 V to 16.5 V).
14	PGND	Ground Reference Point for the Analog Circuitry.
15, 30	AVSS	Negative Analog Supply Voltage (−11.4 V to −16.5 V).

FIGURE 3. Terminal function.

Terminal No.	Mnemonic	Description
16	ISCC	Resistor Connection for Pin Programmable Short-Circuit Current. This pin is used with an optional external resistor to AGND to program the short-circuit current of the output amplifiers.
17	AGNDD	Ground Reference Pin for DAC D Output Amplifier.
18	VOUTD	Analog Output Voltage of DAC D. This buffered output has a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
19	VOUTC	Analog Output Voltage of DAC C. This buffered output has a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
20	AGNDC	Ground Reference Pin for DAC C Output Amplifier.
21	AGNDB	Ground Reference Pin for DAC B Output Amplifier.
22	VOUTB	Analog Output Voltage of DAC B. This buffered output has a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
23	VOUTA	Analog Output Voltage of DAC A. This buffered output has a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
24	AGVDA	Ground Reference Pin for DAC A Output Amplifier.
25	REFAB	External Reference Voltage Input for Channel A and Channel B. Reference input range is 1 V to 7 V. This pin programs the full-scale output voltage. V_{REFIN} = 5 V for specified performance.
26	REFCD	External Reference Voltage Input for Channel C and Channel D. Reference input range is 1 V to 7 V. This pin programs the full-scale output voltage. V_{REFIN} = 5 V for specified performance.
27, 29	NC	No Connect.
28	REFGND	Reference Ground Return for the Reference Generator and Buffers.
32	BIN/$\overline{2sCOMP}$	This pin determines the DAC coding. This pin should be hardwired to either DV_{CC} or DGND. When the pin is hardwired to DV_{CC}, the input coding is offset binary. When the pin is hardwired to DGND, the input coding is twos complement.

FIGURE 3. Terminal function - Continued.

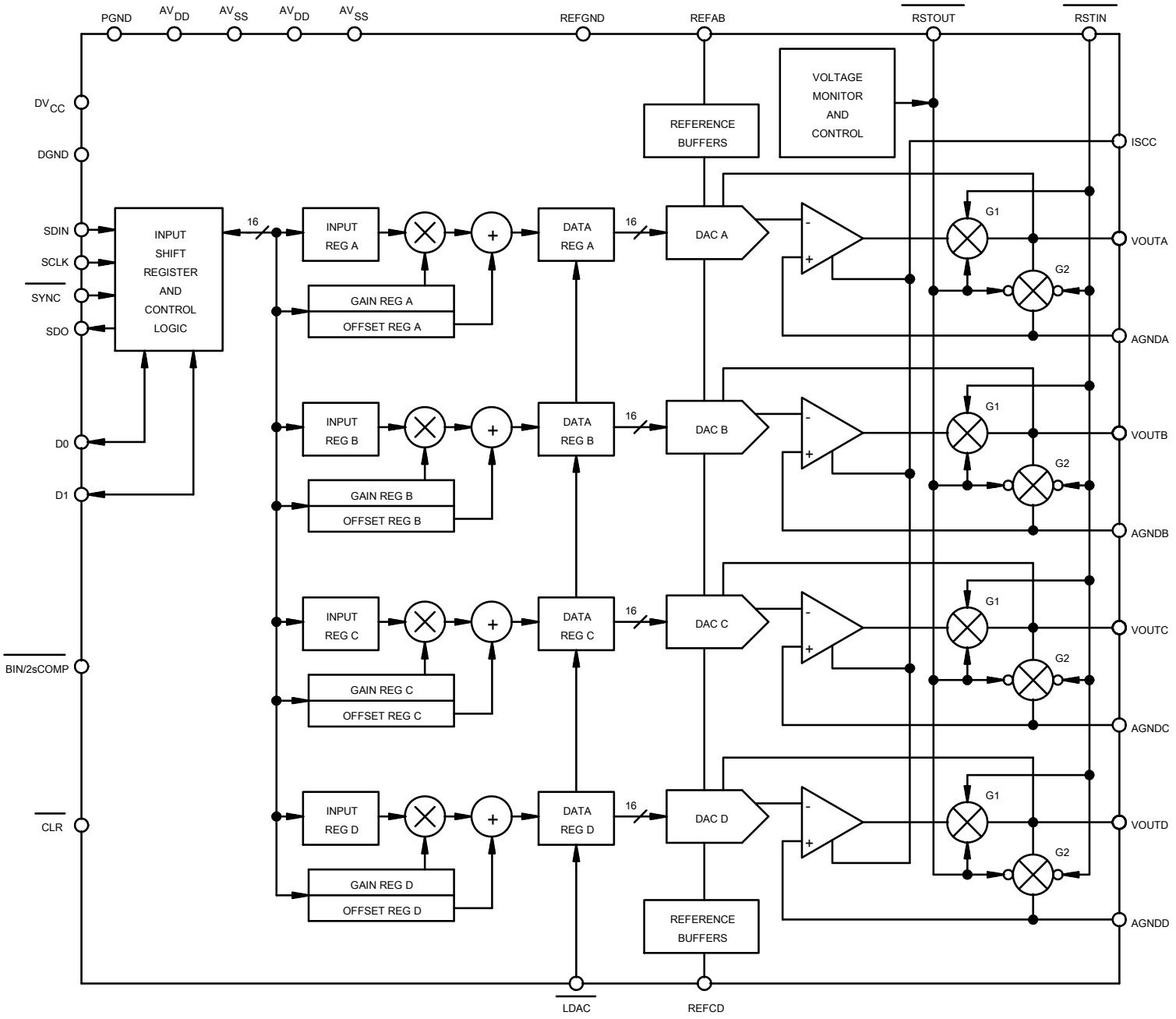


FIGURE 4. Functional block diagram.

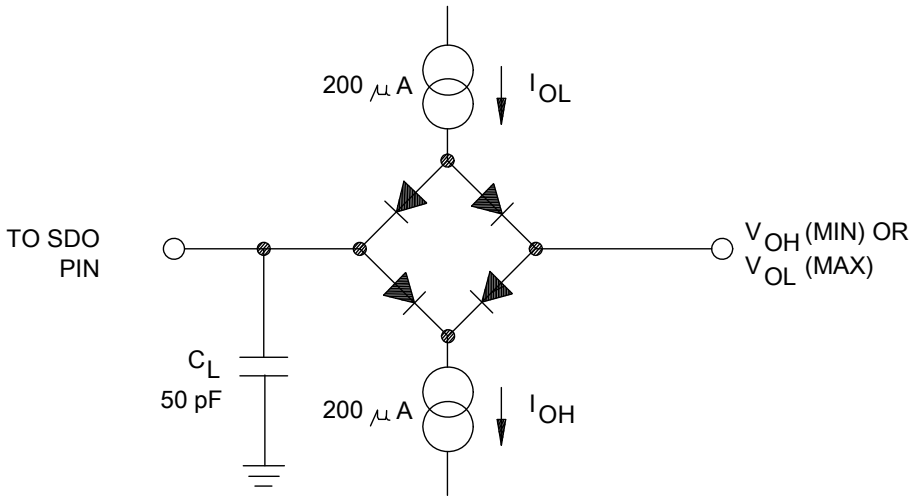


FIGURE 5. Load circuit for SDO timing diagram.

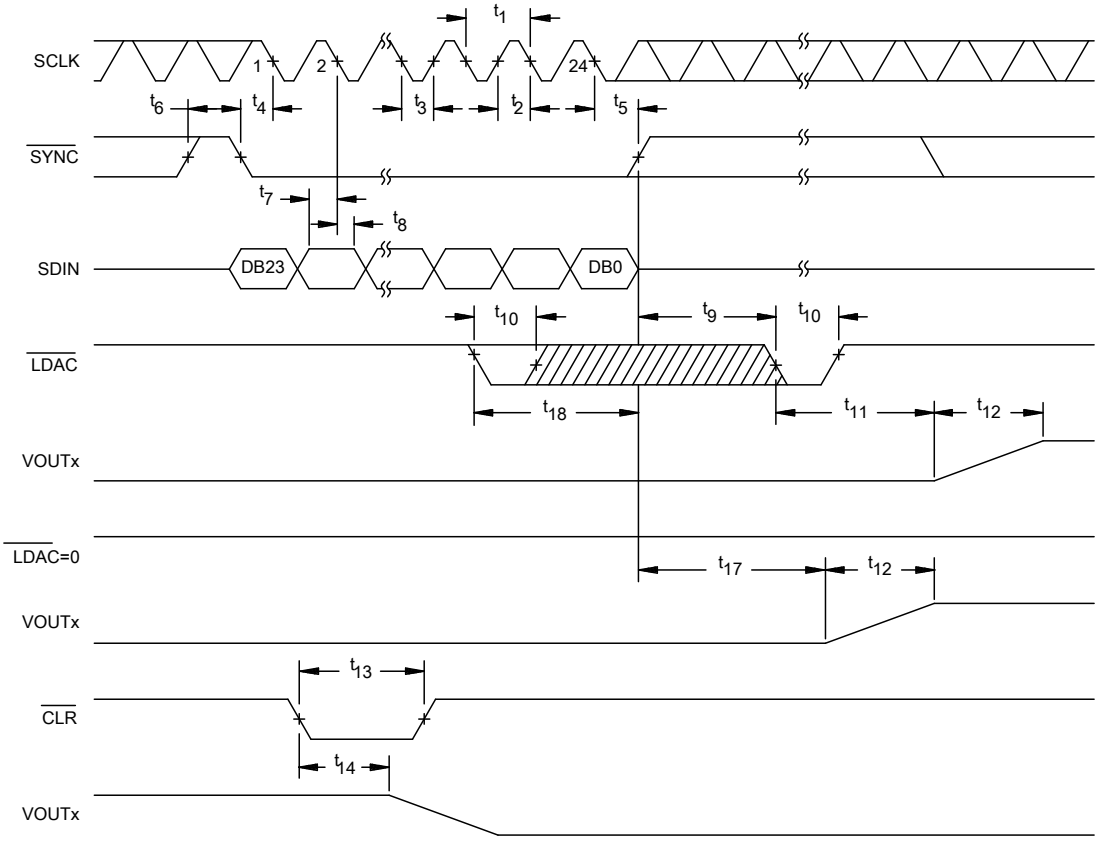


FIGURE 6. Serial interface timing diagram.

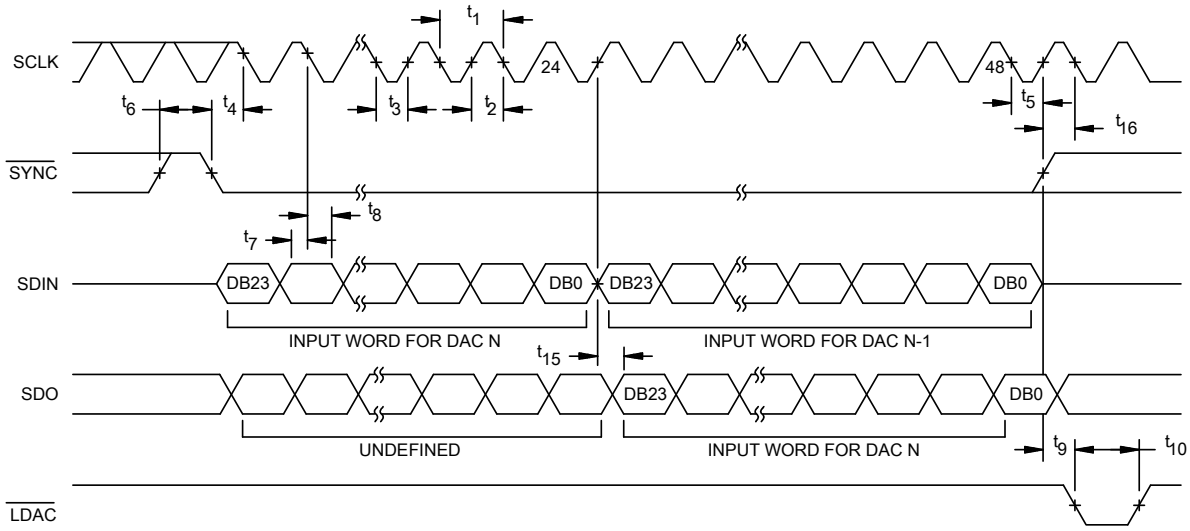


FIGURE 7. Daisy-chain timing diagram.

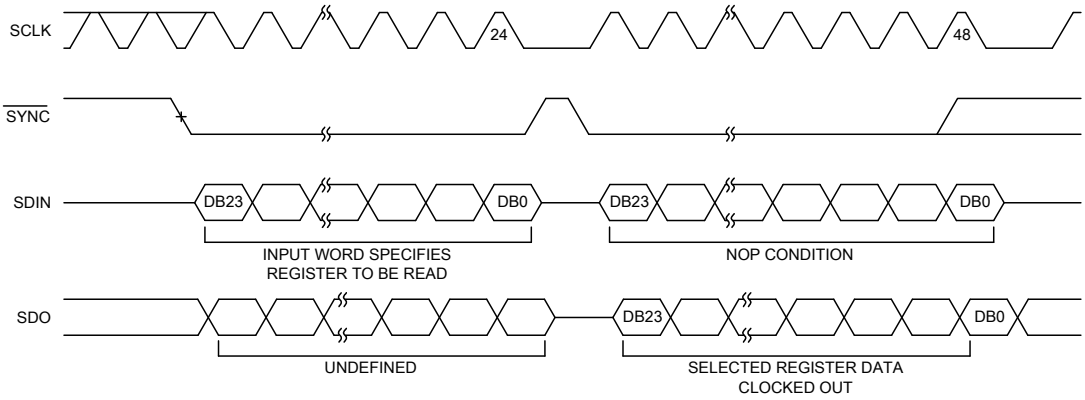


FIGURE 8. Readback timing diagram.

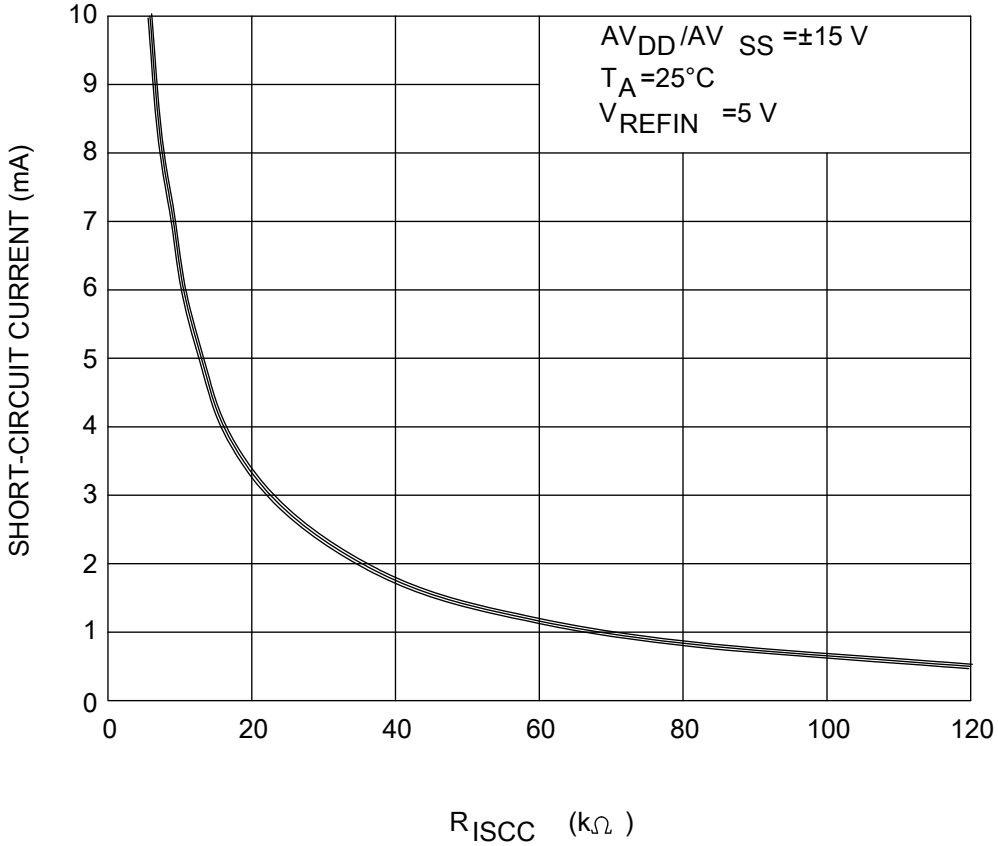


FIGURE 9. Short circuit current vs RISCC.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/14622-01XE	24355	AD5764SSUZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123