REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add lead finish “E” to the devices. - PHN	18-03-08	Thomas M. Hess
B	Delete the Input impedance test under the Analog input section in Table I. Make correction to the JEDEC assignment under Figure 1 by deleting MO-15-AB3 and replacing with MO-220-VKKD-2. Update document paragraphs to current requirements. - ro	23-07-13	James R. Eschmeyer

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B									
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13									

PMIC N/A

Original date of drawing
YY-MM-DD
14-05-06

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TITLE
MICROCIRCUIT, LINEAR, LOW COST, 4-CHANNEL, 16-BIT 1 MSPS PULSAR ADC, MONOLITHIC SILICON

SIZE	CAGE CODE
A	16236

DWG NO. **V62/14620**

REV B

PAGE 1 OF 13

AMSC N/A

5962-V078-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low cost, 4-channel, 16-bit 1 million samples per second (MSPS) PulSAR analog to digital (ADC) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14620	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7655-EP	Low cost, 4-channel, 16-bit 1 MSPS PulSAR ADC

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	JEDEC MO-220- VKKD-2	Lead Frame Chip Scale Package(LFCSP_VQ)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Analog input:
INAx, INBx, REFx, INxN, REFGND ..... AVDD + 0.3 V to AGND – 0.3 V
Ground voltage differences:
AGND, DGND, OGND ..... ±0.3 V
Supply voltages:
AVDD, DVDD, OVDD ..... -0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD ..... ±7 V
DVDD to OVDD ..... -0.3 V to +7 V
Digital inputs ..... -0.3 V to DVDD + 0.3 V
Internal power dissipation ..... 2.5 W 2/
Junction temperature ..... 150°C
Storage temperature range ..... -65°C to 150°C
Lead temperature range (soldering 10 seconds) ..... 300°C

_____

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ Specification is for device in free air: case outline X, θ_{JA} = 26°C/W.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function description. The terminal function description shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Load circuit for digital interface timing. The load circuit for digital interface timing shall be as shown in figure 5.

3.5.6 Voltage reference levels for timings. The voltage reference levels for timings shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{INx} – V_{INxN}$	0		2 V_{REF}	V
Common-Mode Input Voltage	V_{INxN}	-0.1		+0.5	V
Analog Input CMRR	f_{IN} = 100 kHz		55		dB
Input Current	1 MSPS throughput		45		µA
THROUGHPUT SPEED					
Complete Cycle (2 Channels)	Normal mode			2	µs
Throughput Rate	Normal mode	0		1	MSPS
Complete Cycle (2 Channels)	Impulse mode			2.25	µs
Throughput Rate	Impulse mode	0		888	kSPS
DC ACCURACY					
Integral Linearity Error 3/		-6		+6	LSB 4/
No Missing Codes		15			Bits
Transition Noise			0.8		LSB
Full-Scale Error	T_{MIN} to T_{MAX}		±0.25	±0.5	% of FSR
Full-Scale Error Drift			±2		ppm/°C
Unipolar Zero Error	T_{MIN} to T_{MAX}			±0.25	% of FSR
Unipolar Zero Error Drift			±0.8		ppm/°C
Power Supply Sensitivity	AVDD = 5 V ± 5%		±0.8		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 100 kHz		86		dB 5/
Spurious-Free Dynamic Range	f_{IN} = 100 kHz		98		dB
Total Harmonic Distortion	f_{IN} = 100 kHz		-96		dB
Signal-to-Noise and Distortion	f_{IN} = 100 kHz		86		dB
	f_{IN} = 100 kHz, −60 dB input		30		
Channel-to-Channel Isolation	f_{IN} = 100 kHz		-92		dB
−3 dB Input Bandwidth			10		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Delay Matching			30		ps
Aperture Jitter			5		ps rms
Transient Response	Full-scale step			250	ns
REFERENCE					
External Reference Voltage Range		2.3	2.5	AVDD/2	V
External Reference Current Drain	1 MSPS throughput		180		µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
DIGITAL INPUTS						
Logic Levels						
Low level input voltage	V_{IL}		-0.3		+0.8	V
High level input voltage	V_{IH}		+2.0		DVDD + 0.3	V
Low level input current	I_{IL}		-1		+1	µA
High level input current	I_{IH}		-1		+1	µA
DIGITAL OUTPUTS						
Data Format 6/						
Pipeline Delay 7/						
Low level output voltage	V_{OL}	I_{SINK} = 1.6 mA			0.4	V
High level output voltage	V_{OH}	I_{SOURCE} = −500 µA	OVDD – 0.2			V
POWER SUPPLIES						
Specified performance						
Input analog power	AVDD		4.75	5	5.25	V
Digital power	DVDD		4.75	5	5.25	V
Input/output interface digital power	OVDD		2.7		5.25 8/	V
Operating current 9/						
Input analog power	AVDD	1 MSPS throughput		15.5		mA
Digital power	DVDD	1 MSPS throughput		8.5		mA
Input/output interface digital power	OVDD	1 MSPS throughput		100		µA
Power Dissipation		1 MSPS throughput 9/		120	135	mW
		20 kSPS throughput 10/		2.6		
		888 kSPS throughput 10/		114	125	
TEMPERATURE RANGE 11/						
Specified Performance		T_{MIN} to T_{MAX}	-55		+125	°C
TIMING SPECIFICATIONS						
CONVERSION AND RESET						
Convert Pulse Width	t_1		5			ns
Time Between Conversions (Normal Mode/Impulse Mode)	t_2		2/2.25			µs
$\overline{CNVST}$ Low to BUSY High Delay	t_3				32	ns
BUSY High All Modes Except in Master Serial Read After Convert Mode (Normal Mode/Impulse Mode)	t_4				1.75/2	µs
Aperture Delay	t_5			2		ns
End of Conversions to BUSY Low Delay	t_6		10			ns
Conversion Time (Normal Mode/Impulse Mode)	t_7				1.75/2	µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
TIMING SPECIFICATIONS – Continued.						
CONVERSION AND RESET – Continued.						
Acquisition Time	t_8		250			ns
RESET Pulse Width	t_9		10			ns
$\overline{\text{CNVST}}$ Low to $\overline{\text{EOC}}$ high delay	t_{10}				30	ns
$\overline{\text{EOC}}$ high for channel A conversion (Normal Mode/Impulse Mode)	t_{11}				1/1.25	µs
$\overline{\text{EOC}}$ low after Channel A Conversion	t_{12}		45			ns
$\overline{\text{EOC}}$ high for channel A conversion	t_{13}				0.75	µs
Channel Selection Setup Time	t_{14}		250			ns
Channel Selection Hold Time	t_{15}				30	ns
PARALLEL INTERFACE MODES						
$\overline{\text{CNVST}}$ Low to DATA Valid Delay	t_{16}				1.75/2	µs
DATA Valid to BUSY Low Delay	t_{17}		14			ns
Bus Access Request to DATA Valid	t_{18}				40	ns
Bus Relinquish Time	t_{19}		5		15	ns
A/$\overline{\text{B}}$ Low to Data Valid Delay	t_{20}				40	ns
MASTER SERIAL INTERFACE MODES						
$\overline{\text{CS}}$ Low to SYNC Valid Delay	t_{21}				10	ns
$\overline{\text{CS}}$ Low to Internal SCLK Valid Delay 12/	t_{22}				10	ns
$\overline{\text{CS}}$ Low to SDOUT Delay	t_{23}				10	ns
$\overline{\text{CNVST}}$ Low to SYNC Delay, Read During Convert (Normal Mode/Impulse Mode)	t_{24}			250/500		ns
SYNC Asserted to SCLK First Edge Delay	t_{25}		3			ns
Internal SCK Period 13/	t_{26}		23		40	ns
Internal SCLK High 13/	t_{27}		12			ns
Internal SCLK Low 13/	t_{28}		7			ns
SDOUT Valid Setup Time 13/	t_{29}		4			ns
SDOUT Valid Hold Time 13/	t_{30}		2			ns
SCLK Last Edge to SYNC Delay 13/	t_{31}		1			ns
$\overline{\text{CS}}$ High to SYNC High-Z	t_{32}				10	ns
$\overline{\text{CS}}$ High to Internal SCLK High-Z	t_{33}				10	ns
$\overline{\text{CS}}$ High to SDOUT High-Z	t_{34}				10	ns
BUSY High in Master Serial Read after Convert 13/	t_{35}			14/		ns
$\overline{\text{CNVST}}$ Low to SYNC Asserted Delay (Normal Mode/Impulse Mode)	t_{36}			0.75/1		µs
SYNC Deasserted to BUSY Low Delay	t_{37}			25		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
TIMING SPECIFICATIONS – Continued.						
SLAVE SERIAL INTERFACE MODES						
External SCLK Setup Time	t_{38}		5			ns
External SCLK Active Edge to SDOUT Delay	t_{39}		3		18	ns
SDIN Setup Time	t_{40}		5			ns
SDIN Hold Time	t_{41}		5			ns
External SCLK Period	t_{42}		25			ns
External SCLK High	t_{43}		10			ns
External SCLK Low	t_{44}		10			ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V; VREF = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

3/ Linearity is tested using endpoints, not best fit.

4/ LSB means least significant bit. With the 0 V to 5 V input range, 1 LSB is 76.294 µV.

5/ All specifications in dB are referred to as full-scale input, FS. Tested with an input signal at 0.5 dB below full scale unless otherwise specified.

6/ Parallel or serial 16 bit.

7/ Conversion results are available immediately after completed conversion.

8/ The maximum should be the minimum of 5.25 V and DVDD + 0.3 V.

9/ In normal mode; tested in parallel reading mode

10/ In impulse mode; tested in parallel reading mode.

11/ Consult sales for extended temperature range.

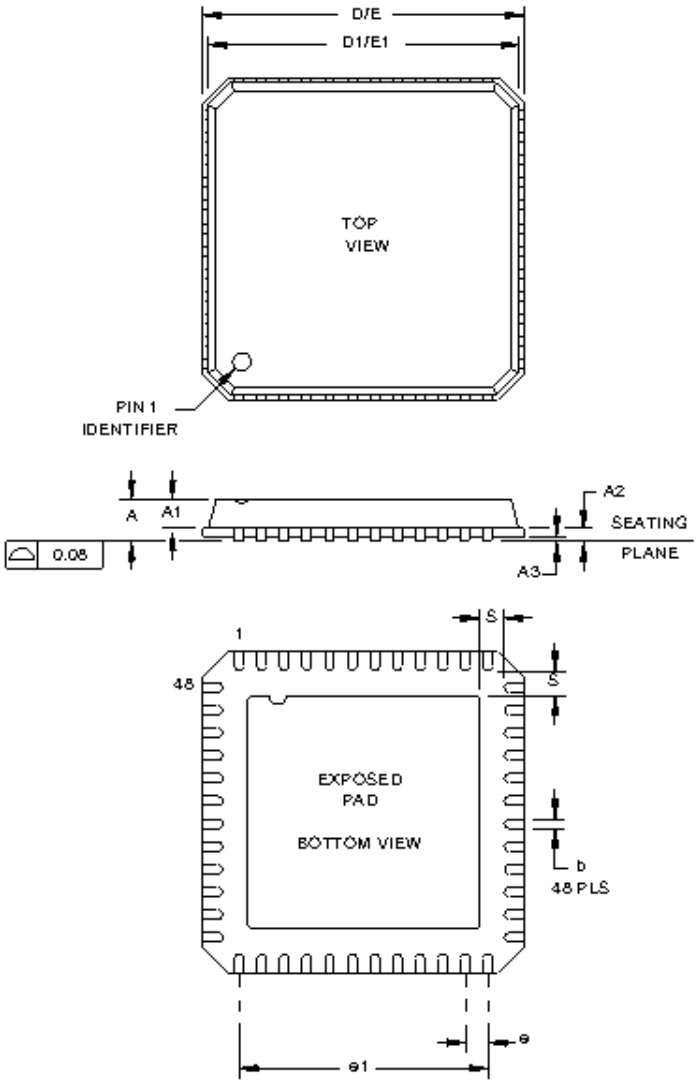
12/ In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise C_L is 60 pF maximum.

13/ In serial master read during convert mode. See 14/ for serial master read after convert mode.

14/ Serial Clock Timings in Master Read After Convert.

DIVSCLK[1]	Symbol	0	0	1	1	Units
DIVSCLK[0]		0	1	0	1	
SYNC to SCLK First Edge Delay Minimum	t_{25}	3	17	17	17	ns
Internal SCLK Period Minimum	t_{26}	25	50	100	200	ns
Internal SCLK Period Typical	t_{26}	40	70	140	280	ns
Internal SCLK High Minimum	t_{27}	12	22	50	100	ns
Internal SCLK Low Minimum	t_{28}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{29}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{30}	2	4	30	80	ns
SCLK Last Edge to SYNC Delay Minimum	t_{31}	1	3	30	80	ns
Busy High Width Maximum (Normal)	t_{35}	3.25	4.25	6.25	10.75	µs
Busy High Width Maximum (Impulse)	t_{35}	3.5	4.5	6.5	11	µs

Case X



Dimen sions					
Symbol	Millimeters		Symbol	Milli meters	
	Min	Max		Min	Max
A	0.80	1.00	D/E	7.00 BSC	
A1		0.80	D1/E1	6.75 BSC	
A2	0.20 REF		e	0.50 BSC	
A3		0.05	e1	5.50 REF	
b	0.18	0.30	S	0.25	

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-220-VKKD-2.

FIGURE 1. Case outline.

Case outline X							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AGND	13	D4/EXT/$\overline{\text{INT}}$	25	D12	37	REF
2	AVDD	14	D5/INVSYNC	26	D13	38	REFGND
3	A0	15	D6/INVSCLK	27	D14	39	INB1
4	BYTESWAP	16	D7/RDC/SDIN	28	D15	40	INBN
5	A/$\overline{\text{B}}$	17	OGND	29	BUSY	41	INB2
6	DGND	18	OVDD	30	$\overline{\text{EOC}}$	42	REFB
7	IMPULSE	19	DVDD	31	$\overline{\text{RD}}$	43	REFA
8	SER/$\overline{\text{PAR}}$	20	DGND	32	$\overline{\text{CS}}$	44	INA2
9	D0	21	D8/SDOUT	33	RESET	45	INAN
10	D1	22	D9/SCLK	34	PD	46	INA1
11	D2/DIVSCLK[0]	23	D10/SYNC	35	$\overline{\text{CNVST}}$	47	AGND
12	D3/DIVSCLK[1]	24	D11/RDERROR	36	DVDD	48	AGND

FIGURE 2. Terminal connections.

Pin No.	Mnemonic	Type 1/	Description
1, 47, 48	AGND	P	Analog Power Ground Pin.
2	AVDD	P	Input Analog Power Pin. Nominally 5 V.
3	A0	DI	Multiplexer Select. When LOW, the analog inputs INA1 and INB1 are sampled simultaneously, then converted. When HIGH, the analog inputs INA2 and INB2 are sampled simultaneously, then converted.
4	BYTESWAP	DI	Parallel Mode Selection (8 Bit, 16 Bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	A/$\overline{\text{B}}$	DI	Data Channel Selection. In parallel mode, when LOW, the data from Channel B is read. When HIGH, the data from Channel A is read. In serial mode, when HIGH, Channel A is output first followed by Channel B. When LOW, Channel B is output first followed by Channel A.
6, 20	DGND	P	Digital Power Ground
7	IMPULSE	DI	Mode Selection. When HIGH, this input selects a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
8	SER/$\overline{\text{PAR}}$	DI	Serial/Parallel Selection Input. When LOW, the parallel port is selected; when HIGH, the serial interface mode is selected and some bits of the DATA bus are used as a serial port.
9, 10	D[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, these outputs are in high impedance.
11, 12	D[2:3] or DIVSCLK[0:1]	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, these outputs are used as Bit 2 and Bit 3 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, EXT/$\overline{\text{INT}}$ is LOW, and RDC/SDIN is LOW, which is the serial master read after convert mode. These inputs, part of the serial port, are used to slow down the internal serial clock that clocks the data output. In the other serial modes, these inputs are not used.

FIGURE 3. Terminal function description.

Pin No.	Mnemonic	Type 1/	Description
13	D[4] or EXT/$\overline{\text{INT}}$	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 4 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock called, respectively, master and slave mode. With EXT/$\overline{\text{INT}}$ tied LOW, the internal clock is selected on SCLK output. With EXT/$\overline{\text{INT}}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D[5] or INVSYNC	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 5 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used to select the active state of the SYNC signal in Master modes. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW
15	D[6] or INVSCLK	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 6 of the parallel port data output bus. When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave modes
16	D[7] or RDC/SDIN	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 7 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input, depending on the state of EXT/$\overline{\text{INT}}$. When EXT/$\overline{\text{INT}}$ is HIGH, RDC/SDIN can be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 32 SCLK periods after the initiation of the read sequence. When EXT/$\overline{\text{INT}}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the previous data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (5 V or 3 V).
19, 36	DVDD	P	Digital Power. Nominally at 5 V.
21	D[8] or SDOUT	DO	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 8 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in a 32-bit on-chip register. The device provides the two conversion results, MSB first, from its internal shift register. The order of channel outputs is controlled by A/$\overline{\text{B}}$. In serial mode, when EXT/$\overline{\text{INT}}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode, when EXT/$\overline{\text{INT}}$ is HIGH: If INVSCLK is LOW, SDOUT is updated on the SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on the SCLK falling edge and valid on the next rising edge.
22	D[9] or SCLK	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 9 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this pin, part of the serial port, is used as a serial data clock input or output, depends upon the logic state of the EXT/$\overline{\text{INT}}$ pin. The active edge where the data SDOUT is updated depends on the logic state of the INVSCLK pin.

FIGURE 3. Terminal function description - Continued.

Pin No.	Mnemonic	Type 1/	Description
23	D[10] or SYNC	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 10 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{INT}$ = Logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and frames SDOUT. After the first channel is output, SYNC is pulsed LOW. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid. After the first channel is output, SYNC is pulsed HIGH.
24	D[11] or RDERROR	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 11 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH and EXT/$\overline{INT}$ is HIGH, this output, part of the serial port, is used as an incomplete read error flag. In slave mode, when a data read is started but not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed HIGH.
25 to 28	D[12:15	DO	Bit 12 to Bit 15 of the parallel port data output bus. When SER/PAR is HIGH, these outputs are in high impedance.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started and remains HIGH until the two conversions are complete and the data is latched into the on-chip shift register. The falling edge of BUSY can be used as a data ready clock signal.
30	$\overline{EOC}$	DO	End of Convert Output. Goes LOW at each channel conversion.
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external serial clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the device. Current conversion, if any, is aborted. If not used, this pin could be tied to DGND
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current conversion is completed.
35	$\overline{CNVST}$	DI	Start Conversion. A falling edge on $\overline{CNVST}$ puts the internal sample-and-hold into the hold state and initiates a conversion. In impulse mode (IMPULSE = HIGH), if $\overline{CNVST}$ is held LOW when the acquisition phase (t8) is complete, the internal sample-and-hold is put into the hold state and a conversion is immediately started
37	REF	AI	This input pin is used to provide a reference to the converter.
38	REFGND	AI	Reference Input Analog Ground.
39, 41	INB_1, INB_2	AI	Channel B Analog Inputs.
40, 45	INBN, INAN	AI	Analog Inputs Ground Senses. Allow to sense each channel ground independently.
42, 43	REFB, REFA	AI	These inputs are the references applied to Channel A and Channel B, respectively.
44,46	INA2, INA1	AI	Channel A Analog Inputs.

FIGURE 3. Terminal function description - Continued.

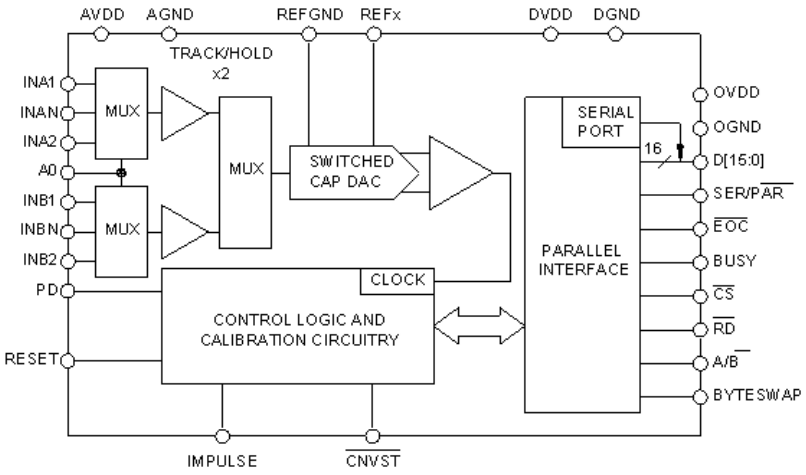
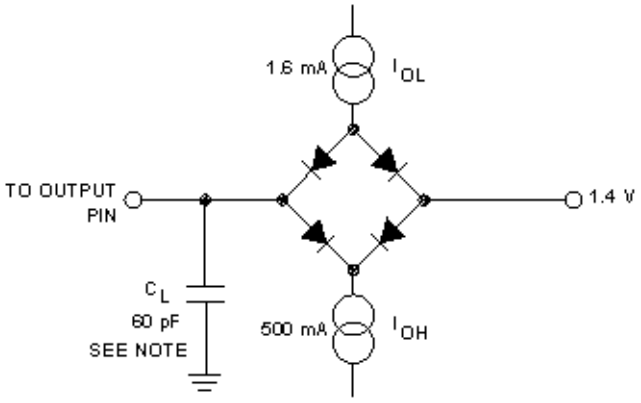


FIGURE 4. Functional block diagram.



NOTES:
1. "In serial interface modes, the SYNC, SCLK and SDOUT timing are defined with a maximum load CL of 10 pF; otherwise, the load is 60 pF maximum.

FIGURE 5. Load circuit for digital interface timing.

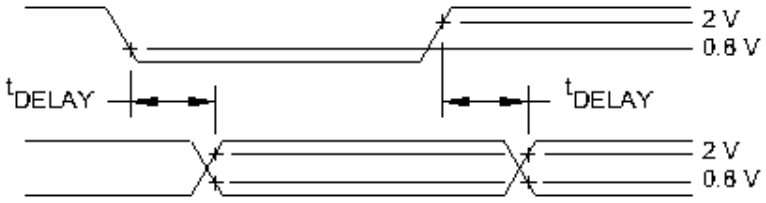


FIGURE 6. Voltage reference levels for timings.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/14620-01XB	24355	AD7655SCP-EP-RL
V62/14620-01XE	24355	AD7655SCPZ-EP-RL

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123