REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 14-05-14	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, LINEAR, LOW POWER, 2.3 V TO 5.5 V, PROGRAMMABLE WAVEFORM GENERATOR, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/14619**
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AMSC N/A

5962-V049-14

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low power, 12.65 mW, 2.3 V to 5.5 V, programmable waveform generator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14619	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD9833-EP	Low power, 12.65 mW, 2.3 V to 5.5 V, programmable waveform generator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	10	MO-187-BA	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Positive power supply voltage (V_{DD}) to analog ground (AGND)	-0.3 V to +6 V
V_{DD} to digital ground (DGND)	-0.3 V to +6 V
AGND to DGND	-0.3 V to +0.3 V
Capacitor (CAP) / 2.5 V	2.75 V
Digital I/O voltage to DGND	-0.3 V to V_{DD} + 0.3 V
Analog I/O voltage to AGND	-0.3 V to V_{DD} + 0.3 V
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum junction temperature (T_J)	+150°C
Lead temperature, soldering (10 seconds)	+300°C
Infrared (IR) reflow, peak temperature	+220°C
Thermal resistance, junction to ambient (θ_{JC})	44°C/W
Thermal resistance, junction to ambient (θ_{JA})	206°C/W

1.4 Recommended operating conditions. 3/

Positive power supply voltage (V_{DD})	2.3 V to 5.5 V
Operating temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Unless otherwise specified, T_A = +25C.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figures 4 and 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Signal digital analog converter (DAC) specifications.							
Resolution			+25°C	01	10 typical		Bits
Update rate			-55°C to +125°C	01		25	MSPS
Output voltage, maximum	V_{OUT}		+25°C	01	0.65 typical		V
Output voltage, minimum	V_{OUT}		+25°C	01	38 typical		mV
V_{OUT} temperature coefficient	V_{OUT}		+25°C	01	200 typical		ppm/°C
DC accuracy: integral nonlinearity			+25°C	01	±1.0 typical		LSB
DC accuracy: differential nonlinearity			+25°C	01	±0.5 typical		LSB
Direct digital synthesis (DDS) specification spurious free dynamic range (SFDR).							
Dynamic specifications: Signal to noise ratio	SNR	f_{MCLK} = 25 MHz, $f_{OUT} = f_{MCLK}/4096$	-55°C to +125°C	01	53.5		dB
			+25°C		60 typical		
Dynamic specifications: Total harmonic distortion	THD	f_{MCLK} = 25 MHz, $f_{OUT} = f_{MCLK}/4096$	-55°C to +125°C	01		-53.5	dBc
			+25°C		-66 typical		
SFDR: Wideband (0 to Nyquist frequency)		f_{MCLK} = 25 MHz, $f_{OUT} = f_{MCLK}/50$	+25°C	01	-60 typical		dBc
SFDR: Narrow band (±200 kHz)		f_{MCLK} = 25 MHz, $f_{OUT} = f_{MCLK}/50$	+25°C	01	-78 typical		dBc
Clock feedthrough			+25°C	01	-60 typical		dBc
Wake up time			+25°C	01	1 typical		ms

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Logic inputs.							
Input high voltage	V_{INH}	2.3 V to 2.7 V power supply	-55°C to +125°C	01	1.7		V
		2.7 V to 3.6 V power supply			2.0		
		4.5 V to 5.5 V power supply			2.8		
Input low voltage	V_{INL}	2.3 V to 2.7 V power supply	-55°C to +125°C	01		0.5	V
		2.7 V to 3.6 V power supply				0.7	
		4.5 V to 5.5 V power supply				0.8	
Input current	I_{INH}/ I_{INL}		-55°C to +125°C	01		10	µA
Input capacitance	C_{IN}		+25°C	01	3 typical		pF
Power supplies.		f_{MCLK} = 25 MHz, $f_{OUT} = f_{MCLK}/4096$					
Positive power supply voltage	V_{DD}		-55°C to +125°C	01	2.3	5.5	V
Positive power supply current	I_{DD}	I_{DD} code dependent, see figure 3	-55°C to +125°C	01		5.5	mA
			+25°C		4.5 typical		
Low power sleep mode		DAC powered down, MCLK running	+25°C	01	0.5 typical		mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristics. 3/ See figures 4 and 5.							
MCLK period	t_1		-55°C to +125°C	01	40		ns
MCLK high duration	t_2		-55°C to +125°C	01	16		ns
MCLK low duration	t_3		-55°C to +125°C	01	16		ns
SCLK period	t_4		-55°C to +125°C	01	25		ns
SCLK high duration	t_5		-55°C to +125°C	01	10		ns
SCLK low duration	t_6		-55°C to +125°C	01	10		ns
FSYNC to SCLK falling edge setup time	t_7		-55°C to +125°C	01	5		ns
FSYNC to SCLK hold time	$t_{8\ min}$		-55°C to +125°C	01	10		ns
	$t_{8\ max}$					t_4 - 5	
Data setup time	t_9		-55°C to +125°C	01	5		ns
Data hold time	t_{10}		-55°C to +125°C	01	3		ns
SCLK high to FSYNC falling edge setup time	t_{11}		-55°C to +125°C	01	5		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = 2.3 V to 5.5 V, AGND = DGND = 0 V, T_A = -55°C to +125°C, typical specifications are at +25°C, R_{SET} = 6.8 kΩ for V_{OUT}.

3/ Guaranteed by design, not production tested.

Case X

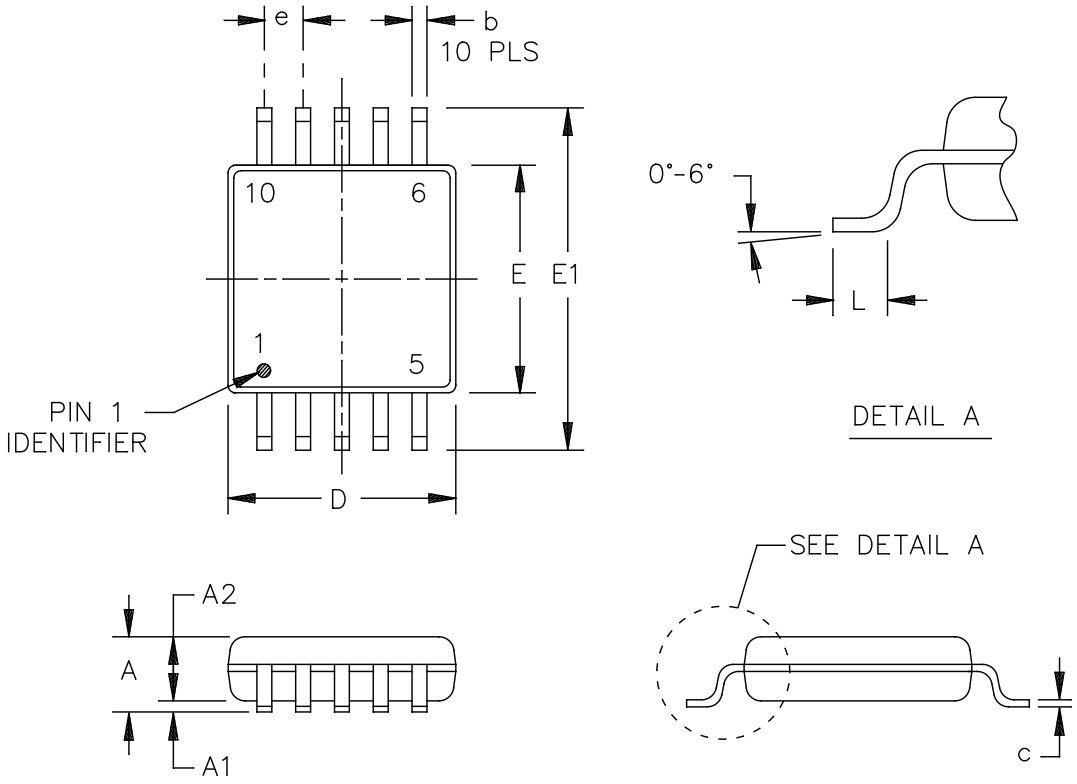

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14619
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Symbol	Dimensions					
	Inches			Millimeters		
	Min	Med	Max	Min	Med	Max
A	---	---	0.043	---	---	1.10
A1	0.0019	---	0.0059	0.05	---	0.15
A2	0.029	0.033	0.037	0.75	0.85	0.95
b	0.0059	---	0.012	0.15	---	0.33
c	0.0051	---	0.009	0.13	---	0.23
D	0.114	0.118	0.122	2.90	3.00	3.10
E	0.114	0.118	0.122	2.90	3.00	3.10
E1	0.183	0.192	0.202	4.65	4.90	5.15
e	0.019 BSC			0.050 BSC		
L	0.015	0.021	0.027	0.40	0.55	0.70

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-187-BA.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	COMP	DAC bias pin. This pin is used for decoupling the DAC bias voltage.
2	V_{DD}	Positive power supply for the analog and digital interface sections. The on board 2.5 V regulator is also supplied from V_{DD}. V_{DD} can have a value from 2.3 V to 5.5 V. A 0.1 μF and a 10 μF decoupling capacitor should be connected between V_{DD} and AGND.
3	CAP/2.5 V	The digital circuitry operates from a 2.5 V power supply. This 2.5 V is generated from V_{DD} using an on board regulator when V_{DD} exceeds 2.7 V. The regulator requires a decoupling capacitor of 100 nF typical, which is connected from CAP/2.5 V to DGND. If V_{DD} is less than or equal to 2.7 V, CAP/2.5 V should be tied directly to V_{DD}.
4	DGND	Digital ground.
5	MCLK	Digital clock input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. The output frequency accuracy and phase noise are determined by this clock.
6	SDATA	Serial data input. The 16 bit serial data word is applied to this input.
7	SCLK	Serial clock input. Data is clocked into the device on each falling edge of SCLK.
8	FSYNC	Active low control input. FSYNC is the frame synchronization signal for the input data. When FSYNC is taken low, the internal logic is informed that a new word is being loaded into the device.
9	AGND	Analog ground.
10	V_{OUT}	Voltage output. The analog and digital output from the device is available at this pin. An external load resistor is not required because the device has a 200 Ω resistor on board.

FIGURE 2. Terminal connections.

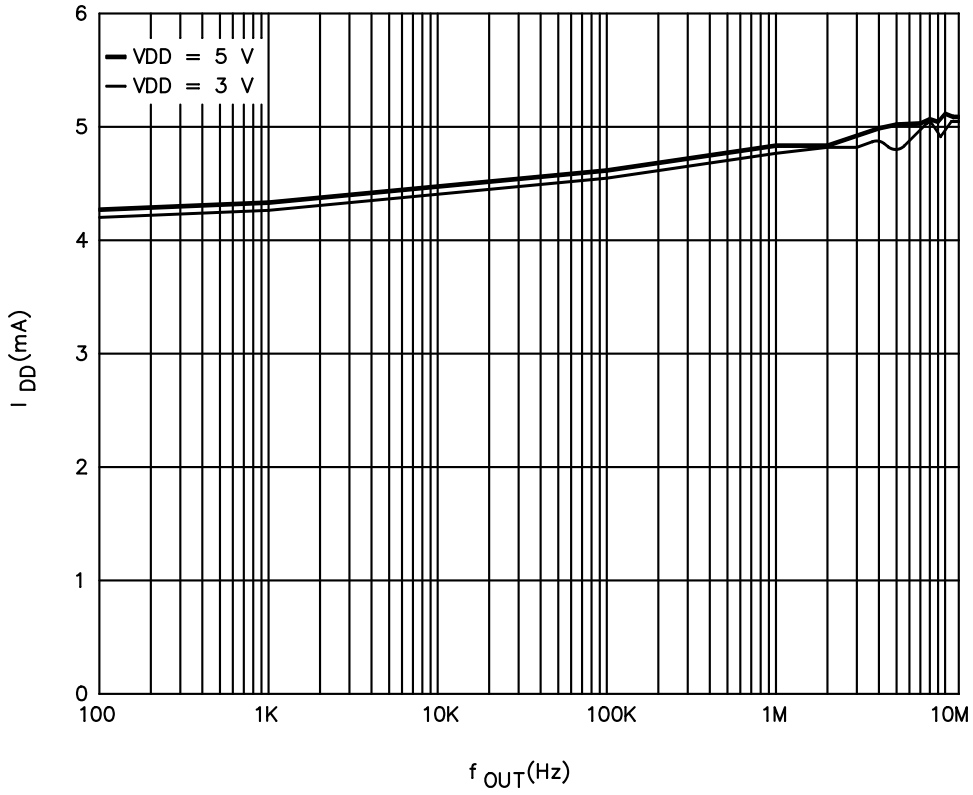

FIGURE 3. Typical I_{DD} versus f_{OUT} for f_{MCLK} = 25 MHz.

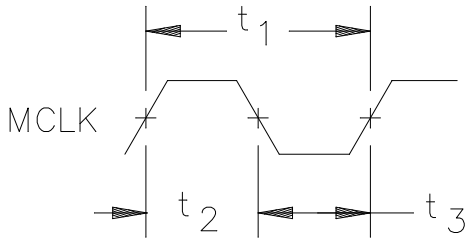

FIGURE 4. Master clock waveform.

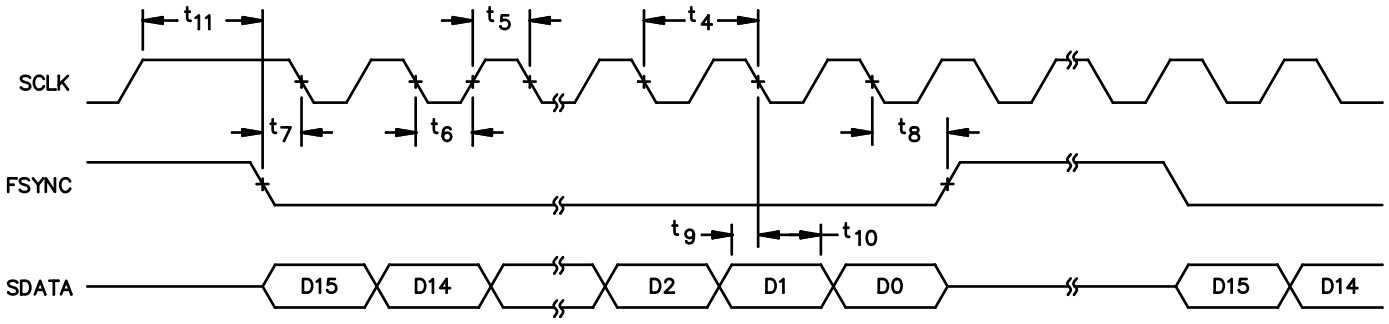

FIGURE 5. Serial timing waveform.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/14619-01XE	24355	DMR	AD9833SRMZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland