REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Make change to BOOT voltage limit from 73 V to 75 V under paragraph 1.3. Add paragraph 1.4 Recommended operating conditions. Add three footnotes under section 1. Delete and add JEDEC references under section 2. Add Top side marking column to paragraph 6.3. Update document paragraphs to current requirements. - ro	21-05-18	James R. Eschmeyer

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			A	A	A	A	A	A	A	A	A	A	A								
	PAGE			1	2	3	4	5	6	7	8	9	10	11								

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 14-07-10	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	TITLE MICROCIRCUIT, LINEAR, 0.5 A, 60 V STEP DOWN DC/DC CONVERTER WITH ECO-MODE, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/14617**
	REV **A**	**PAGE** 1 **OF** 11

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AMSC N/A

5962-V024-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 0.5 A, 60 V step down DC/DC converter with ECO-Mode microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14617	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS54060 -EP	0.5 A, 60 V step down DC/DC converter with ECO-Mode

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	10	MO-187-BA-T	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage:	
VIN	-0.3 V to 65 V
EN	-0.3 V to 5 V
BOOT	75 V
VSENSE	-0.3 V to 3 V
COMP	-0.3 V to 3 V
PWRGD	-0.3 V to 6 V
SS/TR	-0.3 V to 3 V
RT/CLK	-0.3 V to 3.6 V
Output voltage:	
BOOT-PH	8 V
PH	-0.6 V to 65 V
PH, 10-ns Transient	-2 V to 65 V
Voltage difference, PAD to GND	±200 mV
Source current:	
EN	100 µA
BOOT	100 mA
VSENSE	10 µA
PH	Current limit A
RT/CLK	100 µA
Sink current:	
VIN	Current limit A
COMP	100 µA
PWRGR	10 mA
SS/TR	200 µA
Storage temperature	-65°C to +150°C
Electrostatic discharge (ESD):	
Human body model (HBM) per JEDEC JS-001 all pins	1 kV 2/
Charged device model (CDM) per JESD22-C101 all pins	500 V 3/

1.4 Recommended operating conditions. 4/

Input voltage (VIN)	3.5 V to 60 V
Junction temperature range (T_J)	-55°C to +150°C
Ambient temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

3/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

1.5 Thermal characteristics.

Thermal metric 5/ 6/	Case outline X	Units
Junction to ambient thermal resistance, (θ_{JA})	62.5	°C/W
Junction to ambient thermal resistance, (θ_{JA}) 7/	57	°C/W
Junction to case (top) thermal resistance, (θ_{JCtop})	83	°C/W
Junction to board thermal resistance, (θ_{JB})	28	°C/W
Junction to top characterization parameter, (Ψ_{JT})	1.7	°C/W
Junction to board characterization parameter, (Ψ_{JB})	20.1	°C/W
Junction to case (bottom) thermal resistance, (θ_{JCbot})	21	°C/W

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

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5/ For more information about traditional and new thermal metrics, see manufacturer data.

6/ Power rating at a specific ambient temperature TA should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in application section from the manufacturer data.

7/ Test board conditions:

a) 3 inches x 3 inches, 2 layers, thickness: 0.062 inch
b) 2 oz. copper traces located on the top of the PCB.
c) 2 oz. copper ground plane, bottom layer.
d) 6 thermal vias (13 mils) located under the device package.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Simplified schematic. The simplified schematic shall be as shown in figure 4.

3.5.5 Functional block diagram The functional block diagram shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Supply voltage (VIN PIN)						
Operating input voltage			3.5		60	V
Internal under voltage lockout threshold		No voltage hysteresis, rising and falling		2.5		V
Shutdown supply current		EN = 0 V, 3.5 V ≤ VIN ≤ 60 V		1.3	8	µA
Operating: nonswitching supply current		VSENSE = 0.83 V, VIN = 12 V		116	150	µA
Enable and UVLO (EN PIN)						
Enable threshold voltage		No voltage hysteresis, rising and falling	0.9	1.25	1.6	V
Input current		Enable threshold +50 mV		-3.8		µA
		Enable threshold -50 mV		-0.9		
Hysteresis current				-2.9		µA
Voltage reference						
Voltage reference		T_J = 25°C	0.792	0.8	0.808	V
			0.78	0.8	0.821	
High side MOSFET						
On-resistance		VIN = 3.5 V, BOOT-PH = 3 V		300		mΩ
		VIN = 12 V, BOOT-PH = 6 V		200	465	
Error amplifier						
Input current				50		nA
Error amplifier transconductance (g_M)		-2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		97		µMhos
Error amplifier transconductance (g_M) during slow start		-2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{VSENSE} = 0.4 V		26		µMhos
Error amplifier dc gain		V_{VSENSE} = 0.8 V		10,000		V/V
Error amplifier bandwidth				2700		kHz
Error amplifier source/sink		$V_{(COMP)}$ = 1 V, 100 mV overdrive		±7		µA
COMP to switch current transconductance				1.9		A/V
Current limit						
Current limit threshold		VIN = 12 V	0.5	0.94		A

See footnote at end of table.

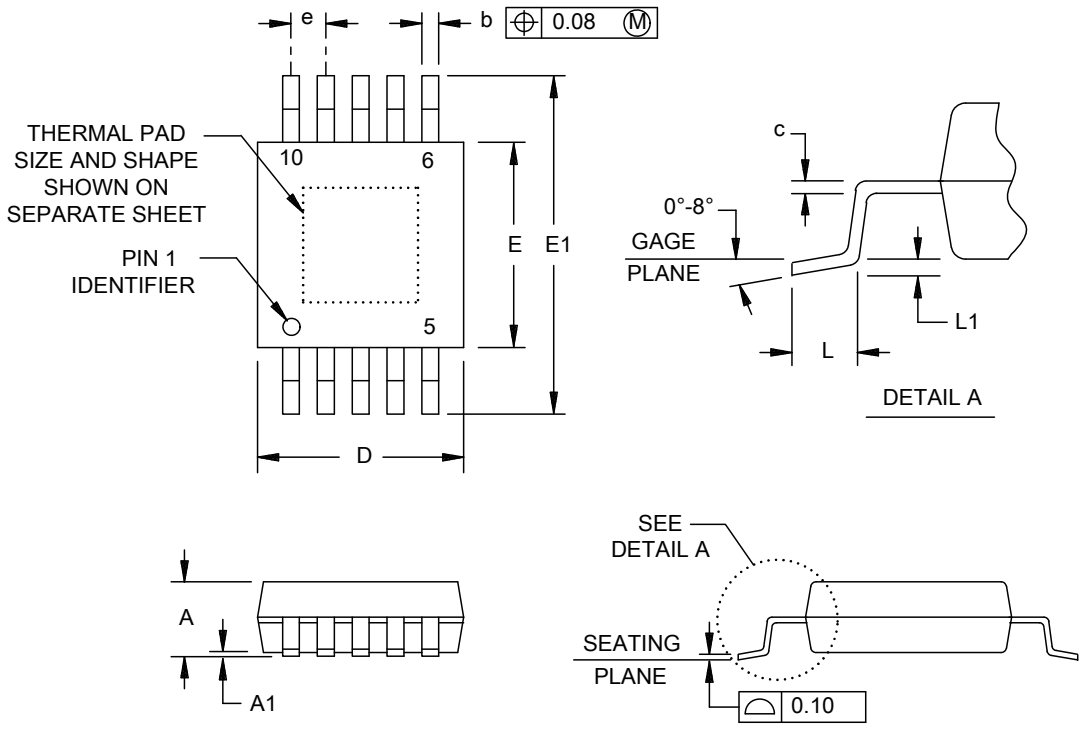
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Thermal Shutdown						
Thermal shutdown				182		°C
Timing resistor and external clock (RT/CLK PIN)						
Switch frequency range using RT mode		$V_{(VIN)}$ = 12 V	130		2500	kHz
Switching frequency	f_{SW}	$V_{(VIN)}$ = 12 V, R_T = 200 kΩ	440	581	740	kHz
Switch frequency range using CLK mode		$V_{(VIN)}$ = 12 V	300		2200	kHz
Minimum CLK input pulse width				40		ns
RT/CLK high threshold		$V_{(VIN)}$ = 12 V		1.9	2.2	V
RT/CLK low threshold		$V_{(VIN)}$ = 12 V	0.5	0.7		V
RT/CLK falling edge to PH rising edge delay		Measured at 500 kHz with resistor in series		60		ns
PLL lock in time		Measured at 500 kHz		100		µs
Slow start and tracking (SS/TR)						
Charge current		$V_{SS/TR}$ = 0.4 V		2		µA
SS/TR to VSENSE matching		$V_{SS/TR}$ = 0.4 V		45		mV
SS/TR to reference crossover		98 % nominal		1.0		V
SS/TR discharge current (overload)		VSENSE = 0 V, V(SS/TR) = 0.4 V		112		µA
SS/TR discharge voltage		VSENSE = 0 V		54		mV
Power good (PWRGD PIN)						
VSENSE threshold	V_{VSENSE}	VSENSE falling (Fault)		92%		
		VSENSE rising (Good)		94%		
		VSENSE rising (Fault)		109%		
		VSENSE falling (Good)		107%		
Hysteresis		VSENSE falling		2%		
Output high leakage		VSENSE = VREF, V(PWRGD) = 5.5 V, 25°C		10		nA
On resistance		I(PWRGD) = 3 mA, VSENSE < 0.79 V		50		Ω
Minimum VIN for defined output		V(PWRGD) < 0.5 V, I(PWRGD) = 100 µA		0.95	1.5	V

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ -55°C ≤ T_J ≤ +150°C, VIN = 3.5 V to 60 V (unless otherwise noted).

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.10	E1	4.75	5.05
A1	0.05	0.15	e	0.50 BSC	
b	0.17	0.27	L	0.40	0.70
c	0.13	0.23	L1	0.25 REF	
D/E	2.90	3.10			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm.
4. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief from manufacturer for information regarding recommended board layout.
5. See the additional figure in the Product data sheet from manufacturer for details regarding the exposed thermal pad features and dimensions.
6. Falls within JEDEC MO-187 variation BA-T.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	BOOT	10	PH
2	VIN	9	GND
3	EN	8	COMP
4	SS/TR	7	VSENSE
5	RT/CLK	6	PWRGD

FIGURE 2. Terminal connections.

Terminal		I/O	Description
Name	No.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
COMP	8	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	3	I	Enable pin, internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
GND	9	-	Ground
PH	10	I	The source of the internal high-side power MOSFET.
PAD	(11)	-	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.
POWRGD	6	O	An open drain output, asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage or EN shut down.
RT/CLK	5	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor set function.
SS/TR	4	I	Slow-start and Tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
VIN	2	I	Input supply voltage, 3.5 V to 60 V.
VSENSE	7	I	Inverting node of the transconductance (gm) error amplifier.

FIGURE 3. Terminal function.

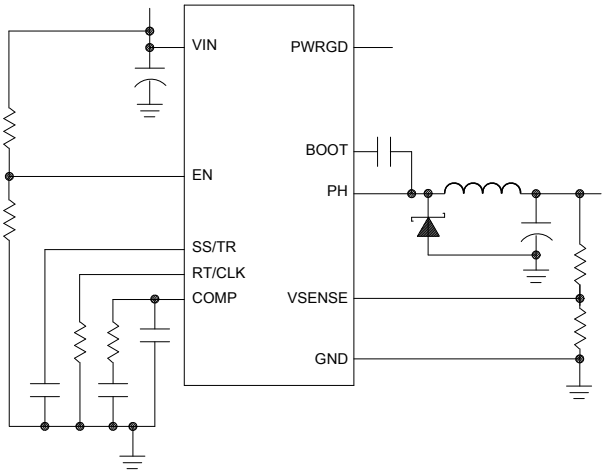


FIGURE 4. Simplified schematic.

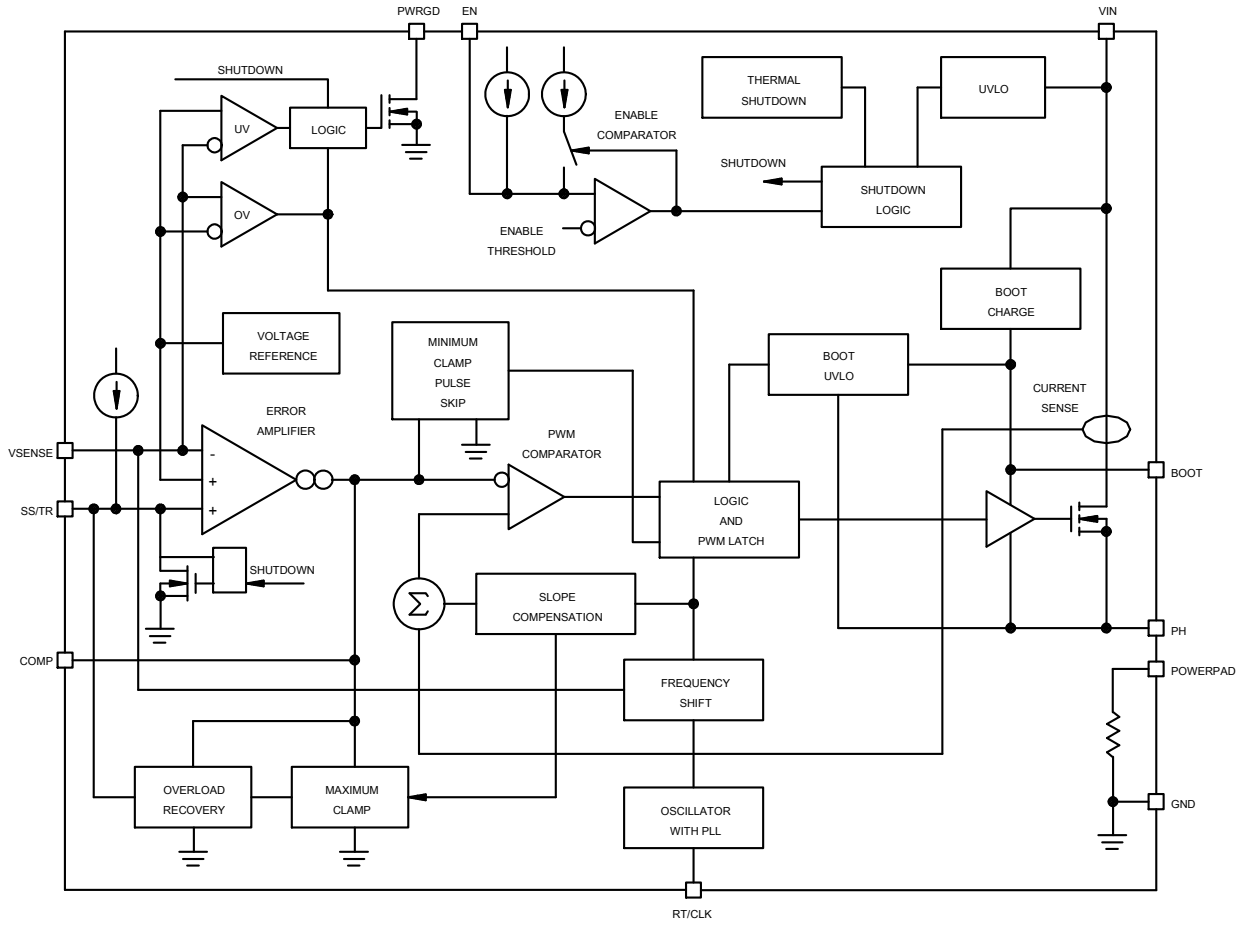


FIGURE 5. Functional block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number 2/
V62/14617-01XE	01295	546M	TPS54060MDGQTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ The case outline X is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54060MDGQTEPR).

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243