



1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 0.5 A, 60 V step down DC/DC converter with ECO-Mode microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/14617</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TPS54060 -EP	0.5 A, 60 V step down DC/DC converter with ECO-Mode

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	10	JEDEC MO-187	Plastic Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Input voltage:	
VIN .....	-0.3 V- to 65 V
EN .....	-0.3 V to 5 V
BOOT .....	73 V
VSENSE .....	-0.3 V to 3 V
COMP .....	-0.3 V to 3 V
PWRGD .....	-0.3 V to 6 V
SS/TR .....	-0.3 V to 3 V
RT/CLK .....	-0.3 V to 3.6 V
Output voltage:	
BOOT-PH .....	8 V
PH .....	-0.6 V to 65 V
PH, 10-ns Transient .....	-2 V to 65 V
Voltage difference, PAD to GND .....	±200 mV
Source current:	
EN .....	100 µA
BOOT .....	100 mA
VSENSE .....	10 µA
PH .....	Current limit A
RT/CLK .....	100 µA
Sink current:	
VIN .....	Current limit A
COMP .....	100 µA
PWRGR .....	10 mA
SS/TR .....	200 µA
Operating junction temperature .....	-55°C to 150°C
Recommended ambient temperature .....	-55°C to 125°C
Storage temperature .....	-65°C to 150°C
Electrostatic discharge:	
(HBM) QSS 009-105 (JESD22-A114A) .....	1 kV
(CDM) QSS 009-147 (JESD22-C101B.01) .....	500 V

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

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1.5 Thermal characteristics.

Thermal metric <u>2/ 3/</u>	Case outline X	Units
Junction to ambient thermal resistance, $\theta_{JA}$	62.5	°C/W
Junction to ambient thermal resistance, $\theta_{JA}$ <u>4/</u>	57	
Junction to top characterization parameter, $\Psi_{JT}$	1.7	
Junction to board characterization parameter, $\Psi_{JB}$	20.1	
Junction to case (top) thermal resistance, $\theta_{JcTop}$	83	
Junction to case (bottom) thermal resistance, $\theta_{JcBot}$	21	
Junction to board thermal resistance, $\theta_{JB}$	28	

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD 22-A114 – Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- JESD22-C101 – Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

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- 2/ For more information about traditional and new thermal metrics, see manufacturer data.
  - 3/ Power rating at a specific ambient temperature  $T_A$  should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in application section from the manufacturer data.
  - 4/ Test board conditions:
    - a) 3 inches x 3 inches, 2 layers, thickness: 0.062 inch
    - b) 2 oz. copper traces located on the top of the PCB.
    - c) 2 oz. copper ground plane, bottom layer.
    - d) 6 thermal vias (13 mils) located under the device package.

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3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Simplified schematic. The simplified schematic shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
<b>Supply voltage (VIN PIN)</b>						
Operating input voltage			3.5		60	V
Internal under voltage lockout threshold		No voltage hysteresis, rising and falling		2.5		V
Shutdown supply current		EN = 0 V, 3.5 V ≤ VIN ≤ 60 V		1.3	8	μA
Operating: nonswitching supply current		VSENSE = 0.83 V, VIN = 12 V		116	150	
<b>Enable and UVLO (EN PIN)</b>						
Enable threshold voltage		No voltage hysteresis, rising and falling	0.9	1.25	1.6	V
Input current		Enable threshold +50 mV		-3.8		μA
		Enable threshold -50 mV		-0.9		
Hysteresis current				-2.9		
<b>Voltage reference</b>						
Voltage reference		T <sub>J</sub> = 25°C	0.792	0.8	0.808	V
			0.78	0.8	0.821	
<b>High side MOSFET</b>						
On-resistance		VIN = 3.5 V, BOOT-PH = 3 V		300		mΩ
		VIN = 12 V, BOOT-PH = 6 V		200	465	
<b>Error amplifier</b>						
Input current				50		nA
Error amplifier transconductance (g <sub>M</sub> )		-2 μA < I <sub>COMP</sub> < 2 μA, V <sub>COMP</sub> = 1 V		97		μMhos
Error amplifier transconductance (g <sub>M</sub> ) during slow start		-2 μA < I <sub>COMP</sub> < 2 μA, V <sub>COMP</sub> = 1 V, V <sub>VSENSE</sub> = 0.4 V		26		
Error amplifier dc gain		V <sub>VSENSE</sub> = 0.8 V		10,000		V/V
Error amplifier bandwidth				2700		kHz
Error amplifier source/sink		V <sub>(COMP)</sub> = 1 V, 100 mV overdrive		±7		μA
COMP to switch current transconductance				1.9		A/V
<b>Current limit</b>						
Current limit threshold		VIN = 12 V	0.5	0.94		A
<b>Thermal Shutdown</b>						
Thermal shutdown				182		°C
<b>Timing resistor and external clock (RT/CLK PIN)</b>						
Switch frequency range using RT mode		V <sub>(VIN)</sub> = 12 V	130		2500	kHz
Switching frequency	f <sub>SW</sub>	V <sub>(VIN)</sub> = 12 V, R <sub>T</sub> = 200 kΩ	440	581	740	kHz
Switch frequency range using CLK mode		V <sub>(VIN)</sub> = 12 V	300		2200	kHz
Minimum CLK input pulse width				40		ns
RT/CLK high threshold		V <sub>(VIN)</sub> = 12 V		1.9	2.2	V
RT/CLK low threshold		V <sub>(VIN)</sub> = 12 V	0.5	0.7		V
RT/CLK falling edge to PH rising edge delay		Measured at 500 kHz with resistor in series		60		ns
PLL lock in time		Measured at 500 kHz		100		μs

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

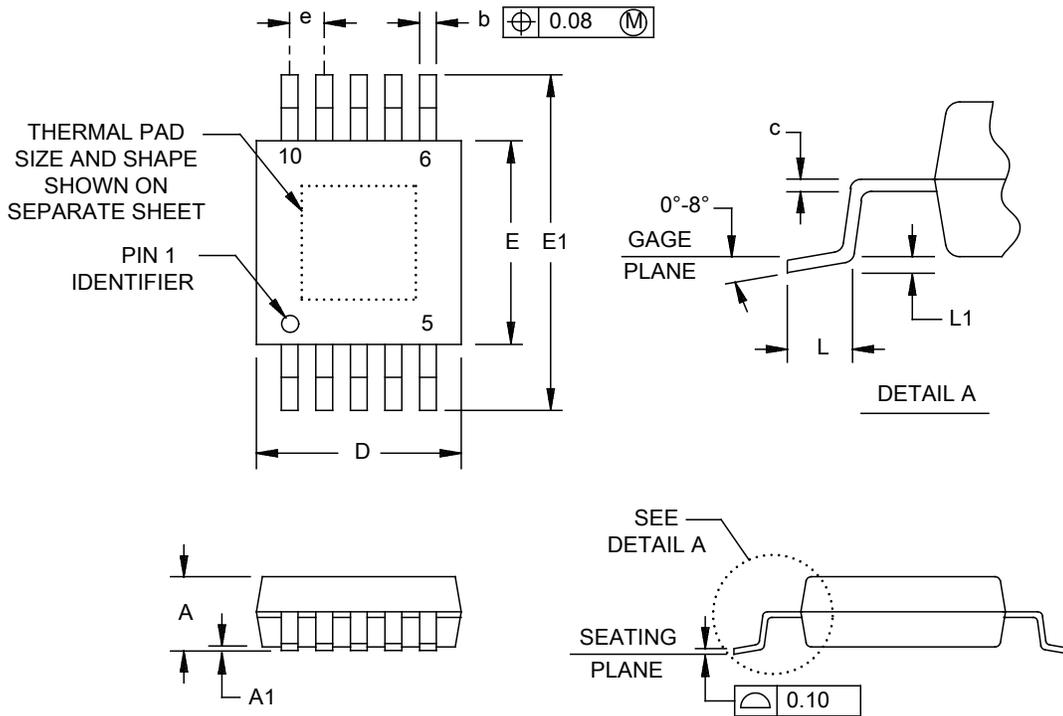
Test	Symbol	Test conditions <u>2/</u>	Limits			Unit
			Min	Typ	Max	
<b>Slow start and tracking (SS/TR)</b>						
Charge current		$V_{SS/TR} = 0.4 \text{ V}$		2		$\mu\text{A}$
SS/TR to VSENSE matching		$V_{SS/TR} = 0.4 \text{ V}$		45		mV
SS/TR to reference crossover		98 % nominal		1.0		V
SS/TR discharge current (overload)		$V_{SENSE} = 0 \text{ V}$ , $V(SS/TR) = 0.4 \text{ V}$		112		$\mu\text{A}$
SS/TR discharge voltage		$V_{SENSE} = 0 \text{ V}$		54		mV
<b>Power good (PWRGD PIN)</b>						
VSENSE threshold	$V_{VSENSE}$	VSENSE falling (Fault)		92%		
		VSENSE rising (Good)		94%		
		VSENSE rising (Fault)		109%		
		VSENSE falling (Good)		107%		
Hysteresis		VSENSE falling		2%		
Output high leakage		$V_{SENSE} = V_{REF}$ , $V(PWRGD) = 5.5 \text{ V}$ , $25^\circ\text{C}$		10		nA
On resistance		$I(PWRGD) = 3 \text{ mA}$ , $V_{SENSE} < 0.79 \text{ V}$		50		$\Omega$
Minimum VIN for defined output		$V(PWRGD) = 0.5 \text{ V}$ , $I(PWRGD) = 100 \mu\text{A}$		0.95	1.5	V

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/  $-55^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$ ,  $V_{IN} = 3.5 \text{ V}$  to  $60 \text{ V}$  (unless otherwise noted).

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.10	E1	4.75	5.05
A1	0.05	0.15	e	0.50 BSC	
b	0.17	0.27	L	0.40	0.70
c	0.13	0.23	L1	0.25 REF	
D/E	2.90	3.10			

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
4. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief from manufacturer for information regarding recommended board layout.
5. See the additional figure in the Product data sheet from manufacturer for details regarding the exposed thermal pad features and dimensions.
6. Falls within JEDEC MO-187 variation BA-T.

FIGURE 1. Case outline.

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Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	BOOT	10	PH
2	VIN	9	GND
3	EN	8	COMP
4	SS/TR	7	VSENSE
5	RT/CLK	6	PWRGD

FIGURE 2. Terminal connections.

Terminal		I/O	Description
Name	No.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
COMP	8	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	3	I	Enable pin, internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
GND	9	-	Ground
PH	10	I	The source of the internal high-side power MOSFET.
POWERPAD	(11)	-	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.
POWRGD	6	O	An open drain output, asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage or EN shut down.
RT/CLK	5	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor set function.
SS/TR	4	I	Slow-start and Tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
VIN	2	I	Input supply voltage, 3.5 V to 60 V.
VSENSE	7	I	Inverting node of the transconductance (gm) error amplifier.

FIGURE 3. Terminal function.

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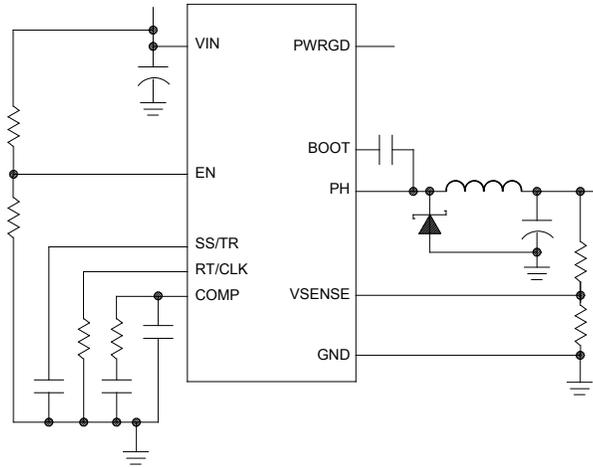


FIGURE 4. Simplified schematic.

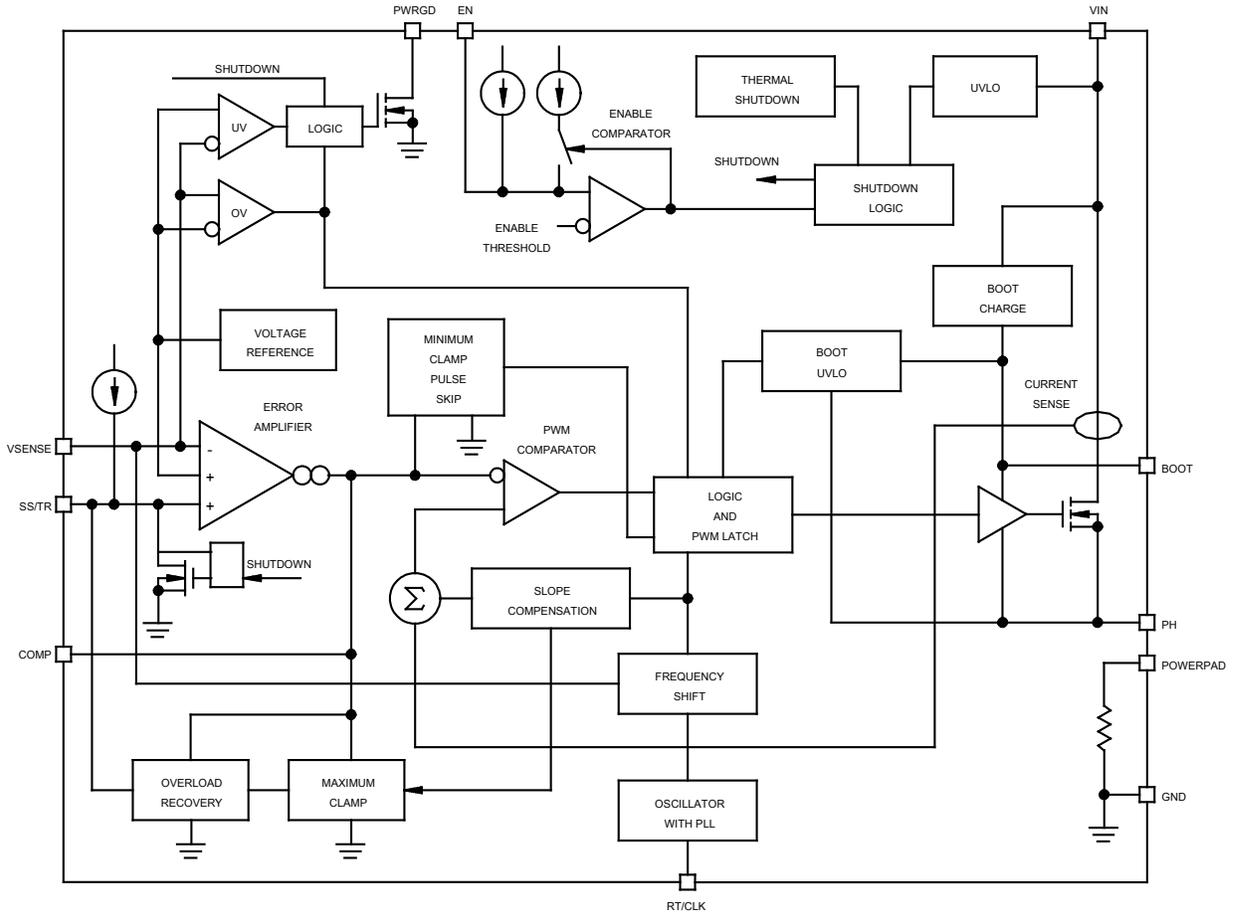


FIGURE 5. Functional block diagram.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number <u>2/</u>
V62/14617-01XE	01295	TPS54060MDGQTEP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ The case outline X is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54060MDGQTEPR).

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

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