REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Make changes to footnotes 4/ and 5/ under paragraph 1.3. Under Figure 2 terminal connections, terminal symbol SYNC description, delete 0.1 MHz and replace with 1.0 MHz. Add Top side marking and Mode of transportation and quantity columns to paragraph 6.3. Update document paragraphs to current requirements. - ro	20-02-12	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			A	A	A	A	A	A	A	A	A	A	A								
	PAGE			1	2	3	4	5	6	7	8	9	10	11								

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 14-08-29	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, 5 AMP 40 VOLT WIDE INPUT RANGE BOOST/SEPIC/FLYBACK DC TO DC REGULATOR, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/14611**
	REV **A**	**PAGE** 1 **OF** 11

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V129-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 5 amp, 40 V wide input range boost / single ended primary inductor converter (SEPIC) / flyback dc to dc regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14611	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS55340	5 amp, 40 V wide input range boost / SEPIC / flyback dc to dc regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-220	Plastic quad leadless flat pack with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltages on pin V_{IN} ..... -0.3 V to 34 V
Voltage on pin EN ..... -0.3 V to 34 V
Voltage on pins FB, FREQ, and COMP ..... -0.3 V to 3 V
Voltage on pin SS ..... -0.3 V to 5 V
Voltage on pin SYNC ..... -0.3 V to 7 V
Voltage on pin SW ..... -0.3 V to 40 V
Operating junction temperature range (T_J) ..... -55°C to +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Electrostatic discharge (ESD): 3/
Human body model (HBM) per JEDEC JS-001, all pins ..... -2000 V and +2000 V 4/
Charge device model (CDM) per JEDEC JESD22-C101, all pins ..... -500 V to +500 V 5/

1.4 Recommended operating conditions. 6/

Input voltage range (V_{IN}) ..... 2.9 V to 32 V
Output voltage range (V_{OUT}) ..... V_{IN} to 38 V
EN voltage range (V_{EN}) ..... 0 V to 32 V
External switching frequency logic input range (V_{SYN}) ..... 0 V to 5 V
Operating free-air temperature range (T_A) ..... -55°C to +125°C
Operating junction temperature range (T_J) ..... -55°C to +150°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	43.3	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	38.7	°C/W
Thermal resistance, junction-to-board	θ_{JB}	14.5	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	0.4	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	14.5	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	3.5	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values are with respect to network ground terminal.
3/ Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
4/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
5/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{IN} = 5 V unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Supply current							
Input voltage range	V_{IN}		-55°C to +150°C	01	2.9	32	V
Operating quiescent current into V_{IN}	I_Q	Device non-switching, V_{FB} = 2 V	+25°C	01	0.5 typical		mA
Shutdown current	I_{SD}	EN = GND	-55°C to +150°C	01		10	µA
			+25°C		2.7 typical		
Under voltage lockout threshold	V_{UVLO}	V_{IN} falling	-55°C to +150°C	01		2.7	V
			+25°C		2.5 typical		
Under voltage lockout hysteresis	V_{hys}		-55°C to +150°C	01	120	160	mV
			+25°C		140 typical		
Enable and reference control.							
EN threshold voltage	V_{EN}	EN rising input	-55°C to +150°C	01	0.9	1.30	V
			+25°C		1.08 typical		
EN threshold hysteresis	V_{ENh}		-55°C to +150°C	01	0.1	0.22	V
			+25°C		0.16 typical		
EN pull down resistor	R_{EN}		-55°C to +150°C	01	400	1600	kΩ
			+25°C		950 typical		
Shutdown delay, SS discharge	t_{off}	EN high to low	+25°C	01	1.0 typical		ms
SYN logic high voltage	V_{SYNh}		-55°C to +150°C	01	1.2		V
SYN logic low voltage	V_{SYNl}		-55°C to +150°C	01		0.4	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{IN} = 5 V unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Voltage and current control.							
Voltage feedback regulation voltage	V_{REF}		-55°C to +150°C	01	1.204	1.254	V
			+25°C		1.229 typical		
Voltage feedback input bias current	I_{FB}		-55°C to +150°C	01		30	nA
					1.6 typical		
COMP pin sink current	I_{sink}	$V_{FB} = V_{REF}$ + 200 mV, V_{COMP} = 1 V	+25°C	01	42 typical		µA
COMP pin source current	I_{source}	$V_{FB} = V_{REF}$ - 200 mV, V_{COMP} = 1 V	+25°C	01	42 typical		µA
COMP pin clamp voltage	V_{CCLP}	High clamp, V_{FB} = 1 V	+25°C	01	3.1 typical		V
		Low clamp, V_{FB} = 1.5 V			0.75 typical		
COMP pin threshold	V_{CTH}	Duty cycle = 0 %	+25°C	01	1.04 typical		V
Error amplifier transconductance	Gea		-55°C to +150°C	01	240	440	µmho
			+25°C		360 typical		
Error amplifier output resistance	Rea		+25°C	01	10 typical		MΩ
Error amplifier crossover frequency	fea		+25°C	01	500 typical		kΩ
Frequency							
Frequency	f_{SW}	R_{FREQ} = 480 kΩ	-55°C to +150°C	01	75	130	kHz
			+25°C		94 typical		
		R_{FREQ} = 80 kΩ	-55°C to +150°C		460	740	
			+25°C		577 typical		
		R_{FREQ} = 40 kΩ	-55°C to +150°C		920	1480	
			+25°C		1140 typical		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{IN} = 5 V unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Frequency – continued.							
Maximum duty cycle	Dmax	V_{FB} = 1.0 V, R_{FREQ} = 80 kΩ	-55°C to +150°C	01	89%		
			+25°C		96% typical		
FREQ pin voltage	V_{FREQ}		+25°C	01	1.25 typical		V
Minimum on pulse width	t_{min_on}	R_{FREQ} = 80 kΩ	+25°C	01	77 typical		ns
Power switch.							
N-channel MOSFET on-resistance	$R_{DS(ON)}$	V_{IN} = 5 V	-55°C to +150°C	01		110	mΩ
			+25°C		60 typical		
		V_{IN} = 3 V	-55°C to +150°C			120	
			+25°C		70 typical		
N-channel leakage current	I_{LN_NFET}	V_{DS} = 25 V	+25°C	01		2.1	μA
OCP and SS							
N-channel MOSFET current limit	I_{LIM}	D = D_{max}	-55°C to +150°C	01	5.25	8.25	A
			+25°C		6.6 typical		
Soft start bias current	I_{SS}	V_{SS} = 0 V	+25°C	01	6 typical		μA
Thermal shutdown.							
Thermal shutdown threshold	$T_{shutdown}$		+25°C	01	165 typical		°C
Thermal shutdown threshold hysteresis	$t_{hysteresis}$		+25°C	01	15 typical		°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X

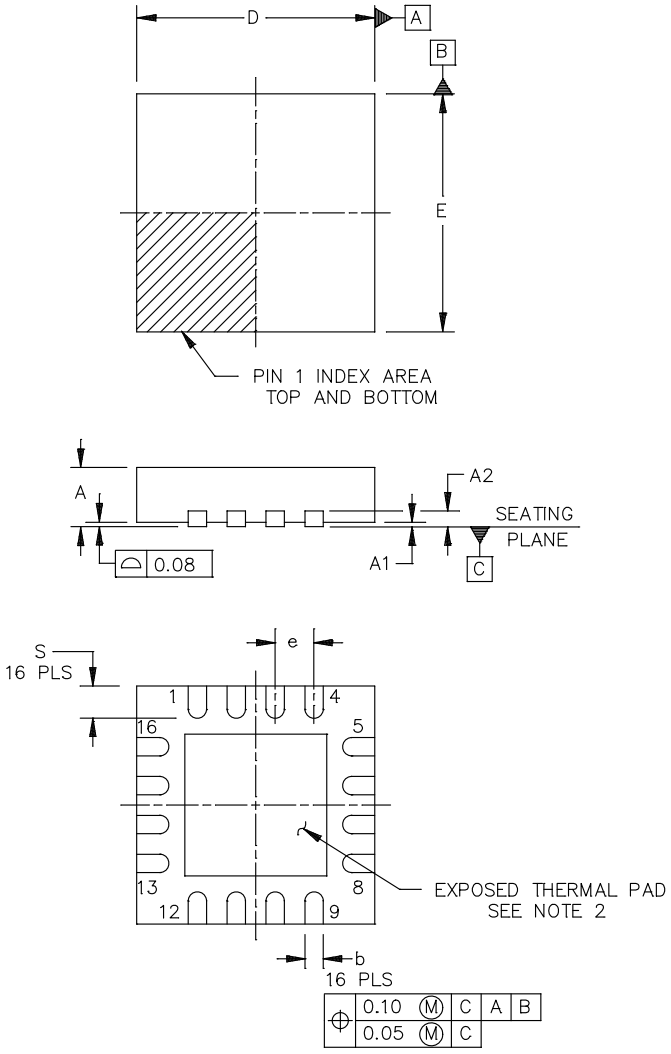

FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.027	0.031	0.70	0.80
A1	0.000	0.001	0.00	0.05
A2	0.0078 REF		0.20 REF	
b	0.0070	0.011	0.18	0.30
D	0.112	0.124	2.85	3.15
E	0.112	0.124	2.85	3.15
e	0.019 BSC		0.50 BSC	
S	0.011	0.019	0.30	0.50

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The package thermal pad must be soldered to the board for thermal and mechanical performance.
3. Falls within reference to JEDEC MO-220.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	SW	SW is the drain of the internal power metal oxide semiconductor field effect transistor (MOSFET). Connect SW to the switched side of the boost or SEPIC inductor or the flyback transformer.
2	VIN	The input supply pin to the integrated circuit (IC). Connect VIN to a supply voltage between 2.9 V to 32 V. It is acceptable for the voltage on the pin to be different from the boost power stage input.
3	EN	Enable pin. When the voltage of this pin falls below the enable threshold for more than 1 ms, the IC turns off.
4	SS	Soft start programming pin. A capacitor between the SS pin and AGND pin programs soft start timing.
5	SYNC	Switching frequency synchronization pin. An external clock signal can be used to set the switching frequency between 200 kHz and 1.0 MHz. If not used, this pin should be tied to AGND.
6	AGND	Signal ground of the IC.
7	COMP	Output of the transconductance error amplifier. An external resistance - capacitance (RC) network connected to this pin compensates the regulator feedback loop.
8	FB	Error amplifier input and feedback pin for positive voltage regulation. Connect to the center tap of a resistor divider to program the output voltage.
9	FREQ	Switching frequency program pin. An external resistor connected between the FREQ pin and AGND sets the switching frequency.
10	NC	Reserved pin that must be connected to ground.
11	PGND	Power ground of the IC. It is connected to the source of the internal power MOSFET switch.
12	PGND	Power ground of the IC. It is connected to the source of the internal power MOSFET switch.
13	PGND	Power ground of the IC. It is connected to the source of the internal power MOSFET switch.
14	NC	Reserved pin that must be connected to ground.
15	SW	SW is the drain of the internal power metal oxide semiconductor field effect transistor (MOSFET). Connect SW to the switched side of the boost or SEPIC inductor or the flyback transformer.
16	SW	SW is the drain of the internal power metal oxide semiconductor field effect transistor (MOSFET). Connect SW to the switched side of the boost or SEPIC inductor or the flyback transformer.
17	Thermal pad	The thermal pad should be soldered to the AGND. If possible, use thermal vias to connect to internal ground plane for improved power dissipation.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/14611-01XE	01295	Tape and reel, 250 units	5340M	TPS55340MRTETEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243