REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Delete figure 5 and all V_S = +3 V tests under Table I. - ro	14-04-03	C. SAFFLE
B	Update JEDEC package from MO-178-AA to MO-178. Add 3 footnotes to ESD section under paragraph 1.3. Add supply voltage limits to paragraph 1.4. Add JEDEC references to paragraph 2. Add sentence to footnote 2/ as specified under Table I. Update the "L" dimension maximum limit as specified under Figure 1. Add terminal descriptions to Figure 2. - ro	20-02-05	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 14-02-25	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, LOW POWER, SINGLE SUPPLY, WIDEBAND OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/14610**
	REV B	**PAGE** 1 **OF** 17

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low power, single supply wideband operational amplifier microcircuit, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14610	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	OPA830-EP	Low power, single supply wideband operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	5	MO-178	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Power supply ..... 12 V dc
Differential input voltage ..... ±2.5 V
Internal power dissipation (P_D) ..... 73 mW
Input voltage range (single supply) ..... -0.5 V to +V_S + 0.3 V
Storage temperature range ..... -65°C to +125°C
Junction temperature range (T_J) ..... +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Electrostatic discharge (ESD): 2/
Human body model (HBM) ..... 2,000 V 3/
Charge device model (CDM) ..... 1,500 V 4/
Machine model (MM) ..... 200 V

1.4 Recommended operating conditions. 5/

Dual supply voltage ..... ±5 V nominal, ±5.5 V maximum
Single supply voltage ..... 5 V nominal, 11 V maximum
Operating junction temperature range (T_J) ..... -40°C to +105°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	218.8	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	87.0	°C/W
Thermal resistance, junction-to-board	θ_{JB}	45.2	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	4.4	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	44.4	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
3/ Level listed above is the passing level per JEDEC JS-001. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
4/ Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250 V HBM allows safe manufacturing with a standard ESD control process.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Test circuits. The test circuits shall be as shown in figures 3 and 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ $V_S = \pm 5$ V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC performance.		See figure 3.					
Small signal bandwidth	SSBW	G = +1, $V_O \leq 0.2$ V_{PP}	+25°C	01	310 typical		MHz
		G = +2, $V_O \leq 0.2$ V_{PP}	-40°C to +85°C		65		
			+25°C		120 typical		
		G = +5, $V_O \leq 0.2$ V_{PP}	-40°C to +85°C		15		
			+25°C		25 typical		
		G = +10, $V_O \leq 0.2$ V_{PP}	-40°C to +85°C		6		
			+25°C		11 typical		
Gain bandwidth product	GBWP	G ≥ +10	-40°C to +85°C	01	80		MHz
			+25°C		110 typical		
Peaking at a gain of +1		$V_O \leq 0.2$ V_{PP}	+25°C	01	6 typical		dB
Slew rate	SR	G = +2, 2 V step	-40°C to +85°C	01	260		V/μs
			+25°C		600 typical		
Rise time	t_R	0.5 V step	-40°C to +85°C	01		5.9	ns
			+25°C		3.3 typical		
Fall time	t_F	0.5 V step	-40°C to +85°C	01		6	ns
			+25°C		3.5 typical		
Settling time to 0.1%	t_S	G = +2, 1 V step	-40°C to +85°C	01		66	ns
			+25°C		42 typical		
Harmonic distortion.		V_O = 2 V_{PP}, f = 5 MHz					
2 nd harmonic		$R_L = 150$ Ω	-40°C to +85°C	01		-56	dBc
			+25°C		-67 typical		
		$R_L \geq 500$ Ω	-40°C to +85°C			-60	
			+25°C		-71 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.1/

Test	Symbol	Conditions 2/ $V_S = \pm 5$ V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC performance – continued.		See figure 3.					
Harmonic distortion – continued.		V_O = 2 V_{PP}, f = 5 MHz					
3 rd harmonic		R_L = 150 Ω	-40°C to +85°C	01		-48	dBc
			+25°C		-60 typical		
		$R_L \geq$ 500 Ω	-40°C to +85°C			-59	
			+25°C		-77 typical		
Input voltage noise		f > 1 MHz	-40°C to +85°C	01		11.5	nV / $\sqrt{Hz}$
			+25°C		9.5 typical		
Input current noise		f > 1 MHz	-40°C to +85°C	01		5.7	pA / $\sqrt{Hz}$
			+25°C		3.7 typical		
NTSC differential gain			+25°C		0.07 typical		%
NTSC differential phase			+25°C		0.17 typical		°
DC performance.		R_L = 150 Ω3/					
Open loop voltage gain	A_{VOL}		-40°C to +105°C	01	64		dB
			+25°C		74 typical		
Input offset voltage	V_{IO}		-40°C to +105°C	01		±8.6	mV
			+25°C		±1.5 typical		
Average offset voltage drift	ΔV_{IO}		+25°C	01		±35	µV / °C
Input bias current	I_{IB}	V_{CM} = 0 V	-40°C to +105°C	01		+13	µA
			+25°C		+5 typical		
Input bias current drift	ΔI_{IB}		+25°C	01		±12	nA / °C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = ±5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC performance - continued.		R_L = 150 Ω 3/					
Input offset current	I_{IO}	V_{CM} = 0 V	-40°C to +105°C	01		±1.49	µA
			+25°C		±0.1 typical		
Input offset current drift	ΔI_{IO}		+25°C	01		±5	nA / °C
Input.							
Negative input 4/ voltage	$-V_{IN}$		-40°C to +105°C	01		-5.1	V
			+25°C		-5.5 typical		
Positive input 4/ voltage	$+V_{IN}$		-40°C to +105°C	01	2.8		V
			+25°C		3.2 typical		
Common mode rejection ratio	CMRR	Input - referred	-40°C to +105°C	01	72		dB
			+25°C		80 typical		
Input impedance.							
Differential mode 5/			+25°C	01	10||2.1 typical		kΩ||pF
Common mode 5/			+25°C	01	400||1.2 typical		kΩ||pF
Output.							
Output voltage swing		G = +2, R_L = 1 kΩ to GND	-40°C to +105°C	01	±4.84		V
			+25°C		±4.88 typical		
		G = +2, R_L = 150 Ω to GND	-40°C to +105°C		±4.56		
			+25°C		±4.64 typical		
Current output, sinking and sourcing			-40°C to +105°C	01	±55		mA
			+25°C		±85 typical		
Short circuit current	I_{OS}	Output shorted to ground	+25°C	01	150 typical		mA
Closed loop output impedance		G = +2, f ≤ 100 kHz	+25°C	01	0.06 typical		Ω

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = ±5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply.							
Minimum operating voltage			+25°C	01	±1.4 typical		V
Maximum operating voltage			-40°C to +105°C	01		±5.5	V
Maximum quiescent current		V_S = ±5 V	-40°C to +105°C	01		5.9	mA
			+25°C		4.25 typical		
Minimum quiescent current		V_S = ±5 V	-40°C to +105°C	01	3.19		mA
			+25°C		4.25 typical		
Power supply rejection ratio	+PSRR	Input referred	-40°C to +105°C	01	59		dB
			+25°C		66 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/ V_S = +5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC performance.		See figure 4.					
Small signal bandwidth	SSBW	G = +1, $V_O \leq 0.2\ V_{PP}$	+25°C	01	250 typical		MHz
		G = +2, $V_O \leq 0.2\ V_{PP}$	-40°C to +85°C		68		
			+25°C		110 typical		
		G = +5, $V_O \leq 0.2\ V_{PP}$	-40°C to +85°C		15		
			+25°C		24 typical		
		G = +10, $V_O \leq 0.2\ V_{PP}$	-40°C to +85°C		6		
			+25°C		11 typical		
Gain bandwidth product	GBWP	G ≥ +10	-40°C to +85°C	01	79		MHz
			+25°C		110 typical		
Peaking at a gain of +1		$V_O \leq 0.2\ V_{PP}$	+25°C	01	5 typical		dB
Slew rate	SR	G = +2, 2 V step	-40°C to +85°C	01	260		V/μs
			+25°C		550 typical		
Rise time	t_R	0.5 V step	-40°C to +85°C	01		5.9	ns
			+25°C		3.3 typical		
Fall time	t_F	0.5 V step	-40°C to +85°C	01		5.9	ns
			+25°C		3.3 typical		
Settling time to 0.1%	t_S	G = +2, 1 V step	-40°C to +85°C	01		67	ns
			+25°C		43 typical		
Harmonic distortion.		V_O = 2 V_{PP}, f = 5 MHz					
2 nd harmonic		R_L = 150 Ω	-40°C to +85°C	01		-53	dBc
			+25°C		-62 typical		
		$R_L \geq$ 500 Ω	-40°C to +85°C			-56	
			+25°C		-64 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.1/

Test	Symbol	Conditions 6/ V_S = +5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC performance – continued.		See figure 4.					
Harmonic distortion – continued.		V_O = 2 V_{PP}, f = 5 MHz					
3 rd harmonic		R_L = 150 Ω	-40°C to +85°C	01		-48	dBc
			+25°C		-58 typical		
		$R_L \geq$ 500 Ω	-40°C to +85°C			-60	
			+25°C		-84 typical		
Input voltage noise		f > 1 MHz	-40°C to +85°C	01		11.2	nV / $\sqrt{Hz}$
			+25°C		9.2 typical		
Input current noise		f > 1 MHz	-40°C to +85°C	01		5.5	pA / $\sqrt{Hz}$
			+25°C		3.5 typical		
NTSC differential gain			+25°C		0.08 typical		%
NTSC differential phase			+25°C		0.09 typical		°
DC performance.		R_L = 150 Ω3/					
Open loop voltage gain	A_{VOL}		-40°C to +105°C	01	64		dB
			+25°C		72 typical		
Input offset voltage	V_{IO}		-40°C to +105°C	01		±6.7	mV
			+25°C		±0.5 typical		
Average offset voltage drift	ΔV_{IO}		+25°C	01		±28	µV / °C
Input bias current	I_{IB}	V_{CM} = 2.5 V	-40°C to +105°C	01		+13	µA
			+25°C		+5 typical		
Input bias current drift	ΔI_{IB}		+25°C	01		±12	nA / °C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/ V_S = +5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC performance - continued.		R_L = 150 Ω 3/					
Input offset current	I_{IO}	V_{CM} = 2.5 V	-40°C to +105°C	01		±1.41	µA
			+25°C		±0.1 typical		
Input offset current drift	ΔI_{IO}		+25°C	01		±5	nA / °C
Input.							
Least positive input 4/ voltage	$+V_{IN}$		-40°C to +105°C	01		-0.2	V
			+25°C		-0.5 typical		
Most positive input 4/ voltage	$+V_{IN}$		-40°C to +105°C	01	2.75		V
			+25°C		3.2 typical		
Common mode rejection ratio	CMRR	Input - referred	-40°C to +105°C	01	72		dB
			+25°C		80 typical		
Input impedance.							
Differential mode 5/			+25°C	01	10||2.1 typical		kΩ||pF
Common mode 5/			+25°C	01	400||1.2 typical		kΩ||pF
Output.							
Least positive output voltage		G = +5, R_L = 1 kΩ to 2.5 V	-40°C to +105°C	01		0.13	V
			+25°C		0.09 typical		
		G = +5, R_L = 150 Ω to GND	-40°C to +105°C			0.26	
			+25°C		0.21 typical		
Most positive output voltage		G = +5, R_L = 1 kΩ to 2.5 V	-40°C to +105°C	01	4.87		V
			+25°C		4.91 typical		
		G = +5, R_L = 150 Ω to GND	-40°C to +105°C		4.72		
			+25°C		4.78 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/ V_S = +5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output – continued.							
Current output, sinking and sourcing			-40°C to +105°C	01	±52		mA
			+25°C		±80 typical		
Short circuit output current	I_{OS}	Output shorted to either supply	+25°C	01	140 typical		mA
Closed loop output impedance		G = +2, f ≤ 100 kHz	+25°C	01	0.06 typical		Ω
Power supply.							
Minimum operating voltage			+25°C	01	+2.8 typical		V
Maximum operating voltage			-40°C to +105°C	01		+11	V
Maximum quiescent current		V_S = +5 V	-40°C to +105°C	01		5.5	mA
			+25°C		3.9 typical		
Minimum quiescent current		V_S = +5 V	-40°C to +105°C	01	3.05		mA
			+25°C		3.9 typical		
Power supply rejection ratio	+PSRR	Input referred	-40°C to +105°C	01	59		dB
			+25°C		66 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, at -40°C ≤ T_J ≤ +105°C, G = +2, R_F = 750 Ω, and R_L = 150 Ω to GND.
For production testing of these parameters to the limits in table I herein, Ambient temperature (T_A) = Junction temperature (T_J).

3/ Current is considered positive out of pin.

4/ Tested < 3 dB below minimum specified CMRR at ± CMIR limits.

5/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

6/ Unless otherwise specified, at -40°C ≤ T_J ≤ +105°C, G = +2, R_F = 750 Ω, and R_L = 150 Ω to V_S / 2.

Case X

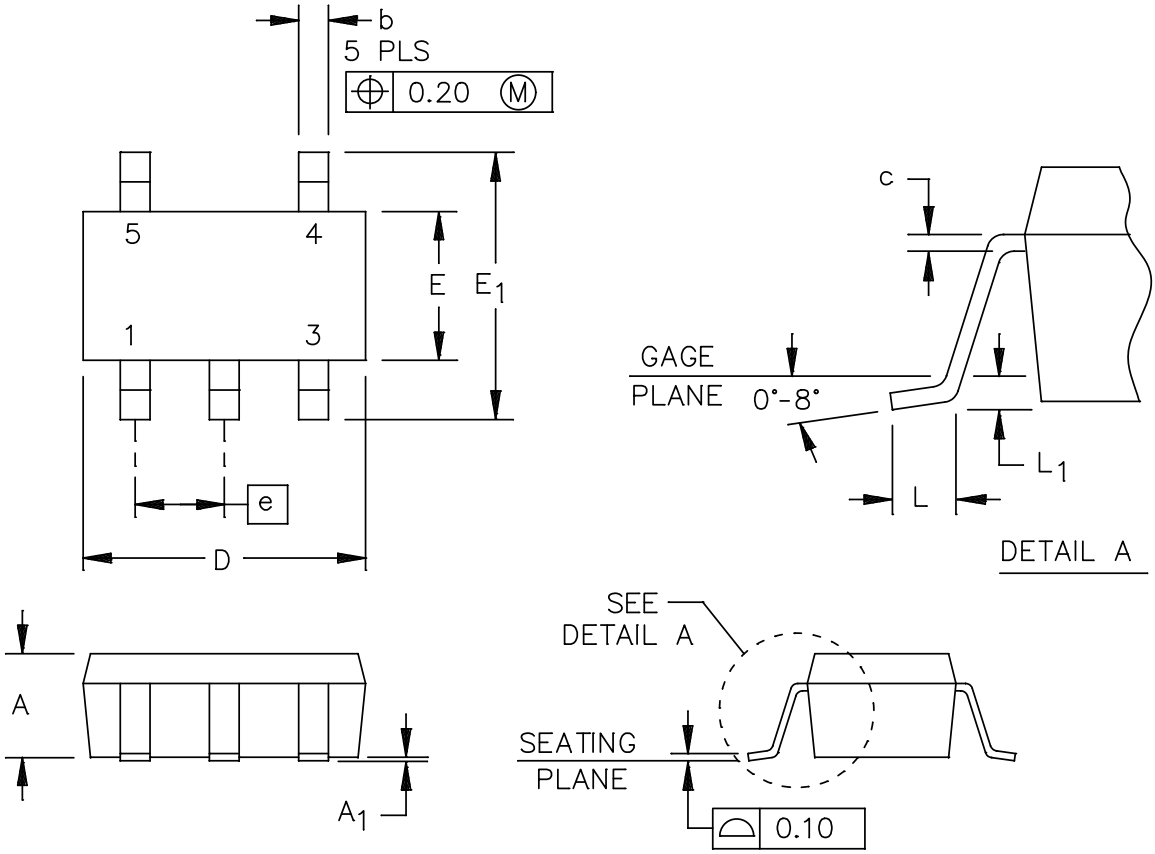

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14610
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Symbol	Dimensions			
	Inch		Millimeters	
	Min	Max	Min	Max
A	---	.057	---	1.45
A1	.000	.006	0.00	0.15
b	.011	.019	0.30	0.50
c	.003	.008	0.08	0.22
D	.108	.120	2.75	3.05
E	.057	.068	1.45	1.75
E1	.102	.118	2.60	3.00
e	.037 BSC		0.95 BSC	
L	.011	.023	0.30	0.60
L1	.009 BSC		0.25 BSC	
n	5 leads		5 leads	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 inch) per end.
3. Falls within reference to JEDEC MO-178.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	OUTPUT	O	Amplifier output.
2	-VS	I	Negative amplifier power supply input.
3	+INPUT	I	Non-inverting amplifier input.
4	-INPUT	I	Inverting amplifier input.
5	+VS	I	Positive amplifier power supply input.

FIGURE 2. Terminal connections.

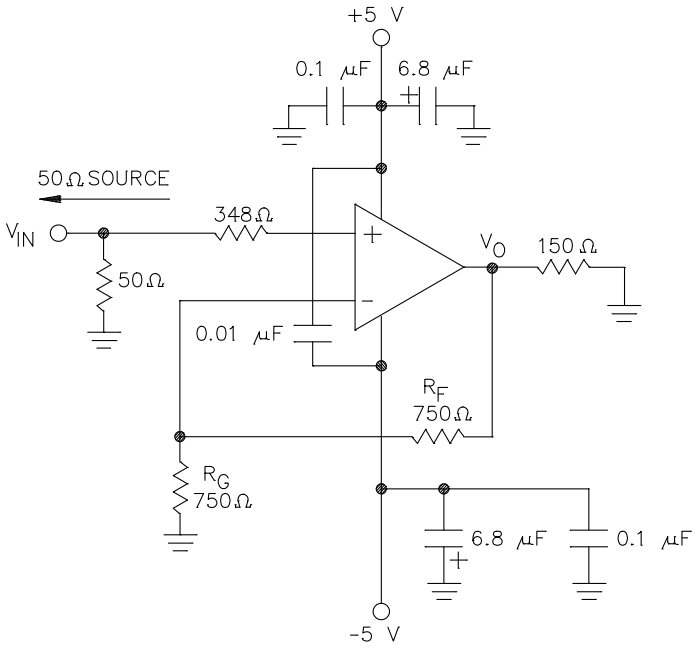

FIGURE 3. DC coupled, G = +2, bipolar supply test circuit.

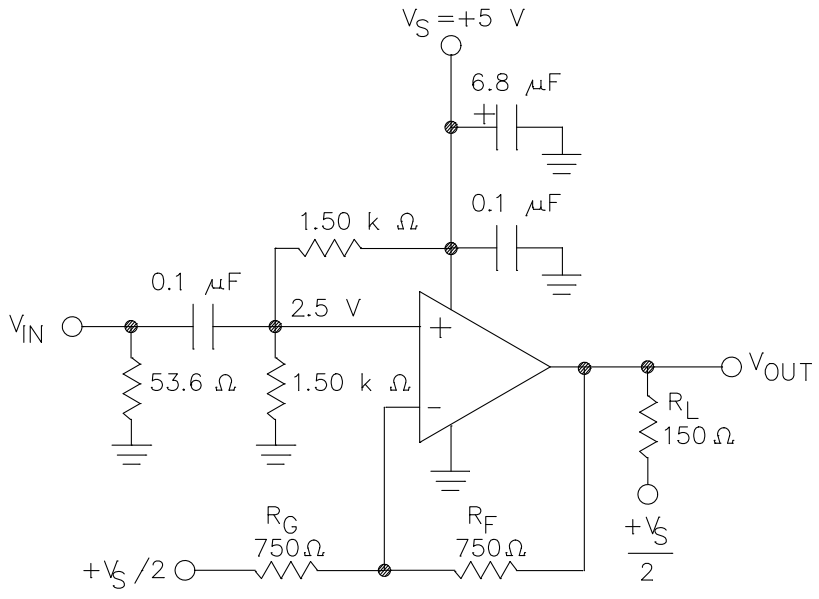

FIGURE 4. AC coupled, G = +2, +5 V single supply test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Transportation mode and quantity	Top side marking	Vendor part number
V62/14610-01XE	01295	Tape and reel, 3000	SLM	OPA830TDBVREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243