REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Under paragraph 1.3, add two footnotes to ESD parameter. Under paragraph 1.4, add minimum limit to the Clock input, Low speed enable parameter. Add two JEDEC references to section 2. Update document paragraphs to current requirements. ro	20-04-15	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV	A	A	A	A	A	A	A	A	A	A												
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REV STATUS OF PAGES																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 14-11-10	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, DIGITAL-LINEAR, DUAL CHANNEL, 14 BIT, 125 MSPS ULTRALOW POWER ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/14609**
	REV A	**PAGE** 1 **OF** 27

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V014-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual channel, 14 bit, 125 million samples per second (MSPS) ultralow power analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14609	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADS4245-EP	Dual channel, 14 bit, 125 MSPS ultralow power analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	64	See figure 1	Plastic quad leadless flat pack with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Analog supply voltage range (AV_{DD})	-0.3 V to 2.1 V
Digital supply voltage range (DV_{DD})	-0.3 V to 2.1 V
Voltage between analog ground (AGND) and output buffer ground (DRGND)	-0.3 V to 0.3 V
Voltage between AV_{DD} to output buffer supply (DRV_{DD}) (when AVDD leads DRV_{DD})	-2.4 V to 2.4 V
Voltage between DRV_{DD} to AV_{DD} (when DRV_{DD} leads AV_{DD})	-2.4 V to 2.4 V
Voltage applied to input pins:	
INP_A, INM_A, INP_B, INM_B	-0.3 V to minimum (1.9 V, AV_{DD} + 0.3 V) 2/
CLKP, CLKM	-0.3 V to AV_{DD} + 0.3 V 3/
RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3	-0.3 V to 3.9 V
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature range (T_J)	-55°C to +150°C
Electrostatic discharge (ESD) rating: 4/	
Human body model (HBM):	±2 kV 5/

1.4 Recommended operating conditions. 6/

Supplies:	
Analog supply voltage (AVDD)	1.7 V minimum, 1.8 V nominal, 1.9 V maximum
Digital supply voltage (DVDD)	1.7 V minimum, 1.8 V nominal, 1.9 V maximum
Analog inputs:	
Differential input voltage range	2 V_{PP} nominal
Input common mode voltage	V_{CM} ± 0.05 V nominal
Maximum analog input frequency with 2 V_{PP} input amplitude 7/	400 MHz nominal
Maximum analog input frequency with 1 V_{PP} input amplitude 7/	600 MHz nominal

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ There is an ESD protection circuit from the analog input pin (INPx or INMx) to AV_{DD} supply. To prevent this circuit from triggering, it is required that maximum voltage on these pins be kept lower than AV_{DD} + 0.3 V during device power up and never exceed the limit of 1.9 V.

3/ When AV_{DD} is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3 V|). This configuration prevents the ESD protection diodes at the clock input pins from turning on.

4/ Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.

5/ Level listed above is the passing per JEDEC JS-001. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

7/ See manufacturer’s datasheet for more information.

1.4 Recommended operating conditions - continued. 6/

Clock input:
Input clock sample rate:
Low speed mode enable 8/ ..... 1 MSPS minimum
80 MSPS maximum
Low speed mode disable 8/ (by default after reset) ..... 80 MSPS minimum,
125 MSPS maximum
Input clock duty cycle: 9/
Low speed mode disabled ..... 35 % minimum,
50 % nominal,
65 % maximum
Low speed mode enabled ..... 40 % minimum,
50 % nominal,
60 % maximum
Digital outputs:
Maximum external capacitance from each output pin to DRGND, C_L ..... 5 pF nominal
Differential load resistance between the LVDS output pairs (LVDS mode), R_L ..... 100 Ω nominal
Operating junction temperature range (T_J) ..... -55°C to +125°C

1.5 Thermal characteristics. 10/

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	23.9	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	10.9	°C/W
Thermal resistance, junction-to-board	θ_{JB}	4.3	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	0.1	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	4.4	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	0.6	°C/W

1.6 High performance modes. 11/ 12/

Parameter	Description
High performance mode	Set the high performance mode register bit obtain best performance across sample clock and input signal frequencies. Register address = 03h, data = 03h.
High frequency mode	Set the high frequency mode channel A and high frequency mode channel B register bits for high input signal frequencies greater than 200 MHz. Register address = 4Ah, data = 01h Register address = 58h, data = 01h

8/ See the manufacturer's datasheet for details on programming the low speed mode.
9/ Ensured by design for temperature range -40°C to +85°C.
10/ For more information about traditional and new thermal metrics, contact the manufacturer.
11/ It is recommended to use these modes to obtain best performance.
12/ See the manufacturer's datasheet for details on register programming.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Resolution			-55°C to +125°C	01		14	Bits
Signal to noise ratio	SNR	f_{IN} = 20 MHz	+25°C	01	73.4 typical		dBFS
		f_{IN} = 70 MHz	-55°C to +125°C		68		
			+25°C		72.9 typical		
		f_{IN} = 100 MHz	+25°C		72.6 typical		
		f_{IN} = 170 MHz	+25°C		71.4 typical		
		f_{IN} = 300 MHz	+25°C		69.3 typical		
Signal to noise ratio and distortion ratio	SINAD	f_{IN} = 20 MHz	+25°C	01	73.2 typical		dBFS
		f_{IN} = 70 MHz	-55°C to +125°C		68		
			+25°C		72.6 typical		
		f_{IN} = 100 MHz	+25°C		72.3 typical		
		f_{IN} = 170 MHz	+25°C		71.2 typical		
		f_{IN} = 300 MHz	+25°C		68.5 typical		
Spurious free dynamic range	SFDR	f_{IN} = 20 MHz	+25°C	01	88 typical		dBc
		f_{IN} = 70 MHz	-55°C to +125°C		71		
			+25°C		86 typical		
		f_{IN} = 100 MHz	+25°C		85 typical		
		f_{IN} = 170 MHz	+25°C		88 typical		
		f_{IN} = 300 MHz	+25°C		78 typical		
Total harmonic distortion	THD	f_{IN} = 20 MHz	+25°C	01	86 typical		dBc
		f_{IN} = 70 MHz	-55°C to +125°C		68		
			+25°C		84 typical		
		f_{IN} = 100 MHz	+25°C		83 typical		
		f_{IN} = 170 MHz	+25°C		84 typical		
		f_{IN} = 300 MHz	+25°C		75 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Second harmonic distortion	HD2	f_{IN} = 20 MHz	+25°C	01	88 typical		dBc
		f_{IN} = 70 MHz	-55°C to +125°C		66.5		
			+25°C		86 typical		
		f_{IN} = 100 MHz	+25°C		85 typical		
		f_{IN} = 170 MHz	+25°C		88 typical		
		f_{IN} = 300 MHz	+25°C		78 typical		
Third harmonic distortion	HD3	f_{IN} = 20 MHz	+25°C	01	93 typical		dBc
		f_{IN} = 70 MHz	-55°C to +125°C		72.5		
			+25°C		89 typical		
		f_{IN} = 100 MHz	+25°C		89 typical		
		f_{IN} = 170 MHz	+25°C		90 typical		
		f_{IN} = 300 MHz	+25°C		81 typical		
Worst spur (other than second and third harmonics)		f_{IN} = 20 MHz	+25°C	01	95 typical		dBc
		f_{IN} = 70 MHz	-55°C to +125°C		73		
			+25°C		94 typical		
		f_{IN} = 100 MHz	+25°C		93 typical		
		f_{IN} = 170 MHz	+25°C		91 typical		
		f_{IN} = 300 MHz	+25°C		89 typical		
Two tone intermodulation distortion	IMD	f_1 = 46 MHz, f_2 = 50 MHz, each tone at -7 dBFS	+25°C	01	96 typical		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at -7 dBFS			92 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Crosstalk		20 MHz full scale signal on channel under observation; 170 MHz full scale signal on other channel	+25°C	01	95 typical		dB
Input overload recovery		Recovery to within 1% (of full scale) for 6 dB overload with sine wave input	+25°C	01	1 typical		Clock cycle
AC power supply rejection ratio	PSRR	For 100 mV_{PP} signal on AV_{DD} supply, up to 10 MHz	+25°C	01	> 30 typical		dB
Effective number of bits	ENOB	f_{IN} = 70 MHz	+25°C	01	11.5 typical		LSBs
Differential nonlinearity	DNL	f_{IN} = 70 MHz	-55°C to +125°C	01	-0.97	1.9	LSBs
			+25°C		±0.5 typical		
Integrated nonlinearity	INL	f_{IN} = 70 MHz	-55°C to +125°C	01		±5	LSBs
			+25°C		±2 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 3/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Analog inputs							
Differential input voltage range (0 dB gain)			+25°C	01	2 typical		V_{PP}
Differential input resistance (at 200 MHz)			+25°C	01	0.75 typical		kΩ
Differential input capacitance (at 200 MHz)			+25°C	01	3.7 typical		pF
Analog input bandwidth (with 50 Ω source impedance, and 50 Ω termination			+25°C	01	550 typical		MHz
Analog input common mode current (per input pin of each channel)			+25°C	01	1.5 typical		μA/ MSPS
Common mode output voltage	V_{CM}		+25°C	01	0.95 typical		V
V_{CM} output current capability			+25°C	01	4 typical		mA
DC accuracy							
Offset voltage error			-55°C to +125°C	01	-25	25	mV
					2.5 typical		
Temperature coefficient of offset error			+25°C	01	0.003 typical		mV/°C
Gain error as a result of internal reference inaccuracy alone	E_{GREF}		-55°C to +125°C	01	-4	4	%FS
Gain error of channel alone	E_{GCHAN}		+25°C	01	±0.1 typical		%FS
Temperature coefficient of E_{GCHAN}			+25°C	01	0.002 typical		Δ%/°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 3/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Power supply							
Analog supply current	IAV_{DD}		-55°C to +125°C	01		130	mA
			+25°C		105 typical		
Output buffer supply current	$IDRV_{DD}$	LVDS interface, 350 mV swing with 100 Ω external termination, f_{IN} = 2.5 MHz	-55°C to +125°C	01		120	mA
			+25°C		99 typical		
Output buffer supply current	$IDRV_{DD}$	CMOS interface, no load capacitance, 4/ f_{IN} = 2.5 MHz	+25°C	01	49 typical		mA
Analog power			+25°C	01	189 typical		mW
Digital power		LVDS interface, 350 mV swing with 100 Ω external termination, f_{IN} = 2.5 MHz	+25°C	01	179 typical		mW
		CMOS interface, no load capacitance, 4/ f_{IN} = 2.5 MHz			88 typical		
Global power down			-55°C to +125°C	01		25	mW
Digital characteristics. 5/							
Digital inputs (RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3) 6/							
High level input voltage	V_{IH}	All digital inputs support 1.8 V and 3.3 V CMOS logic levels	-55°C to +125°C	01	1.3		V
Low level input voltage	V_{IL}	All digital inputs support 1.8 V and 3.3 V CMOS logic levels	-55°C to +125°C	01		0.4	V
High level input current	I_{IH}	SDATA, SCLK, V_{HIGH} = 1.8 V 7/	+25°C	01	10 typical		µA
		SEN, V_{HIGH} = 1.8 V 8/			0 typical		
Low level input current	I_{IL}	SDATA, SCLK, V_{LOW} = 0 V	+25°C	01	0 typical		µA
		SEN, V_{LOW} = 0 V			10 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 3/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Digital characteristics - continued. 5/							
Digital outputs, CMOS interface (DA[13:0], DB[13:0], CLKOUT, SDOUT). 6/							
High level output voltage	V_{OH}		-55°C to +125°C	01	DRV_{DD} – 0.1		V
			+25°C		DRV_{DD} typical		
Low level output voltage	V_{OL}		-55°C to +125°C	01		0.1	V
			+25°C		0 typical		
Digital outputs, LVDS interface. See figure 3.							
High level output differential voltage	V_{ODH}	With an external 100 Ω termination	-55°C to +125°C	01	220	490	mV
			+25°C		350 typical		
Low level output differential voltage	V_{ODL}	With an external 100 Ω termination	-55°C to +125°C	01	-490	-220	mV
			+25°C		-350 typical		
Output common mode voltage	V_{OCM}		-55°C to +125°C	01	0.9	1.25	V
			+25°C		1.05 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 9/ 10/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Timing characteristics: LVDS and CMOS modes. See figures 5, 6, and 7.							
Aperture delay	t_A		+25°C	01	0.8 typical		ns
Aperture delay matching		Between the two channels of the same device	+25°C	01	±70 typical		ps
Variation of aperture delay		Between two devices at the same temperature and DRVDD supply	+25°C	01	±150 typical		ps
Aperture jitter	t_J		+25°C	01	140 typical		f_S rms
Wakeup time		Time to valid data after coming out of STANDBY mode	-55°C to +125°C	01		100	µs
			+25°C		50 typical		
		Time to valid data after coming out of GLOBAL power down mode	-55°C to +125°C			500	
			+25°C		100 typical		
ADC latency 13/		Default latency after reset	+25°C	01	16 typical		Clock cycles
		Digital functions enabled (EN DIGITAL = 1)			24 typical		
DDR LVDS mode 14/							
Data setup time	t_{SU}	Data valid 15/ to zero crossing of CLKOUTP	-55°C to +125°C	01	1.5		ns
			+25°C		2.0 typical		
Data hold time	t_H	Zero crossing of CLKOUTP to data becoming invalid 15/	-55°C to +125°C	01	0.35		ns
			+25°C		0.6 typical		
Clock propagation delay	t_{PDI}	Input clock rising edge cross over to output clock rising edge cross over	-55°C to +125°C	01	5.0	7.5	ns
			+25°C		6.1 typical		
LVDS bit clock duty cycle		Duty cycle of differential clock, (CLKOUTP-CLKOUTM)	+25°C	01	49 typical		%

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 9/ 10/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Timing characteristics: LVDS and CMOS modes – continued. See figures 5, 6, and 7.							
DDR LVDS mode – continued. 14/							
Data rise time	t_{RISE}	Rise time measured from -100 mV to +100 mV, 1 MSPS ≤ sampling frequency ≤ 160 MSPS	+25°C	01	0.13 typical		ns
Data fall time	t_{FALL}	Fall time measured from +100 mV to -100 mV, 1 MSPS ≤ sampling frequency ≤ 160 MSPS	+25°C	01	0.13 typical		ns
Output clock rise time	$t_{CLKRISE}$	Rise time measured from -100 mV to +100 mV, 1 MSPS ≤ sampling frequency ≤ 160 MSPS	+25°C	01	0.13 typical		ns
Output clock fall time	$t_{CLKFALL}$	Fall time measured from +100 mV to -100 mV, 1 MSPS ≤ sampling frequency ≤ 160 MSPS	+25°C	01	0.13 typical		ns
Parallel CMOS mode.							
Data setup time	t_{SU}	Data valid 16/ to zero crossing of CLKOUT	-55°C to +125°C	01	1.6		ns
			+25°C		2.5 typical		
Data hold time	t_H	Zero crossing of CLKOUT to data becoming invalid 16/	-55°C to +125°C	01	2.3		ns
			+25°C		2.7 typical		
Clock propagation delay	t_{PDI}	Input clock rising edge cross over to output clock rising edge cross over	-55°C to +125°C	01	4.5	8.5	ns
			+25°C		6.4 typical		
Output clock duty cycle		Duty cycle of output clock, 1 MSPS ≤ sampling frequency ≤ 160 MSPS	+25°C	01	46 typical		%
Data rise time	t_{RISE}	Rise time measured from 20 % to 80 % of DRV_{DD}, 1 MSPS ≤ sampling frequency ≤ 160 MSPS	+25°C	01	1 typical		ns
Data fall time	t_{FALL}	Fall time measured from 80 % to 20 % of DRV_{DD}, 1 MSPS ≤ sampling frequency ≤ 160 MSPS	+25°C	01	1 typical		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 9/ 10/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Timing characteristics: LVDS and CMOS modes – continued. See figures 5, 6, and 7.							
Parallel CMOS mode – continued.							
Output clock rise time	tCLKRISE	Rise time measured from 20 % to 80 % of DRV_{DD}, 1 MSPS ≤ sampling frequency ≤ 160 MSPS	+25°C	01	1 typical		ns
Output clock fall time	tCLKFALL	Fall time measured from 80 % to 20 % of DRV_{DD}, 1 MSPS ≤ sampling frequency ≤ 160 MSPS	+25°C	01	1 typical		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, 50% clock duty cycle, -1 dBFS differential analog input, LVDS interface, and 0 dB gain.

3/ Unless otherwise specified, AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, 50% clock duty cycle, -1 dBFS differential analog input..

4/ In CMOS mode, the DRV_{DD} current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage. See the manufacture's datasheet for more information.

5/ Unless otherwise specified, AV_{DD} = 1.8 V and DRV_{DD} = 1.8 V. DC specifications refer to the condition where the digital outputs do not switch but, are permanently at a valid logic level "0" or "1".

6/ SCLK, SDATA, and SEN function as digital input pins in serial configuration mode.

7/ SDATA, SCLK have internal 150 kΩ pull down resistor.

8/ SEN has an internal 150 kΩ pull up resistor to AV_{DD}. Because the pull up is weak, SEN can also be driven by 1.8 V or 3.3 V CMOS buffers.

9/ Timing parameters are ensured by design and characterization and not tested in production.

10/ Unless otherwise specified, AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, sampling frequency = 160 MSPS, sine wave input clock, 1.5 V_{PP} clock amplitude, C_L = 5 pF 11/, and R_L = 100 Ω 12/.

11/ C_L is the effective external single ended load capacitance between each output pin and ground.

12/ R_L is the differential load resistance between the LVDS output pair.

13/ At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.

14/ Measurements are done with transmission line of 100 Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.

15/ Data valid refers to a logic high of +100 mV and a logic low of -100 mV.

16/ Data valid refers to a logic high of 1.26 V and a logic low of 0.54 V.

Case X

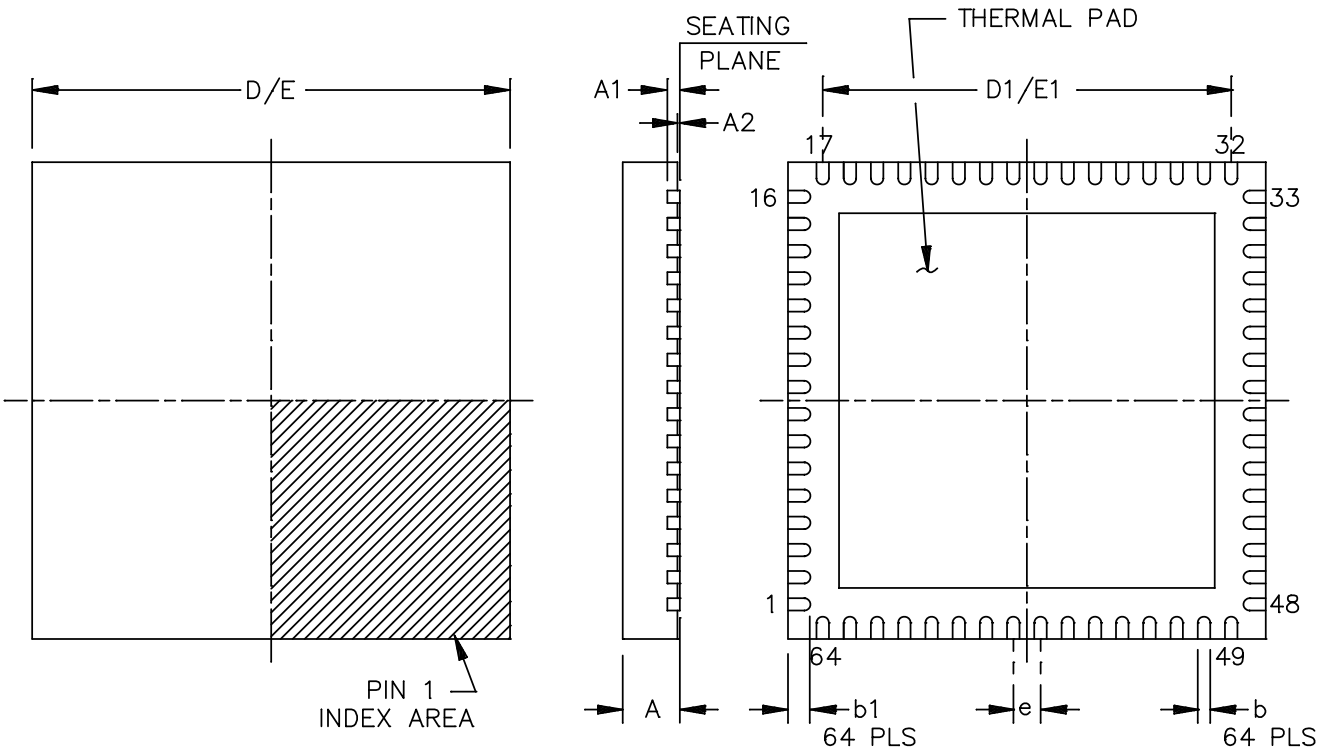

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14609
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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.031	0.039	0.80	1.00
A1	0.007 REF		0.20 REF	
A2	0.000	0.002	0.00	0.05
b	0.007	0.011	0.18	0.30
b1	0.011	0.019	0.30	0.50
D/E	0.348	0.360	8.85	9.15
D1/E1	0.295 BSC		7.50 BSC	
e	0.019 BSC		0.50 BSC	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The package thermal pad must be soldered to the board for thermal and mechanical performance.
3. See the additional figure in the manufacturer's data sheet for details regarding the exposed thermal pad features and dimensions.

FIGURE 1. Case outline - Continued.

LVDS mode

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DRVDD	17	AGND	33	AVDD	49	DRGND
2	DB4M	18	AGND	34	AVDD	50	DA8M
3	DB4P	19	INP_B	35	CTRL1	51	DA8P
4	DB6M	20	INM_B	36	CTRL2	52	DA10M
5	DB6P	21	AGND	37	CTRL3	53	DA10P
6	DB8M	22	AVDD	38	NC	54	DA12M
7	DB8P	23	VCM	39	NC	55	DA12P
8	DB10M	24	AGND	40	DA0M	56	CLKOUTM
9	DB10P	25	CLKP	41	DA0P	57	CLKOUTP
10	DB12M	26	CLKM	42	DA2M	58	NC
11	DB12P	27	AGND	43	DA2P	59	NC
12	RESET	28	AGND	44	DA4M	60	DB0M
13	SCLK	29	INP_A	45	DA4P	61	DB0P
14	SDATA	30	INM_A	46	DA6M	62	DB2M
15	SEN	31	AGND	47	DA6P	63	DB2P
16	AVDD	32	AGND	48	DRVDD	64	SDOUT

NOTES:

1. The thermal pad is connected to DRGND.
2. NC = do not connect; must float.
3. The output format for the LVDS mode is either offset binary or twos complement. The voltage level for the LVDS mode is 350 mV for logic 1 and -350 mV for logic 0.

FIGURE 2. Terminal connections.

LVDS mode – continued.

Terminal symbol	Number of pins	Function	Description
DRVDD	2	Input	Output buffer supply.
RESET	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option. In parallel interface mode, the RESET pin must be permanently tied high. SCLK and SEN are used as parallel control pins in this mode. This pin has an internal 150 kΩ pull down resistor.
SCLK	1	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low speed mode selection when RESET is tied high; see Table IV for detailed information. This pin has an internal 150 kΩ pull down resistor.
SDATA	1	Input	Serial interface data input; this pin has an internal 150 kΩ pull down resistor
SEN	1	Input	This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table V for detailed information. This pin has an internal 150 kΩ pull up resistor to AVDD.
AVDD	4	Input	Analog power supply.
AGND	8	Input	Analog ground.
INP_B	1	Input	Differential analog positive input, channel B.
INM_B	1	Input	Differential analog negative input, channel B.
VCM	1	Output	This pin outputs the common mode voltage (0.95 V) that can be used externally to bias the analog input pins.
CLKP	1	Input	Differential clock positive input.
CLKM	1	Input	Differential clock negative input.
INP_A	1	Input	Differential analog positive input, channel A.
INM_A	1	Input	Differential analog negative input, channel A.
CTRL1	1	Input	Digital control input pins. Together, they control the various power down modes.
CTRL2	1	Input	Digital control input pins. Together, they control the various power down modes.
CTRL3	1	Input	Digital control input pins. Together, they control the various power down modes.

FIGURE 2. Terminal connections - Continued.

LVDS mode – continued.

Terminal symbol	Number of pins	Function	Description
DRGND	2	Input	Output buffer ground.
CLKOUTM	1	Output	Differential output clock, complement.
CLKOUTP	1	Output	Differential output clock, true.
SDOUT	1	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is in high impedance state.
DA0P, DA0M	2	Output	Channel A differential output data pair, D0 and D1 multiplexed.
DA2P, DA2M	2	Output	Channel A differential output data D2 and D3 multiplexed.
DA4P, DA4M	2	Output	Channel A differential output data D4 and D5 multiplexed.
DA6P, DA6M	2	Output	Channel A differential output data D6 and D7 multiplexed.
DA8P, DA8M	2	Output	Channel A differential output data D8 and D9 multiplexed.
DA10P, DA10M	2	Output	Channel A differential output data D10 and D11 multiplexed.
DA12P, DA12M	2	Output	Channel A differential output data D12 and D13 multiplexed.
DB0P, DB0M	2	Output	Channel B differential output data pair, D0 and D1 multiplexed.
DB2P, DB2M	2	Output	Channel B differential output data D2 and D3 multiplexed.
DB4P, DB4M	2	Output	Channel B differential output data D4 and D5 multiplexed.
DB6P, DB6M	2	Output	Channel B differential output data D6 and D7 multiplexed.
DB8P, DB8M	2	Output	Channel B differential output data D8 and D9 multiplexed.
DB10P, DB10M	2	Output	Channel B differential output data D10 and D11 multiplexed.
DB12P, DB12M	2	Output	Channel B differential output data D12 and D13 multiplexed.
NC	4	---	Do not connect, must be floated.

FIGURE 2. Terminal connections - Continued.

CMOS mode

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DRVDD	17	AGND	33	AVDD	49	DRGND
2	DB4	18	AGND	34	AVDD	50	DA8
3	DB5	19	INP_B	35	CTRL1	51	DA9
4	DB6	20	INM_B	36	CTRL2	52	DA10
5	DB7	21	AGND	37	CTRL3	53	DA11
6	DB8	22	AVDD	38	NC	54	DA12
7	DB9	23	VCM	39	NC	55	DA13
8	DB10	24	AGND	40	DA0	56	UNUSED
9	DB11	25	CLKP	41	DA1	57	CLKOUT
10	DB12	26	CLKM	42	DA2	58	NC
11	DB13	27	AGND	43	DA3	59	NC
12	RESET	28	AGND	44	DA4	60	DB0
13	SCLK	29	INP_A	45	DA5	61	DB1
14	SDATA	30	INM_A	46	DA6	62	DB2
15	SEN	31	AGND	47	DA7	63	DB3
16	AVDD	32	AGND	48	DRVDD	64	SDOUT

NOTES:

1. The thermal pad is connected to DRGND.
2. NC = do not connect; must float.
3. The output format for the CMOS mode is either offset binary or twos complement. The voltage level for the CMOS mode is 1.8 V for logic 1 and 0 V for logic 0.

FIGURE 2. Terminal connections.

CMOS mode – continued.

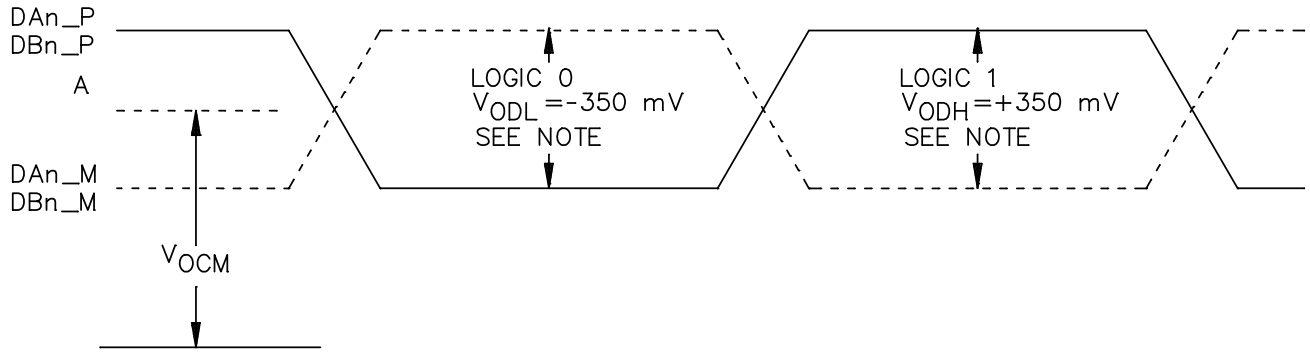
Terminal symbol	Number of pins	Function	Description
DRVDD	2	Input	Output buffer supply.
RESET	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option. In parallel interface mode, the RESET pin must be permanently tied high. SDATA and SEN are used as parallel control pins in this mode. This pin has an internal 150 kΩ pull down resistor.
SCLK	1	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low speed mode selection when RESET is tied high; see Table IV for detailed information. This pin has an internal 150 kΩ pull down resistor.
SDATA	1	Input	Serial interface data input; this pin has an internal 150 kΩ pull down resistor
SEN	1	Input	This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table V for detailed information. This pin has an internal 150 kΩ pull up resistor to AVDD.
AVDD	4	Input	Analog power supply.
AGND	8	Input	Analog ground.
INP_B	1	Input	Differential analog positive input, channel B.
INM_B	1	Input	Differential analog negative input, channel B.
VCM	1	Output	This pin outputs the common mode voltage (0.95 V) that can be used externally to bias the analog input pins.
CLKP	1	Input	Differential clock positive input.
CLKM	1	Input	Differential clock negative input.
INP_A	1	Input	Differential analog positive input, channel A.
INM_A	1	Input	Differential analog negative input, channel A.
CTRL1	1	Input	Digital control input pins. Together, they control the various power down modes.
CTRL2	1	Input	Digital control input pins. Together, they control the various power down modes.
CTRL3	1	Input	Digital control input pins. Together, they control the various power down modes.

FIGURE 2. Terminal connections - Continued.

CMOS mode – continued.

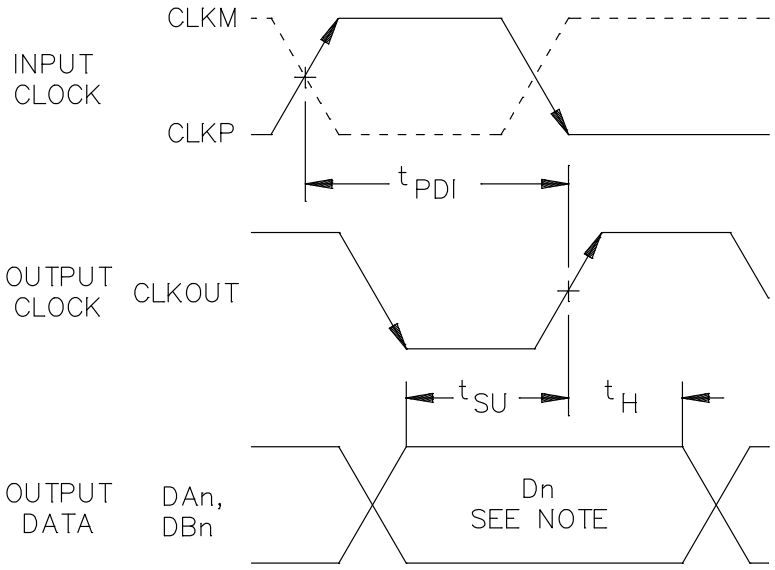
Terminal symbol	Number of pins	Function	Description
DRGND	2	Input	Output buffer ground.
UNUSED	1	---	This pin is not used in the CMOS interface.
CLKOUT	1	Output	CMOS output clock.
SDOUT	1	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is in high impedance state.
DA0 to DA11	12	Output	Channel A ADC output data bits, CMOS levels.
DA12 to DA13	2	Output	Channel A ADC output data bits, CMOS levels.
DB0 to DB11	12	Output	Channel B ADC output data bits, CMOS levels.
DB12 to DB13	2	Output	Channel B ADC output data bits, CMOS levels.
NC	4	---	Do not connect, must be floated.

FIGURE 2. Terminal connections - Continued.



NOTE: With external 100 Ω termination.

FIGURE 3. LVDS output voltage levels.



NOTE: Dn = bits D0, D1, D2, etc.. of channels A and B.

FIGURE 4. CMOS interface timing diagram.

TABLE II. LVDS timings at lower sampling frequencies.

Sampling frequency (MSPS)	Setup time (ns)			Hold time (ns)			Clock propagation delay, t_{PDI} (ns)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
65	5.9	6.6		0.35	0.6		5.0	6.1	7.5
80	4.5	5.2		0.35	0.6		5.0	6.1	7.5
125	2.3	2.9		0.35	0.6		5.0	6.1	7.5

TABLE III. CMOS timings at lower sampling frequencies.

Sampling frequency (MSPS)	Setup time (ns)			Hold time (ns)			Clock propagation delay, t_{PDI} (ns)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
65	6.1	7.2		6.7	7.1		4.5	6.4	8.5
80	4.7	5.8		5.3	5.8		4.5	6.4	8.5
125	2.7	3.6		3.1	3.6		4.5	6.4	8.5

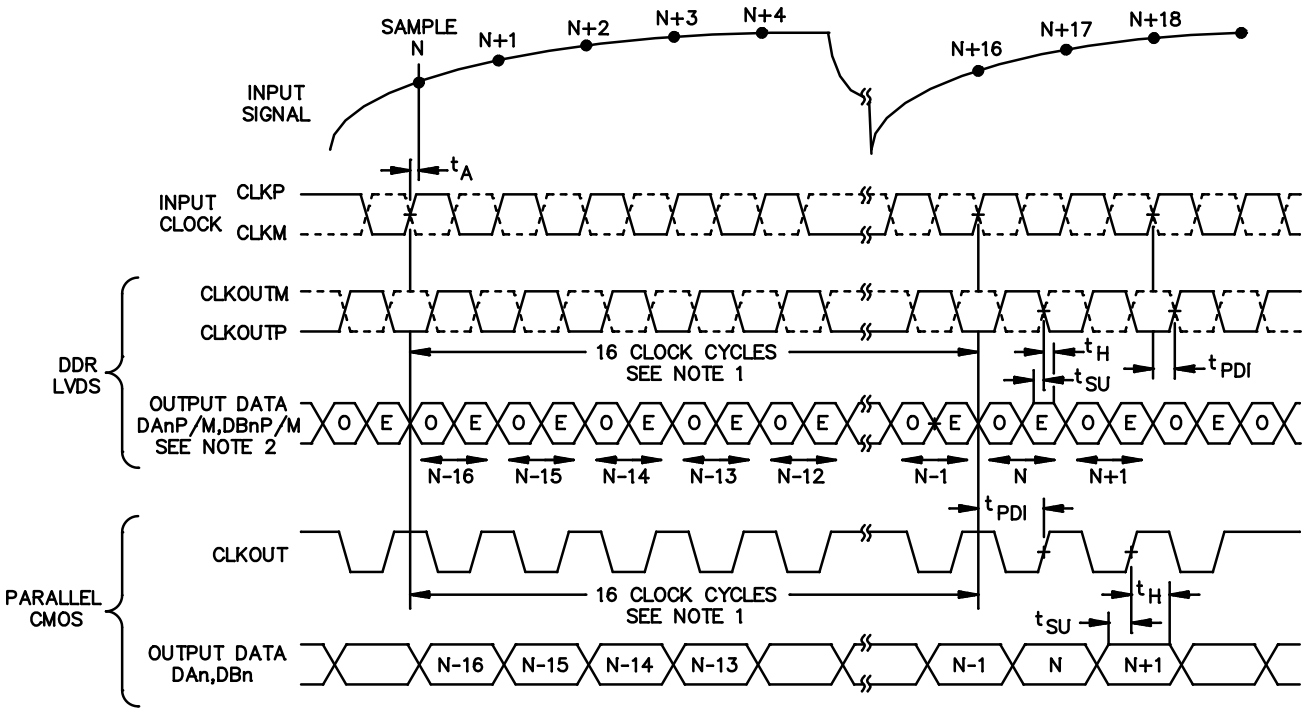
TABLE IV. SCLK control pin.

Voltage applied on SCLK	Description
Low	Low speed mode is disabled.
High	Low speed mode is enabled. 1/

1/ Low speed mode is enabled in the device by default.

TABLE V. SEN control pin.

Voltage applied on SEN	Description
0 (+50 mV / 0 mV)	Twos complement and parallel CMOS output.
(3/8) AVDD (±50 mV)	Offset binary and parallel CMOS output.
(5/8) 2AVDD (±50 mV)	Offset binary and DDR LVDS output.
AVDD (0 mV / -50 mV)	Twos complement and DDR LVDS output.



NOTES:

1. ADC latency after reset. At higher sampling frequencies, t_{PDI} is greater than one clock cycle, which then makes the overall latency = ADC latency + 1.
2. E = even bits (D0, D2, D4, etc..) and O = odd bits (D1, D3, D5, etc.).

FIGURE 5. Latency timing diagram.

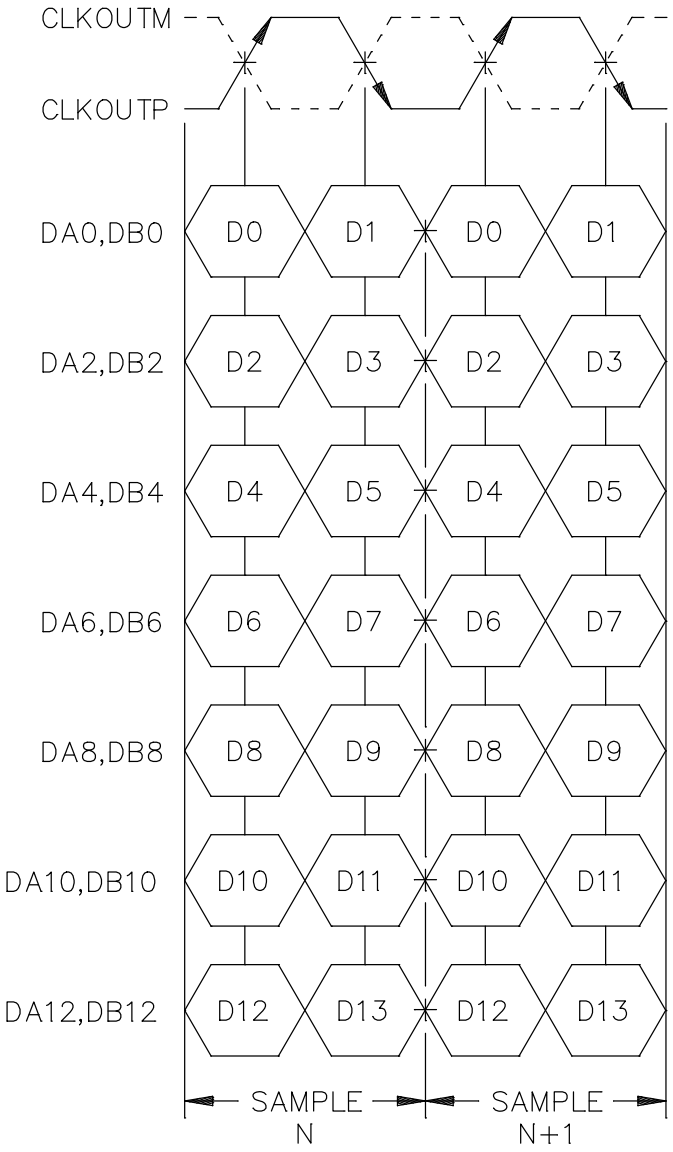


FIGURE 6. LVDS interface timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/ 2/ 3/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/14609-01XE	01295	AZ4245EP	ADS4245MRGC25EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243