REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current VID description requirements. - PHN	22-03-22	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A						
SHEET	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

Original date of drawing

YY MM DD

14-12-22

PREPARED BY
Phu H. Nguyen

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DEFENSE SUPPLY CENTER, COLUMBUS
COLUMBUS, OHIO 43218-3990

TITLE
MICROCIRCUIT, DIGITAL, MIXED SIGNAI MICRCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/14608
REV A		PAGE 1 OF 38

AMSC N/A

5962-V027-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance mixed signal microcontroller microcircuit, with an operating temperature range of -40ºC to +105ºC for device type 01 and -55ºC to +125ºC for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14608	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic		Circuit function
01	MSP430F5438-EP	-40°C to 105°C	Mixed signal microcontroller
02	MSP430F5438-EP	-55°C to 125°C	Mixed signal microcontroller

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	113	JEDEC MO-225	Plastic Ball Grid Array
Y	100	JEDEC MS-026	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage applied at V_{CC} to V_{SS} ..... -0.3 V to 4.1 V
Voltage apply to any pin (excluding VCORE) ..... -0.3 V to V_{CC} + 0.3 V 2/
Diode current at any device pin ..... ±2 mA
Storage temperature, T_{stg} ..... -55°C to 150°C 3/
Maximum junction temperature, T_J ..... 95°C

1.4 Thermal characteristics.

Thermal metric 4/	Case outline X	Case outline Y	Units
Junction to ambient thermal resistance, θ_{JA} 5/	43.6	49	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 6/	16.6	9.3	
Junction to board thermal resistance, θ_{JB} 7/	17.8	25	
Junction to top characterization parameter, Ψ_{JT} 8/	0.3	0.2	
Junction to board characterization parameter, Ψ_{JB} 9/	15.1	24.7	
Junction to case (bottom) thermal resistance, θ_{JCbot} 10/	N/A	N/A	

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltage referenced to V_{SS}. VCORE is for internal device usage only. No external DC loading or voltage should be applied.
3/ Higher temperature may be applied during board soldering according to the current JEDEC J-STD 020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
4/ For more information about traditional and new thermal metrics, see manufacturer data.
5/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.
6/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
7/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
8/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
9/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
10/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

1.5 Recommended operating conditions. 11/

Supply voltage during program execution and flash programming (AV_{CC} = $DV_{CC1/2/3/4}$= DV_{CC}):	1.8 V to 3.6 V 12/ 13/
Supply voltage (AV_{SS} = $DV_{SS1/2/3/4}$ =DV_{SS})	0 V
Operating free air temperature (T_A):	
Device type 01	-40°C to 125°C
Device type 02	-55°C to 125°C
Operating junction temperature (T_J):	
Device type 01	-40°C to 125°C
Device type 02	-55°C to 125°C
Recommended capacitor at VCORE (C_{VCORE})	470 Typical nF
Capacitor ratio of DVCC to VCORE (C_{DVCC}/C_{VCORE})	10
Processor frequency (maximum MCLK frequency) 14/ 15/ (See Figure 4)	
PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V, (default condition)	0 MHz to 8.0 MHz
PMMCOREVx = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V	0 MHz to 12.0 MHz
PMMCOREVx = 1, 2.2 V ≤ V_{CC} ≤ 3.6 V	0 MHz to 20.0 MHz
PMMCOREVx = 1, 2.4 V ≤ V_{CC} ≤ 3.6 V	0 MHz to 25.0 MHz

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51	–	Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).
JESD51-2a	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-8	–	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board
J-STD-020	–	Joint IPC/JEDEC standard for moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices.

(Copies of these documents are available online at https://www.jedec.org).

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available online at https:/www.ansi.org.

4/ Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).
5/ It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
6/ The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the PMM, SVS High Side threshold parameters for the exact values and further details.
7/ The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
8/ Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Frequency vs Supply Voltage. The Frequency vs Supply Voltage shall be as shown in figure 4.

3.5.5 SPI master mode, CKPH = 0. The SPI master mode, CKPH = 0 shall be as shown in figure 5.

3.5.6 SPI master mode, CKPH = 1. The SPI master mode, CKPH = 1 shall be as shown in figure 6.

3.5.7 SPI slave mode, CKPH = 0. The SPI slave mode, CKPH = 0 shall be as shown in figure 7.

3.5.8 SPI slave mode, CKPH = 1. The SPI slave mode, CKPH = 1 shall be as shown in figure 8.

3.5.9 I2C mode timing. The I2C mode timing shall be as shown in figure 9.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Condition 2/	V_{CC}	PMMCOREV	-55°C		-40°C		25°C		125 °C		Unit
					Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Low Power Mode Supply Current (into V_{CC}) Excluding External Current 3/ 4/													
Low power mode 0 6/ 7/	$I_{LPM0, 1MHz}$		2.2 V	0	69	93	69	93	69	93	85	150	µA
			3 V	3	73	100	73	100	73	100	90	150	
Low power mode 2 7/ 8/	I_{LPM2}		2.2 V	0	11	15.5	11	15.5	11	15.5	12.5	30	
			3 V	3	11.7	17.5	11.7	17.5	11.7	17.5	12.5	34	
Low power mode 3, crystal mode 9/ 7/	$I_{LPM3, XT1LF}$		2.2 V	0	1.4		1.4		1.7		8.5		
				1	1.5		1.5		1.8		9.9		
				2	1.5		1.5		2.0		10.1		
			3 V	0	1.8		1.8		2.1	2.4	7.1	21	
				1	1.8		1.8		2.3		10.5		
				2	1.9		1.9		2.4		10.6		
				3	2.0		2.0		2.3	2.6	11.8	34	
Low power mode 3, VLO mode 7/ 10/	$I_{LPM3, VLO}$		3 V	0	1.0		1.0		1.2	1.42	7.5	32	
				1	1.0		1.0		1.3		8		
				2	1.1		1.1		1.4		8.5		
				3	1.2		1.2		1.4	1.62	8.5	32	
Low power mode 4 7/ 11/	I_{LPM4}		3 V	0	1.1		1.1		1.2	1.35	7.5	30	
				1	1.2		1.2		1.2		8		
				2	1.3		1.3		1.3		8.5		
				3	1.3		1.3		1.3	1.52	8.5		
Low power mode 4.5 12/	$I_{LPM4.5}$		3 V		0.10		0.10		0.10	0.16	0.75	32	

Test	Execution Memory	Condition 2/	V_{CC}	PMMCOREV	Frequency (f_{DCO} = f_{MCLK} = f_{SMCLK})										Unit
					1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
					Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Active Mode Supply Current into V_{CC} Excluding External Current 3/ 4/ 5/															
$I_{AM, Flash}$	Flash		3 V	0	0.29	0.45	2.08	2.30							mA
				1	0.32		2.08		3.10						
				2	0.33		2.24		3.50		6.37				
				3	0.35		2.36		3.70		6.75		8.90	14	
$I_{AM, RAM}$	RAM			0	0.17	0.30	0.90	1.10							mA
			3 V	1	0.18		1.00		1.47						
				2	0.19		1.13		1.68		2.82				
				3	0.20		1.20		1.78		3.00		4.50	8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Schmitt-Trigger Inputs – General Purpose I/O 13/							
Positive going input threshold voltage	V_{IT+}		1.8 V	0.75		1.45	V
			3 V	1.45		2.15	
Negative going input threshold voltage	V_{IT+}		1.8 V	0.40		1.05	
			3 V	0.70		1.7	
Input voltage hysteresis (V_{IT+} - V_{IT-})	V_{hys}		1.8 V	0.25		0.9	
			3 V	0.35		1.05	
Pullup/Pulldown resistor	R_{Pull}	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		21	35	51	kΩ
Input capacitance	C_I	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
Inputs – Ports P1 and P2 15/							
External interrupt timing 16/	$t_{(int)}$	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag	2.2 V, 3 V		20		ns
Leakage Current – General Purpose I/O							
High-impedance leakage current	$I_{lkg(Px.x)}$	17/ 18/	1.8 V, 3 V			±50	nA
Outputs – General Purpose I/O (Full Drive Strength)							
High level output voltage	V_{OH}	$I_{(OHmax)}$ = –3 mA 19/	1.8 V	V_{CC} - 0.35		V_{CC}	V
		$I_{(OHmax)}$ = –10 mA 20/		V_{CC} - 0.70		V_{CC}	
		$I_{(OHmax)}$ = –5 mA 19/	3 V	V_{CC} - 0.35		V_{CC}	
		$I_{(OHmax)}$ = –15 mA 20/		V_{CC} - 0.70		V_{CC}	
Low level output voltage	V_{OL}	$I_{(OLmax)}$ = 3 mA 19/	1.8 V	V_{SS}		V_{SS} + 0.35	
		$I_{(OLmax)}$ = 10 mA 20/		V_{SS}		V_{SS} + 0.70	
		$I_{(OLmax)}$ = 5 mA 19/	3 V	V_{SS}		V_{SS} + 0.35	
		$I_{(OLmax)}$ = 15 mA 20/		V_{SS}		V_{SS} + 0.70	

See footnotes at end of table.

v6214608a

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits Min	Limits Typ	Limits Max	Unit
Outputs – General Purpose I/O (Reduced Drive Strength) 21/							
High level output voltage	V_{OH}	$I_{(OHmax)}$ = –1 mA 19/	1.8 V	V_{CC} - 0.35		V_{CC}	V
		$I_{(OHmax)}$ = –3 mA 20/		V_{CC} - 0.70		V_{CC}	
		$I_{(OHmax)}$ = –2 mA 19/	3 V	V_{CC} - 0.35		V_{CC}	
		$I_{(OHmax)}$ = –6 mA 20/		V_{CC} - 0.70		V_{CC}	
Low level output voltage	V_{OL}	$I_{(OLmax)}$ = 1 mA 19/	1.8 V	V_{SS}		V_{SS} + 0.35	
		$I_{(OLmax)}$ = 3 mA 20/		V_{SS}		V_{SS} + 0.70	
		$I_{(OLmax)}$ = 2 mA 19/	3 V	V_{SS}		V_{SS} + 0.35	
		$I_{(OLmax)}$ = 6 mA 20/		V_{SS}		V_{SS} + 0.70	
Output Frequency – General Purpose I/O							
Port output frequency (with load)	$f_{Px.y}$	P1.6/SMCLK 22/ 23/	V_{CC} = 1.8 V, PMMCOREVx = 0			16	MHz
			V_{CC} = 3 V, PMMCOREVx = 3			25	
Clock output frequency	f_{Port_CLK}	P1.0/TA0CLK/ACLK P1.6/SMCLK P2.0/TA1CLK/MCLK C_L = 20 pF 23/	V_{CC} = 1.8 V, PMMCOREVx = 0			16	
			V_{CC} = 3 V, PMMCOREVx = 3			25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Crystal Oscillator, XT1, Low-Frequency Mode 24/							
Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	$\Delta I_{DVCC.LF}$	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C	3 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
XT1 oscillator crystal frequency, LF mode	$f_{XT1,LF0}$	XTS = 0, XT1BYPASS = 0			32768		Hz
XT1 oscillator logic-level square wave input frequency, LF mode	$f_{XT1,LF,SW}$	XTS = 0, XT1BYPASS = 1 25/ 26/		10	32768	50	KHz
Oscillation allowance for LF crystals 27/	OA_{LF}	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
Integrated effective load capacitance, LF mode 28/	$C_{L,eff}$	XTS = 0, XCAPx = 0 29/			2		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
Duty cycle, LF mode		XTS = 0, Measured at ACLK, fXT1,LF = 32768 Hz		30		70	%
Oscillator fault frequency, LF mode 30/	$f_{Fault,LF}$	XTS = 0 31/		10		10000	Hz
Startup time, LF mode	$t_{STAR,LF}$	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 6 pF	3 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C, $C_{L,eff}$ = 12 pF			500		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Crystal Oscillator, XT1, High Frequency Mode 24/							
XT1 oscillator crystal current, HF mode	$I_{DVCC.HF}$	f_{OSC} = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C	3 V		200		µA
		f_{OSC} = 12 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C			260		
		f_{OSC} = 20 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			325		
		f_{OSC} = 32 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			450		
XT1 oscillator crystal frequency, HF mode 0	$f_{XT1,HF0}$	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0 32/		4		8	MHz
XT1 oscillator crystal frequency, HF mode 1	$f_{XT1,HF1}$	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 1 32/		8		16	
XT1 oscillator crystal frequency, HF mode 2	$f_{XT1,HF2}$	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2 32/		16		24	
XT1 oscillator crystal frequency, HF mode 3	$f_{XT1,HF3}$	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3 32/		24		32	
XT1 oscillator logic-level square-wave input frequency, HF mode, bypass mode	$f_{XT1,HF,SW}$	XTS = 1, XT1BYPASS = 1 32/ 25/		0.7		32	MHz
Oscillation allowance for HF crystals 33/	OA_{HF}	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,HF}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,HF}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2, $f_{XT1,HF}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3, $f_{XT1,HF}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Crystal Oscillator, XT1, High Frequency Mode - Continued 24/							
Startup time, HF mode	$t_{START,HF}$	f_{OSC} = 6 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3 V		0.5		ms
		f_{OSC} = 20 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
Integrated effective load capacitance, HF mode 28/ 34/	$C_{L,eff}$	XTS = 1			1		pF
Duty cycle, HF mode		XTS = 1 Measured at ACLK, $f_{XT1,HF2}$ = 20 MHz		40	50	60	%
Oscillator fault frequency, HF mode 30/	$f_{Fault,HF}$	XTS = 1 31/		30		300	kHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Crystal Oscillator, XT2 35/ 36/							
XT2 oscillator crystal current consumption	$I_{DVCC.XT2}$	f_{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C	3 V		200		µA
		f_{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 1, T_A = 25°C			260		
		f_{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C			325		
		f_{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 3, T_A = 25°C			450		
XT2 oscillator crystal frequency, mode 0	$f_{XT2,HF0}$	XT2DRIVEx = 0, XT2BYPASS = 0 32/		4		8	MHz
XT2 oscillator crystal frequency, mode 1	$f_{XT2,HF0}$	XT2DRIVEx = 1, XT2BYPASS = 0 32/		8		16	
XT2 oscillator crystal frequency, mode 2	$f_{XT2,HF0}$	XT2DRIVEx = 2, XT2BYPASS = 0 32/		16		24	
XT2 oscillator crystal frequency, mode 3	$f_{XT2,HF0}$	XT2DRIVEx = 3, XT2BYPASS = 0 32/		24		32	
XT2 oscillator logic-level square wave input frequency, bypass mode	$f_{XT2,HF,SW}$	XT2BYPASS = 1 32/ 37/		0.7		32	MHz
Oscillation allowance for HF crystals 33/	OA_{HF}	XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 p			450		Ω
		XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 12 MHz, $C_{L,eff}$ = 15 p			320		
		XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 20 MHz, $C_{L,eff}$ = 15 p			200		
		XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 32 MHz, $C_{L,eff}$ = 15 p			200		
Startup time	$t_{START,HF}$	f_{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3 V		0.5		ms
		f_{OSC} = 20 MHz, XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
Integrated effective load capacitance, HF mode 35/ 38/	$C_{L,eff}$				1		pF
Duty cycle, HF mode		Measured at ACLK, $f_{XT2,HF2}$ = 20 MHz		40	50	60	%
Oscillator fault frequency 30/	$f_{Fault,HF}$	XT2BYPASS = 1 39/		30		300	kHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits			Unit
				Min	Typ	Max	
Internal Very-Low-Power Low-Frequency Oscillator (VLO)							
VLO frequency	f_{VLO}	Measured at ACLK	1.8 V to 3.6 V	5	9.4	14	kHz
VLO frequency temperature drift	df_{VLO}/d_T	Measured at ACLK 40/	1.8 V to 3.6 V		0.5		%/°C
VLO frequency supply voltage drift	df_{VLO}/dV_{CC}	Measured at ACLK 41/	1.8 V to 3.6 V		4		%/V
Duty cycle		Measured at ACLK	1.8 V to 3.6 V	40	50	60	%
Internal Reference, Low-Frequency Oscillator (REFO)							
REFO oscillator current consumption	I_{REFO}	T_A = 25°C	1.8 V to 3.6 V		3		µA
REFO frequency calibrated		Measured at ACLK	1.8 V to 3.6 V		32768		Hz
REFO absolute tolerance calibrated	f_{REFO}	Full temperature range	1.8 V to 3.6 V		±3.5		%
		T_A = 25°C	3 V		±1.5		%
REFO frequency temperature drift	df_{REFO}/d_T	Measured at ACLK 40/	1.8 V to 3.6 V		0.01		%/°C
REFO frequency supply voltage drift	df_{REFO}/dV_{CC}	Measured at ACLK 41/	1.8 V to 3.6 V		1.0		%/V
Duty cycle		Measured at ACLK	1.8 V to 3.6 V	40	50	60	%
REFO startup time	t_{START}	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Limits			Unit
			Min	Typ	Max	
DCO frequency						
DCO frequency (0, 0) 42/	$f_{DCO(0,0)}$	DCORSELx = 0, DCOx = 0, MODx = 0	0.065		0.25	MHz
DCO frequency (0, 31) 42/	$f_{DCO(0,31)}$	DCORSELx = 0, DCOx = 31, MODx = 0	0.65		1.75	
DCO frequency (1, 0) 42/	$f_{DCO(0,0)}$	DCORSELx = 1, DCOx = 0, MODx = 0	0.10		0.41	
DCO frequency (1, 31) 42/	$f_{DCO(0,31)}$	DCORSELx = 1, DCOx = 31, MODx = 0	1.42		3.5	
DCO frequency (2, 0) 42/	$f_{DCO(0,0)}$	DCORSELx = 2, DCOx = 0, MODx = 0	0.27		0.8	
DCO frequency (2, 31) 42/	$f_{DCO(0,31)}$	DCORSELx = 2, DCOx = 31, MODx = 0	3.12		7.43	
DCO frequency (3, 0) 42/	$f_{DCO(0,0)}$	DCORSELx = 3, DCOx = 0, MODx = 0	0.59		1.56	
DCO frequency (3, 31) 42/	$f_{DCO(0,31)}$	DCORSELx = 3, DCOx = 31, MODx = 0	6.02		14.05	
DCO frequency (4, 0) 42/	$f_{DCO(0,0)}$	DCORSELx = 4, DCOx = 0, MODx = 0	1.25		3.25	
DCO frequency (4, 31) 42/	$f_{DCO(0,31)}$	DCORSELx = 4, DCOx = 31, MODx = 0	12.25		28.25	
DCO frequency (5, 0) 42/	$f_{DCO(0,0)}$	DCORSELx = 5, DCOx = 0, MODx = 0	2.45		6.05	
DCO frequency (5, 31) 42/	$f_{DCO(0,31)}$	DCORSELx = 5, DCOx = 31, MODx = 0	23.65		54.15	
DCO frequency (6, 0) 42/	$f_{DCO(0,0)}$	DCORSELx = 6, DCOx = 0, MODx = 0	4.55		10.75	
DCO frequency (6, 31) 42/	$f_{DCO(0,31)}$	DCORSELx = 6, DCOx = 31, MODx = 0	38.95		88.05	
DCO frequency (7, 0) 42/	$f_{DCO(0,0)}$	DCORSELx = 7, DCOx = 0, MODx = 0	8.45		19.65	
DCO frequency (7, 31) 42/	$f_{DCO(0,31)}$	DCORSELx = 7, DCOx = 31, MODx = 0	59.95		135.05	
Frequency step between range DCORSEL and DCORSEL + 1	f_{CORSEL}	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
Frequency step between tap DCO and DCO + 1	S_{DCO}	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	
Duty cycle		Measured at SMCLK	40	50	60	%
DCO frequency temperature drift 40/	df_{DCO}/dT	f_{DCO} = 1 MHz		0.1		%/°C
DCO frequency voltage drift 41/	df_{DCO}/dV_{CC}	f_{DCO} = 1 MHz		1.9		%/V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Limits			Unit
			Min	Typ	Max	
PMM, Brown-Out Reset (BOR)						
BORH on voltage, DV_{CC} falling level	$V_{(DVCC\_BOR\_IT-)}$	$\lvert dDV_{CC}/d_t \rvert$ < 3 V/s			1.47	V
BORH off voltage, DV_{CC} rising level	$V_{(DVCC\_BOR\_IT+)}$	$\lvert dDV_{CC}/d_t \rvert$ < 3 V/s	0.78	1.30	1.52	V
BORH hysteresis	$V_{(DVCC\_BOR\_hys)}$		58		275	mV
Pulse length required at $\overline{RST}$/NMI pin to accept a reset	t_{RESET}		2			µs
PMM, Core Voltage						
Core voltage, active mode, PMMCOREV = 3	$V_{CORE3(AM)}$	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.90		V
Core voltage, active mode, PMMCOREV = 2	$V_{CORE2(AM)}$	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.80		
Core voltage, active mode, PMMCOREV = 1	$V_{CORE1(AM)}$	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.60		
Core voltage, active mode, PMMCOREV = 0	$V_{CORE0(AM)}$	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.40		
Core voltage, low current mode, PMMCOREV = 3	$V_{CORE3(LPM)}$	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.94		
Core voltage, low current mode, PMMCOREV = 2	$V_{CORE2(LPM)}$	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.84		
Core voltage, low current mode, PMMCOREV = 1	$V_{CORE1(LPM)}$	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.64		
Core voltage, low current mode, PMMCOREV = 0	$V_{CORE0(LPM)}$	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.44		
PMM, SVS High Side						
SVS current consumption		SVSHE = 0, DV_{CC} = 3.6 V		0		nA
	$I_{(SVSH)}$	SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		1.5		µA
SVS_H on voltage level 43/	$V_{(SVSH\_IT-)}$	SVSHE = 1, SVSHRVL = 0	1.55	1.68	1.8	V
		SVSHE = 1, SVSHRVL = 1	1.77	1.88	2	
		SVSHE = 1, SVSHRVL = 2	1.96	2.08	2.23	
		SVSHE = 1, SVSHRVL = 3	2.07	2.18	2.33	
SVS_H off voltage level 43/	$V_{(SVSH\_IT+)}$	SVSHE = 1, SVSMHRRL = 0	1.60	1.74	1.87	
		SVSHE = 1, SVSMHRRL = 1	1.86	1.94	2.09	
		SVSHE = 1, SVSMHRRL = 2	2.05	2.14	2.3	
		SVSHE = 1, SVSMHRRL = 3	2.18	2.30	2.44	
		SVSHE = 1, SVSMHRRL = 4	2.30	2.40	2.57	
		SVSHE = 1, SVSMHRRL = 5	2.50	2.70	2.9	
		SVSHE = 1, SVSMHRRL = 6	2.85	3.10	3.25	
		SVSHE = 1, SVSMHRRL = 7	2.85	3.10	3.25	
SVS_H propagation delay	$t_{pd(SVSH)}$	SVSHE = 1, SVSHFP = 1 dV_{DVCC}/dt = 10 mV/µs,		2.5		µs
		SVSHE = 1, SVSHFP = 0 dV_{DVCC}/dt = 1 mV/µs		20		
SVS_H on or off delay time	$t_{(SVSH)}$	SVSHE = 0 → 1, SVSHFP = 1 dV_{DVCC}/dt = 10 mV/µs,		12.5		
		SVSHE = 0 → 1, SVSHFP = 0 dV_{DVCC}/dt = 10 mV/µs,		100		
DV_{CC} rise time	dV_{DVCC}/dt		0		1000	V/s

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Limits			Unit
			Min	Typ	Max	
PMM, SVM High Side						
SVM_H current consumption	$I_{(SVMH)}$	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		1.5		µA
SVM_H on or off voltage level 44/	$V_{(SVMH)}$	SVMHE = 1, SVSMHRRL = 0	1.61	1.74	1.87	V
		SVMHE = 1, SVSMHRRL = 1	1.86	1.94	2.09	
		SVMHE = 1, SVSMHRRL = 2	2.05	2.14	2.30	
		SVMHE = 1, SVSMHRRL = 3	2.18	2.30	2.44	
		SVMHE = 1, SVSMHRRL = 4	2.30	2.40	2.58	
		SVMHE = 1, SVSMHRRL = 5	2.50	2.70	2.93	
		SVMHE = 1, SVSMHRRL = 6	2.85	3.10	3.25	
		SVMHE = 1, SVSMHRRL = 7	2.85	3.10	3.25	
		SVMHE = 1, SVMHOVPE = 1		3.75		
SVM_H propagation delay	$t_{pd(SVMH)}$	SVMHE = 1, SVMHFP = 1 dV_{DVCC}/dt = 10 mV/µs,		2.5		µs
		SVMHE = 1, SVMHFP = 0 dV_{DVCC}/dt = 1 mV/µs		20		
SVM_H on or off delay time	$t_{(SVMH)}$	SVMHE = 0 → 1, SVMHFP = 1 dV_{DVCC}/dt = 10 mV/µs,		12.5		µs
		SVMHE = 0 → 1, SVMHFP = 0 dV_{DVCC}/dt = 10 mV/µs,		100		
PMM, SVS Low Side						
SVS_L current consumption	$I_{(SVSL)}$	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		1.5		µA
SVS_L propagation delay	$t_{pd(SVSL)}$	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		2.5		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		20		
SVS_L on or off delay time	$t_{(SVSL)}$	SVSLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		12.5		
		SVSLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		100		
PMM, SVM Low Side						
SVM_L current consumption	$I_{(SVML)}$	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 0		200		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 1		1.5		µA
SVM_L propagation delay	$t_{pd(SVML)}$	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		20		
SVM_L on or off delay time	$t_{(SVML)}$	SVMLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		12.5		
		SVMLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/		V_{CC}	Limits Min	Limits Typ	Limits Max	Unit
Wake-Up From Low Power Modes and Reset								
Wake up time from LPM2, LPM3, or LPM4 to active mode 45/	$t_{WAKE-UP-FAST}$	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	$f_{MCLK} \geq 4.0$ MHz			3.5	7.5	µs
			1.0 MHz < f_{MCLK} < 4.0 MHz			4.5	9.5	
Wake up time from LPM2, LPM3, or LPM4 to active mode 46/	$t_{WAKE-UP-SLOW}$	PMMCOREV = SVSMLRRL = n where n = 0, 1, 2, or 3), SVSLFP = 0				150	170	µs
Wake up time from LPM4.5 to active mode 45/	$t_{WAKE-UP-LPM5}$					2	3.5	ms
Wake up time from $\overline{RST}$ or BOR event to active mode 47/	$t_{WAKE-UP-RESET}$					2	3.5	ms
Timer_A								
Timer_A input clock frequency	f_{TA}	Internal: SMCLK, ACLK, External: TACLK, Duty cycle = 50% ± 10%		1.8 V, 3 V			25	MHz
Timer_A capture timing	$t_{TA,cap}$	All capture inputs Minimum pulse width required for capture		1.8 V, 3 V	20			ns
Timer_B								
Timer_B input clock frequency	f_{TB}	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ± 10%		1.8 V, 3 V			25	MHz
Timer_B capture timing	$t_{TB,cap}$	All capture inputs Minimum pulse width required for capture		1.8 V, 3 V	20			ns
USCI (UART Mode) Recommended Operating Conditions								
USCI input clock frequency	f_{USCI}	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = 50% ± 10%					f_{SYSTEM}	MHz
BITCLK clock frequency (equals baud rate in MBaud)	f_{BITCLK}						1	
USCI (UART Mode)								
UART receive deglitch time	t_T			2.2 V	50		600	ns
				3 V	48		620	
USCI (SPI Master Mode) Recommended Operating Conditions								
USCI input clock frequency	f_{USCI}	Internal: SMCLK, ACLK, Duty cycle = 50% ± 10%					f_{SYSTEM}	MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits			Unit
				Min	Typ	Max	
USCI (SPI Master Mode) 49/ see FIGURE 5 and 6							
USCI input clock frequency	f_{USCI}	SMCLK, ACLK, Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
SOMI input data setup time	$t_{SU,MI}$	PMMCOREV = 0	1.8 V	55			ns
			3 V	38			
		PMMCOREV = 3	2.4 V	30			
			3 V	25			
SOMI input data hold time	$t_{HD,MI}$	PMMCOREV = 0	1.8 V	0			
			3 V	0			
		PMMCOREV = 3	2.4 V	0			
			3 V	0			
SIMO output data valid time 50/	$t_{VALID,MO}$	UCLK edge to SIMO valid,	1.8 V			20	
		C_L = 20 pF, PMMCOREV = 0	3 V			18	
		UCLK edge to SIMO valid,	2.4 V			16	
		C_L = 20 pF, PMMCOREV = 3	3 V			15	
SIMO output data hold time 51/	$t_{HD,MO}$	CL = 20 pF, PMMCOREV = 0	1.8 V	-10			
			3 V	-8			
		CL = 20 pF, PMMCOREV = 3	2.4 V	-10			
			3 V	-8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits			Unit
				Min	Typ	Max	
USCI (SPI Slave Mode) 52/ see FIGURE 7 and 8							
STE lead time, STE low to clock	$t_{STE,LEAD}$	PMMCOREV = 0	1.8 V	11			ns
			3 V	8			
		PMMCOREV = 3	2.4 V	7			
			3 V	6			
STE lag time, Last clock to STE high	$t_{STE,LAG}$	PMMCOREV = 0	1.8 V	3			
			3 V	3			
		PMMCOREV = 3	2.4 V	3			
			3 V	3			
STE access time, STE low to SOMI data out	$t_{STE,ACC}$	PMMCOREV = 0	1.8 V			66	
			3 V			50	
		PMMCOREV = 3	2.4 V			36	
			3 V			30	
STE disable time, STE high to SOMI high impedance	$t_{STE,DIS}$	PMMCOREV = 0	1.8 V			30	
			3 V			23	
		PMMCOREV = 3	2.4 V			16	
			3 V			13	
SIMO input data setup time	$t_{SU,SI}$	PMMCOREV = 0	1.8 V	5			
			3 V	5			
		PMMCOREV = 3	2.4 V	2			
			3 V	2			
SIMO input data hold time	$t_{HD,SI}$	PMMCOREV = 0	1.8 V	5			
			3 V	5			
		PMMCOREV = 3	2.4 V	5			
			3 V	5			
SOMI output data valid time 52/	$t_{VALID,SO}$	UCLK edge to SOMI valid, C_L = 20 pF	1.8 V			76	
		PMMCOREV = 0	3 V			60	
		UCLK edge to SOMI valid,	2.4 V			44	
		C_L = 20 pF	3 V			40	
		PMMCOREV = 3					
SOMI output data hold time 53/	$t_{HD,SO}$	C_L = 20 pF	1.8 V	18			
		PMMCOREV = 0	3 V	12			
		C_L = 20 pF	2.4 V	10			
		PMMCOREV = 3	3 V	8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits			Unit
				Min	Typ	Max	
USCI (I2C Mode) see FIGURE 9							
USCI input clock frequency	f_{USCI}	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
SCL clock frequency	f_{SCL}		2.2 V, 3 V	0		400	kHz
Hold time (repeated) START	$t_{HD,STA}$	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
Setup time for a repeated START	$t_{SU,STA}$	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7			
		f_{SCL} > 100 kHz		0.6			
Data hold time	$t_{HD,DAT}$		2.2 V, 3 V	0			ns
Data setup time	$t_{SU,DAT}$		2.2 V, 3 V	250			ns
Setup time for STOP	$t_{SU,STO}$	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
Pulse duration of spikes suppressed by input filter	t_{SP}		2.2 V	50		600	ns
			3 V	50		600	
12-Bit ADC, Power Supply and Input Range Conditions 55/							
Analog supply voltage	AV_{CC}	AVCC and DVCC are connected together, AVSS and DVSS are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
Analog input voltage range 56/	$V_{(Ax)}$	All ADC12 analog input pins Ax		0		AV_{CC}	V
Operating supply current into AV_{CC} terminal 57/	I_{ADC12_A}	$f_{ADC12CLK}$ = 5.0 MHz 58/	2.2 V		125	155	µA
			3 V		150	270	
Input capacitance	C_I	Only one terminal Ax can be selected at one time			20		pF
Input MUX ON resistance	R_I	0 V ≤ VAx ≤ AV_{CC}			200		Ω
12-Bit ADC, Timing Parameters							
ADC conversion clock	$f_{ADC12CLK}$	For specified performance of ADC12 linearity parameters using an external reference voltage or AV_{CC} as reference 59/	2.2 V, 3 V	0.45	4.8	5.0	MHz
		For specified performance of ADC12 linearity parameters using the internal reference 60/		0.45	2.4	4.0	
		For specified performance of ADC12 linearity parameters using the internal reference 61/		0.45	2.4	2.7	
Internal ADC12 oscillator 62/	$f_{DC12OSC}$	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
Conversion time	$t_{CONVERT}$	REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock	2.2 V, 3 V	2.4		3.1	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			63/		
Sampling time	t_{Sample}	R_S = 400 Ω, R_I = 1000 Ω, C_I = 20 pF, T = [R_S + R_I] × C_I 64/	2.2 V, 3 V	1000			ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits Min	Limits Typ	Limits Max	Unit
12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage							
Integral linearity error 65/	E_I	1.4 V ≤ dVREF ≤ 1.6 V 66/	2.2 V, 3 V		±2.0		LSB
		1.6 V < dVREF 66/			±1.7		
Differential linearity error 65/	E_D	66/	2.2 V, 3 V		±1.0		
Offset error 67/	E_O	dVREF ≤ 2.2 V 66/	2.2 V, 3 V		±2.0		
		dVREF > 2.2 V 66/	2.2 V, 3 V		±2.0		
Gain error 67/	E_G	66/	2.2 V, 3 V		±2.0		
Total unadjusted error	E_T	dVREF ≤ 2.2 V 66/	2.2 V, 3 V		±3.5		
		dVREF > 2.2 V 66/	2.2 V, 3 V		±3.5		
12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage							
Integral linearity error 65/	E_I	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±1.7	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±2.5	
Differential linearity error 65/	E_D	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±2.0	
		ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 2.7 MHz			±1.5	
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±2.5	
Offset error 67/	E_O	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±4.0	
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±4.0	
Gain error 67/	E_G	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±2.5	
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±1.5% 69/	VREF
Total unadjusted error	E_T	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±5	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±1.5% 69/	VREF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Min	Limits Typ	Max	Unit
12-Bit ADC, Temperature Sensor and Built-In V_{MID} 70/							
71/	V_{SENSOR}	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		680		mV
			3 V		680		
	TC_{SENSOR}	ADC12ON = 1, INCH = 0Ah	2.2 V		2.25		mV/°C
			3 V		2.25		
Sample time required if channel 10 is selected 72/	$t_{SENSOR(sample)}$	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	100			µs
			3 V	100			
AV_{CC} divider at channel 11, VAV_{CC} factor	V_{MID}	ADC12ON = 1, INCH = 0Bh	2.2 V	0.48	0.5	0.52	V_{AVCC}
AVCC divider at channel 11		ADC12ON = 1, INCH = 0Bh	2.2 V	1.04	1.1	1.14	V
			3 V	1.44	1.5	1.56	
Sample time required if channel 11 is selected 73/	$t_{VMID(sample)}$	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V, 3 V	1000			ns
REF, External Reference 74/							
Positive external reference voltage input	V_{eREF+}	$V_{eREF+} > V_{REF-}/V_{eREF-}$ 75/		1.4		AV_{CC}	V
Negative external reference voltage input	V_{REF-}/V_{eREF-}	$V_{eREF+} > V_{REF-}/V_{eREF-}$ 76/		0		1.2	
Differential external reference voltage input	($V_{eREF+} - V_{REF-}/V_{eREF-}$)	$V_{eREF+} > V_{REF-}/V_{eREF-}$ 77/		1.4		AV_{CC}	
Static input current	I_{VeREF+}, I_{VREF-}/V_{eREF-}	1.4 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, Conversion rate 200 ksps	2.2 V, 3 V		±26		µA
		1.4 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, Conversion rate 200 ksps	2.2 V, 3 V	-2.5		2.5	µA
Capacitance at VREF+/-terminal	$C_{VREF+/-}$	See 78/			10		µF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{CC}		Limits		Unit
		2/		Min	Typ	Max	
REF, Built-In Reference 79/							
Positive built-in reference voltage output	V_{REF+}	REFVSEL = {2} for 2.5 V, REFON = REFOUT = 1, I_{VREF+} = 0 A	3 V		2.50	±2.5%	V
		REFVSEL = {1} for 2.0 V, REFON = REFOUT = 1, I_{VREF+} = 0 A	3 V		1.98	±2.5%	
		REFVSEL = {0} for 1.5 V, REFON = REFOUT = 1, I_{VREF+} = 0 A	2.2 V, 3 V		1.49	±2.5%	
AVCC minimum voltage, Positive built-in reference active	$AV_{CC(min)}$	REFVSEL = {0} for 1.5 V		2.2			
		REFVSEL = {1} for 2.0 V		2.3			
		REFVSEL = {2} for 2.5 V		2.8			
Operating supply current into AV_{CC} terminal 80/ 81/	I_{REF+}	ADC12SR = 1 , REFON = 1, REFOUT = 0, REFBURST = 0	3 V		70		µA
		ADC12SR = 1, REFON = 1, REFOUT = 1, REFBURST = 0	3 V		0.45		mA
		ADC12SR = 0, REFON = 1, REFOUT = 0, REFBURST = 0	3 V		210	350	µA
		ADC12SR = 0, REFON = 1, REFOUT = 1, REFBURST = 0	3 V		0.95	2	mA
Load-current regulation, VREF+ terminal 82/	$I_{L(VREF+)}$	REFVSEL = (0, 1, 2), I_{VREF+} = +10 µA/–1000 µA, AV_{CC} = $AV_{CC(min)}$ for each reference level, REFVSEL = (0, 1, 2}, REFON = REFOUT = 1			2500		µV/mA
Capacitance at VREF+ terminals	C_{VREF+}	REFON = REFOUT = 1		20		100	pF
Temperature coefficient of built-in reference 40/	TCREF+	I_{VREF+} = 0 A, REFVSEL = (0, 1, 2}, REFON = 1, REFOUT = 0 or 1			30		ppm/°C
Power supply rejection ratio (DC)	PSRR_DC	AV_{CC} = $AV_{CC(min)}$ - $AV_{CC(max)}$, T_A = 25°C, REFVSEL = (0, 1, 2}, REFON = 1, REFOUT = 0 or 1			120		µV/V
Power supply rejection ratio (AC)	PSRR_AC	AV_{CC} = $AV_{CC(min)}$ - $AV_{CC(max)}$, T_A = 25°C, f = 1 kHz, ΔVpp = 100 mV, REFVSEL = (0, 1, 2}, REFON = 1, REFOUT = 0 or 1			6.4		mV/V
Settling time of reference voltage 83/	t_{SETTLE}	AV_{CC} = $AV_{CC(min)}$ - $AV_{CC(max)}$, REFVSEL = (0, 1, 2}, REFOUT = 0, REFON = 0 → 1			75		µs
		AV_{CC} = $AV_{CC(min)}$ - $AV_{CC(max)}$, C_{VREF} = $C_{VREF(max)}$, REFVSEL = (0, 1, 2}, REFOUT = 1, REFON = 0 → 1			75		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Limits			Unit
			Min	Typ	Max	
Flash Memory						
Program or erase supply voltage	$DV_{CC(PGM/ERASE)}$		1.8		3.6	V
Average supply current from DVCC during program	I_{PGM}			3	7	mA
Average supply current from DVCC during erase	I_{ERASE}				7	mA
Average supply current from DVCC during mass erase or bank erase	I_{MERASE}, I_{BANK}				7	mA
Cumulative program time	t_{CPT}	84/			16	ms
Program and erase endurance			10^4	10^5		cycles
Data retention duration	$t_{Retention}$	T_J = 25°C	100			years
Word or byte program time	t_{Word}	85/	64		85	µs
Block program time for first byte or word	$t_{Block, 0}$	85/	49		65	
Block program time for each additional byte or word, except for last byte or word	$t_{Block, 1–(N–1)}$	85/	37		49	
Block program time for last byte or word	$t_{Block, N}$	85/	55		73	
Erase time for segment, mass erase, and bank erase (when available)	t_{Erase}	85/	23		32	ms
MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4. MGR1 = 1)	$f_{MCLK,MGR}$		0		1	MHz

Test	Symbol	Conditions 2/	V_{CC}	Limits			Unit
				Min	Typ	Max	
JTAG and Spy-Bi-Wire Interface							
Spy-Bi-Wire input frequency	f_{SBW}		2.2 V, 3 V	0		20	MHz
Spy-Bi-Wire low clock pulse length	$t_{SBW,Low}$		2.2 V, 3 V	0.025		15	µs
Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) 86/	$t_{SBW, En}$		2.2 V, 3 V			1	
Spy-Bi-Wire return to normal operation time	$t_{SBW,Rst}$			15		100	
TCK input frequency, 4-wire JTAG 87/	f_{TCK}		2.2 V	0		5	MHz
			3 V	0		10	MHz
Internal pulldown resistance on TEST	$R_{internal}$		2.2 V, 3 V	45	60	80	kΩ

See footnotes at end of table.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted).

3/ All inputs tied to 0 V or to V_{CC}. Outputs do not source or sink any current.

4/ The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

5/ Characterized with program executing typical data processing.
f_{ACLK} = 32786 Hz, f_{DCO} = f_{MCLK} = f_{SMCLK} at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

6/ Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz.

7/ Current for brownout, high side supervisor (SVS_H) normal mode included. Low side supervisor and monitors disabled (SVS_L, SVM_L). High side monitor disabled (SVM_H). RAM retention enabled.

8/ Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.

9/ Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0. (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz.

10/ Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{VLO}, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz..

11/ CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); fDCO = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz..

12/ Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz.

13/ Same parametric apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

14/ Also applies to $\overline{RST}$ pin when pullup/pulldown resistor is enabled.

15/ Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

16/ An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

17/ The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.

18/ The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

19/ The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

20/ The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

21/ Selecting reduced drive strength may reduce EMI.

22/ A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.

23/ The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

24/ To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.

25/ When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.

26/ Maximum frequency of operation of the entire device cannot be exceeded.

27/ Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
(a) For XT1DRIVEx = 0, CL,eff ≤ 6 pF
(b) For XT1DRIVEx = 1, 6 pF ≤ CL,eff ≤ 9 pF
(c) For XT1DRIVEx = 2, 6 pF ≤ CL,eff ≤ 10 pF
(d) For XT1DRIVEx = 3, CL,eff ≥ 6 pF

28/ Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

29/ Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

30/ Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

31/ Measured with logic-level input frequency but also applies to operation with crystals.

32/ This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.

33/ Oscillation allowance is based on a safety factor of 5 for recommended crystals.

34/ Requires external capacitors at both terminals. Values are specified by crystal manufacturers. In general, an effective load capacitance of up to 18 pF can be supported.

35/ Requires external capacitors at both terminals. Values are specified by crystal manufacturers. In general, an effective load capacitance of up to 18 pF can be supported.

36/ To improve EMI on the XT2 oscillator the following guidelines should be observed.
(a) Keep the traces between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
(d) Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.

37/ When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.

38/ Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

39/ Measured with logic-level input frequency but also applies to operation with crystals.

40/ Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C)).

41/ Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V).

42/ When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO}, should be set to reside within the range of $f_{DCO(n, 0),MAX} \le f_{DCO} \le f_{DCO(n, 31),MIN}$, where $f_{DCO(n, 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that theselected range is at its minimum or maximum tap setting.

43/ The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. See the Power Management Module and Supply Voltage Supervisor chapter in the MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208) on recommended settings and usage from manufacturer data sheet.

44/ The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. See the Power Management Module and Supply Voltage Supervisor chapter in the MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208) on recommended settings and usage from manufacturer data sheet.

45/ This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVSL) and low side monitor (SVML). Fastest wakeup times are possible with SVSLand SVML in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVSLand SVML while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

46/ This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVSL) and low side monitor (SVML). In this case, the SVSLand SVML are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVSLand SVML while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) from manufacturer data sheet.

47/ This value represents the time from the wakeup event to the reset vector execution.

48/ Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

49/ $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$. For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ see the SPI parameters of the attached slave.

50/ Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5 and Figure 6.

51/ Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5 and Figure 6.

52/ $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$. For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.

53/ Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5 and Figure 6.

54/ Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5 and Figure 6.

55/ The leakage current is specified by the digital I/O input leakage.

56/ The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required (see REF, External Reference and REF, Built-In Reference from manufacturer data sheet).

57/ The internal reference supply current is not included in current consumption parameter I_{ADC12_A}.

58/ ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0.

59/ REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with $f_{ADC12CLK}$ maximum of 5.0 MHz.

60/ SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1.

61/ SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.

62/ The ADC12OSC is sourced directly from MODOSC inside the UCS.

63/ 13 × ADC12DIV × $1/f_{ADC12CLK}$.

64/ Approximately ten Tau (T) are needed to get an error of less than ±0.5 LSB: $t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance.

65/ Parameters are derived using the histogram method.

66/ The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. $dVREF = V_{R+} - V_{R-}$, $V_{R+} < AV_{CC}$, $V_{R-} > AV_{SS}$. Unless otherwise mentioned, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω and two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF+/VREF- to decouple the dynamic current. See also the MSP430x5xx and MSP430x6xxFamily User's Guide (SLAU208) from manufacturer data sheet.

67/ Parameters are derived using a best fit curve.

68/ The internal reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 1. $dVREF = V_{R+} - V_{R-}$.

69/ The gain error and total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode the reference voltage used by the ADC12_A is not available on a pin.

70/ The temperature sensor is provided by the REF module. See the REF module parametric, IREF+, regarding the current consumption of the temperature sensor.

71/ The temperature sensor offset can be significant. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor. The TLV structure contains calibration values for 30°C ± 3°C and 85°C ± 3°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} * (\text{Temperature,°C}) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy. See also the MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208) from manufacturer data sheet.

72/ The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.

73/ The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

74/ The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.

75/ The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.

76/ The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.

77/ The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

78/ Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208) from manufacturer data sheet.

79/ The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger for driving the VREF+ terminal. When REFOUT = 1, the reference is available at the VREF+ terminal, as well as, used as the reference for the conversion and utilizes the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and utilizes the smaller buffer.

80/ The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.

81/ The temperature sensor is provided by the REF module. Its current is supplied via terminal AV_{CC} and is equivalent to I_{REF+} with REFON =1 and REFOUT = 0.

82/ Contribution only due to the reference and buffer including package. This does not include resistance due to PCB trace, etc.

83/ The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.

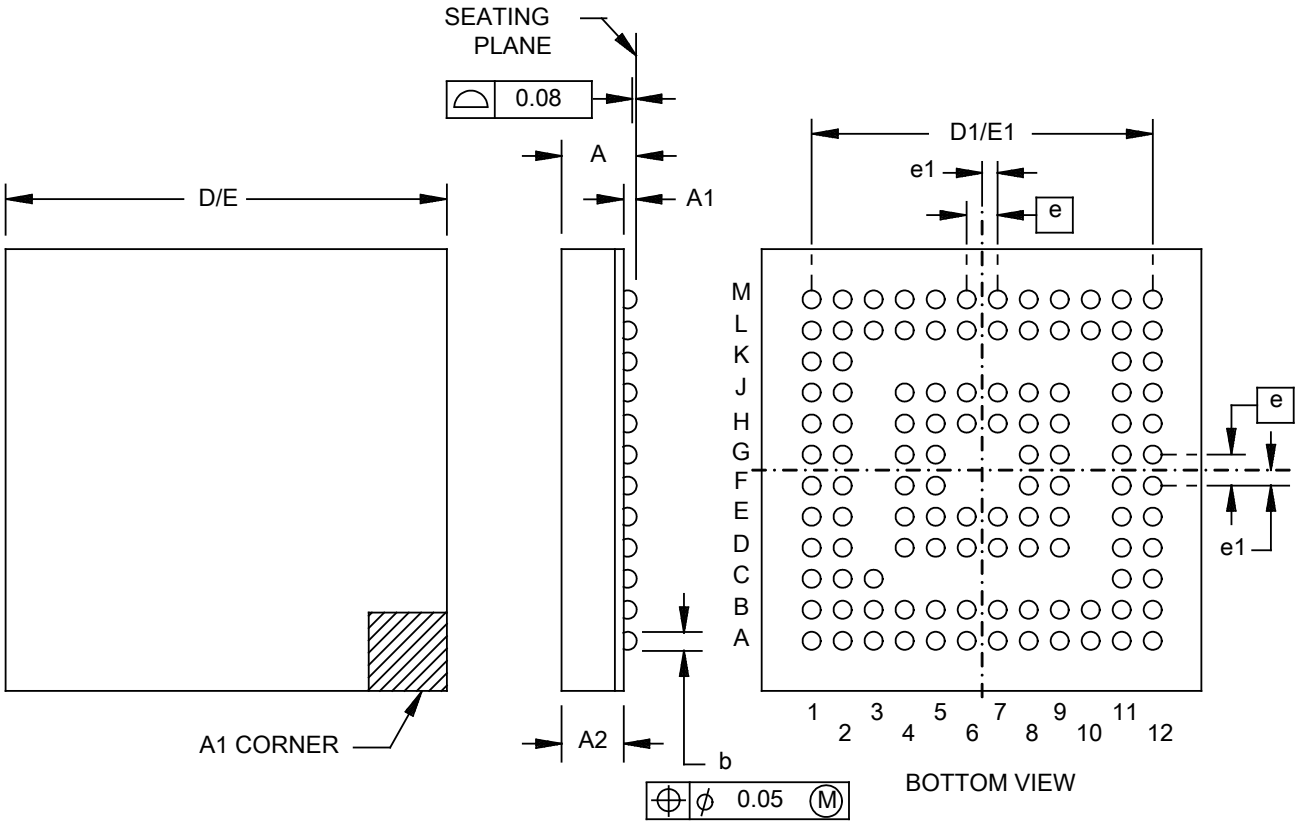
84/ The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.

85/ These values are hardwired into the flash controller's state machine.

86/ Tools accessing the Spy-Bi-Wire interface need to wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

87/ f_{TCK} may be restricted to meet the timing requirements of the module selected.

Case X

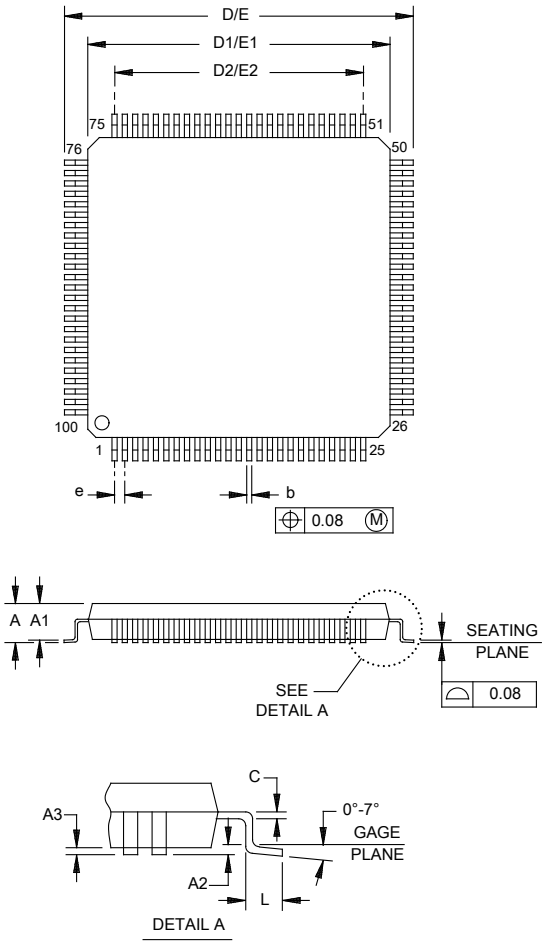


Dimensions					
Symbol	Millimeters		Symbol	Millim eters	
	Min	Max		Min	Max
A		1.00	D/E	6.90	7.10
A1	0.15	0.25	D1/E1	5.50 TYP	
A2	0.71	0.77	e	0.50 BSC	
b	0.25	0.35	e1	0.25 TYP	

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-225.

FIGURE 1. Case outline.

Case Y



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.60	D/E	15.80	16.20
A1	1.35	1.45	D1/E1	13.80	14.20
A2	0.25 TYP			12.00 TYP	
A3	0.05		e	0.50 BSC	
b	0.17	0.27	L	0.45	0.75
c	0.13 NOM				

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MS-026.

FIGURE 1. Case outline - Continued.

Case outline X

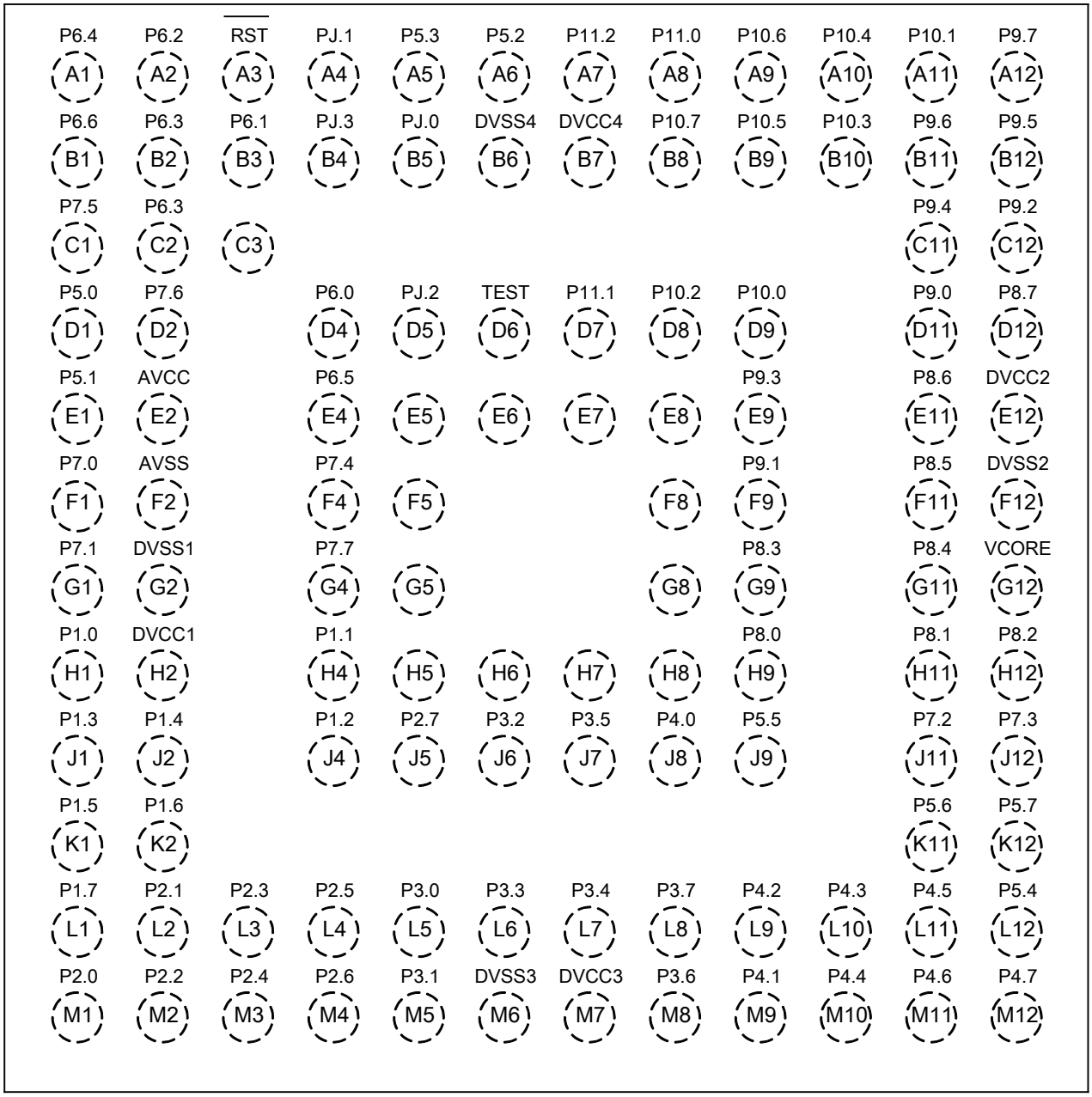


FIGURE 2. Terminal connections.

Case outline Y.

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P6.4/A4	26	P2.1/TA1.0
2	P6.5/A5	27	P2.2/TA1.1
3	P6.6/A6	28	P2.3/TA1.2
4	P6.7/A7	29	P2.4/RTCCLK
5	P7.4/A12	30	P2.5
6	P7.5/A13	31	P2.6/ACLK
7	P7.6/A14	32	P2.7/ADC12CLK/DMAE0
8	P7.7/A15	33	P3.0/UCB0STE/UCA0CLK
9	P5.0/A8/VREF+/VeREF+	34	P3.1/UCB0SIMO/UCB0SDA
10	P5.1/A9/VREF−/VeREF−	35	P3.2/UCB0SOMI/UCB0SCL
11	AVCC	36	P3.3/UCB0CLK/UCA0STE
12	AVSS	37	DVSS3
13	P7.0/XIN	38	DVCC3
14	P7.1/XOUT	39	P3.4/UCA0TXD/UCA0SIMO
15	DVSS1	40	P3.5/UCA0RXD/UCA0SOMI
16	DVCC1	41	P3.6/UCB1STE/UCA1CLK
17	P1.0/TA0CLK/ACLK	42	P3.7/UCB1SIMO/UCB1SDA
18	P1.1/TA0.0	43	P4.0/TB0.0
19	P1.2/TA0.1	44	P4.1/TB0.1
20	P1.3/TA0.2	45	P4.2/TB0.2
21	P1.4/TA0.3	46	P4.3/TB0.3
22	P1.5/TA0.4	47	P4.4/TB0.4
23	P1.6/SMCLK	48	P4.5/TB0.5
24	P1.7	49	P4.6/TB0.6
25	P2.0/TA1CLK/MCLK	50	P4.7/TB0CLK/SMCLK

FIGURE 2. Terminal connections - Continued.

Terminal number	Terminal symbol	Terminal number	Terminal symbol
51	P5.4/UCB1SOMI/UCB1SCL	76	P10.0/UCB3STE/UCA3CLK
52	P5.5/UCB1CLK/UCA1STE	77	P10.1/UCB3SIMO/UCB3SDA
53	P5.6/UCA1TXD/UCA1SIMO	78	P10.2/UCB3SOMI/UCB3SCL
54	P5.7/UCA1RXD/UCA1SOMI	79	P10.3/UCB3CLK/UCA3STE
55	P7.2/TB0OUTH/SVMOUT	80	P10.4/UCA3TXD/UCA3SIMO
56	P7.3/TA1.2	81	P10.5/UCA3RXDUCA3SOMI
57	P8.0/TA0.0	82	P10.6
58	P8.1/TA0.1	83	P10.7
59	P8.2/TA0.2	84	P11.0/ACLK
60	P8.3/TA0.3	85	P11.1/MCLK
61	P8.4/TA0.4	86	P11.2/SMCLK
62	VCORE	87	DVCC4
63	DVSS2	88	DVSS4
64	DVCC2	89	P5.2/XT2IN
65	P8.5/TA1.0	90	P5.3/XT2OUT
66	P8.6/TA1.1	91	TEST/SBWTCK
67	P8.7	92	PJ.0/TDO
68	P9.0/UCB2STE/UCA2CLK	93	PJ.1/TDI/TCLK
69	P9.1/UCB2SIMO/UCB2SDA	94	PJ.2/TMS
70	P9.2/UCB2SOMI/UCB2SCL	95	PJ.3/TCK
71	P9.3/UCB2CLK/UCA2STE	96	$\overline{\text{RST}}$/NMI/SBWTDIO
72	P9.4/UCA2TXD/UCA2SIMO	97	P6.0/A0
73	P9.5/UCA2RXDUCA2SOMI	98	P6.1/A1
74	P9.6	99	P6.2/A2
75	P9.7	100	P6.3/A3

FIGURE 2. Terminal connections - Continued.

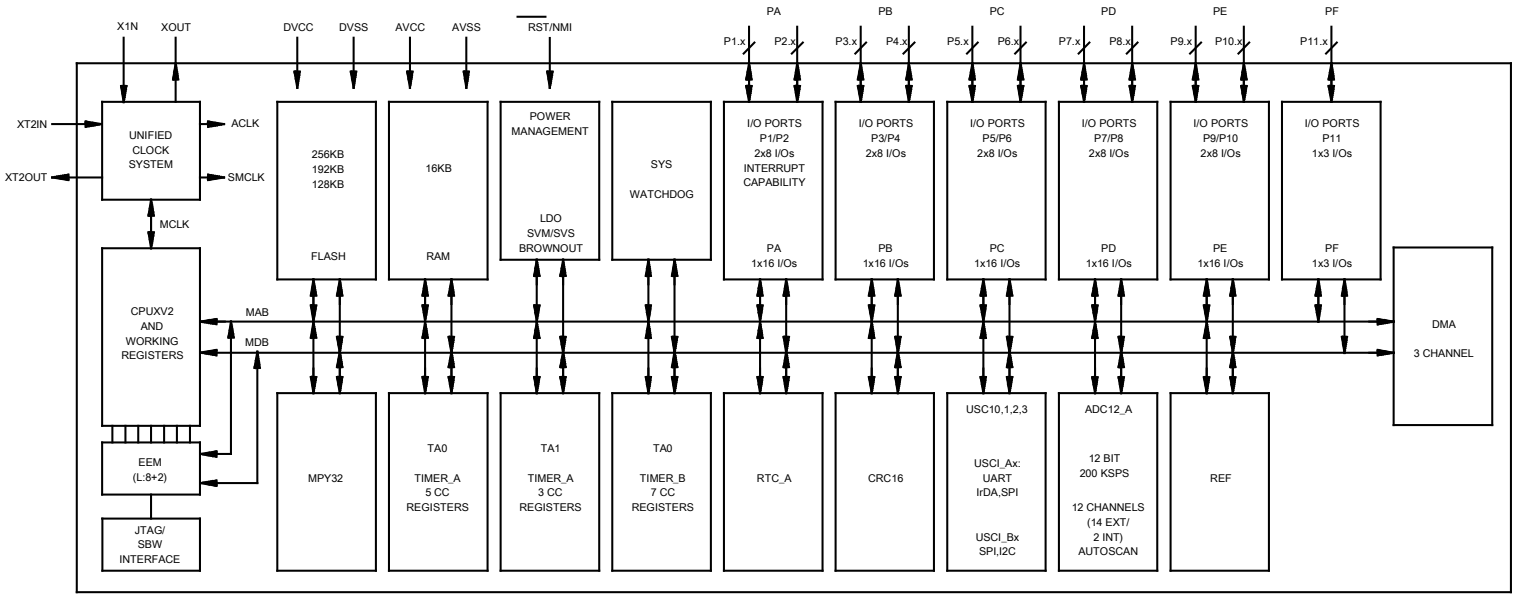


FIGURE 3. Functional block diagram.

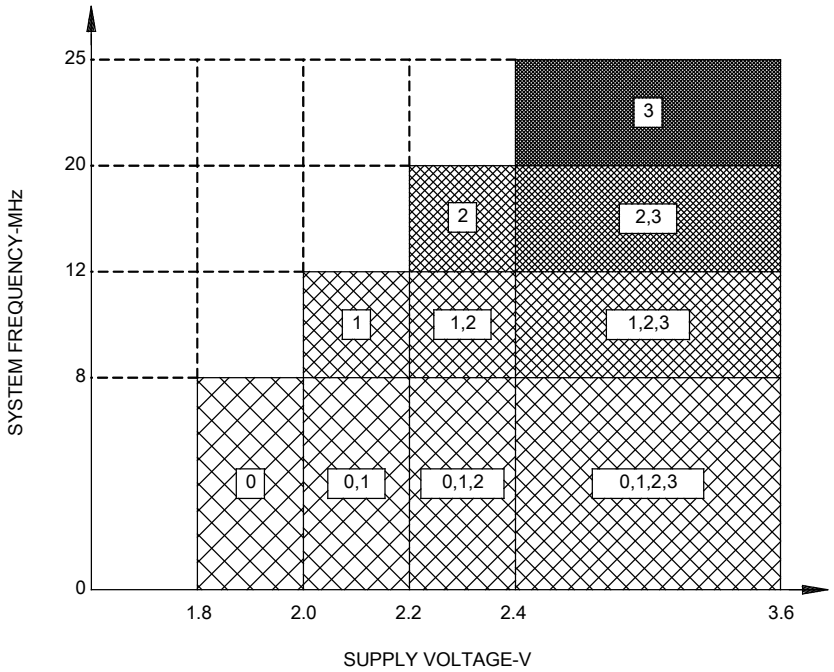


FIGURE 4. Frequency vs Supply voltage.

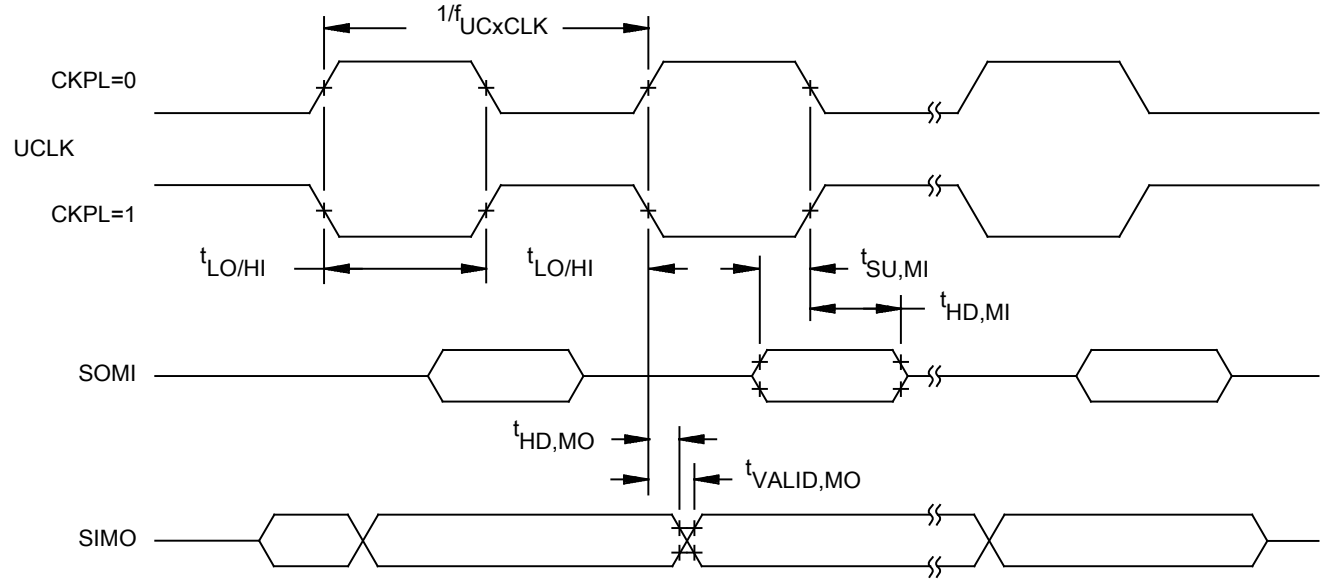


FIGURE 5. SPI master mode, CKPH = 0.

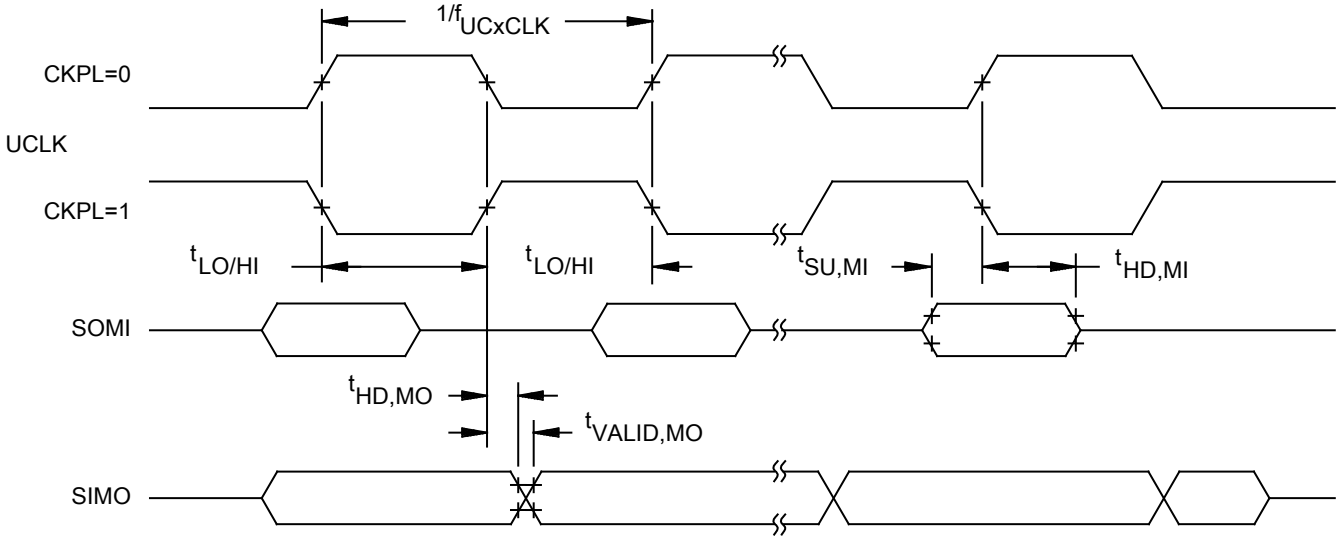


FIGURE 6. SPI master mode, CKPH = 1.

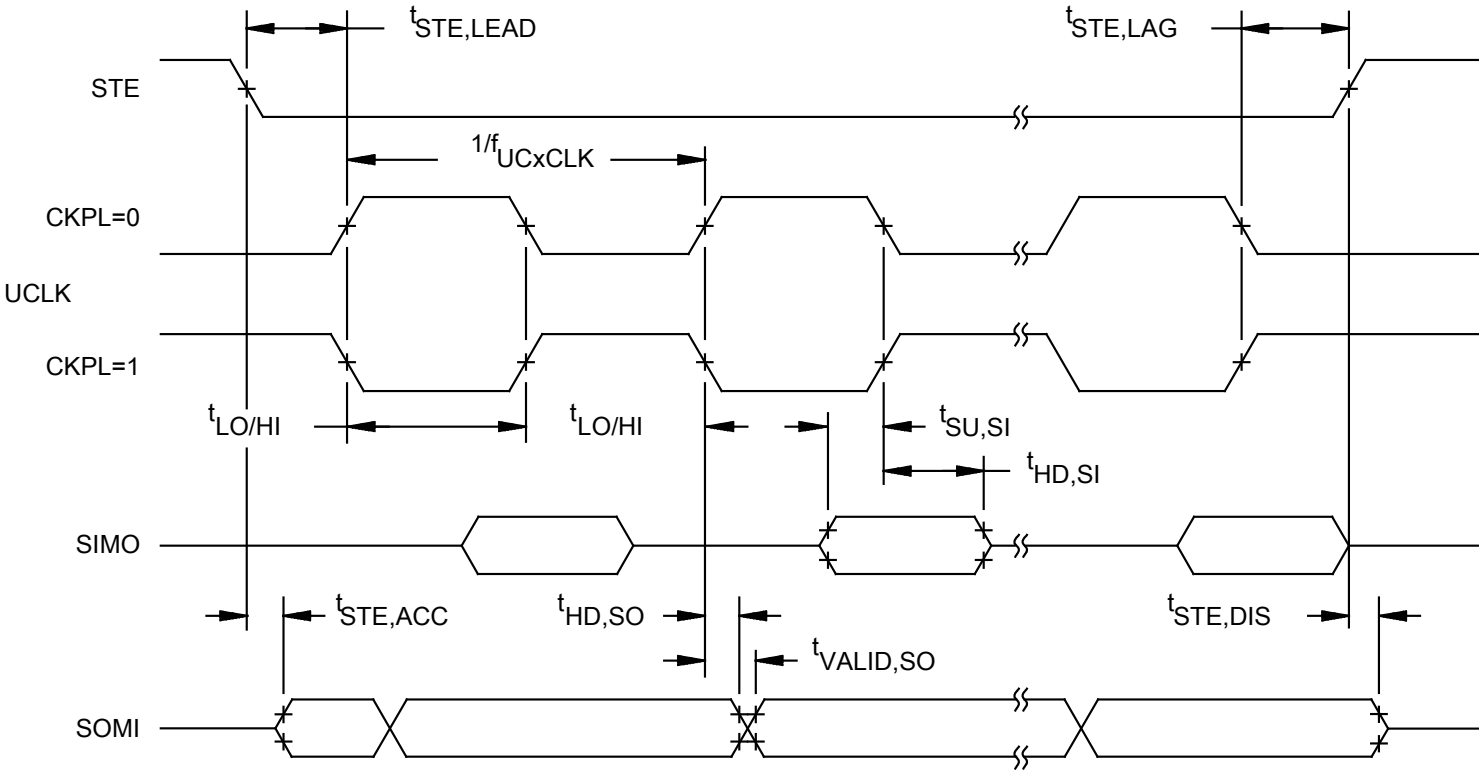


FIGURE 7. SPI slave mode, CKPH = 0.

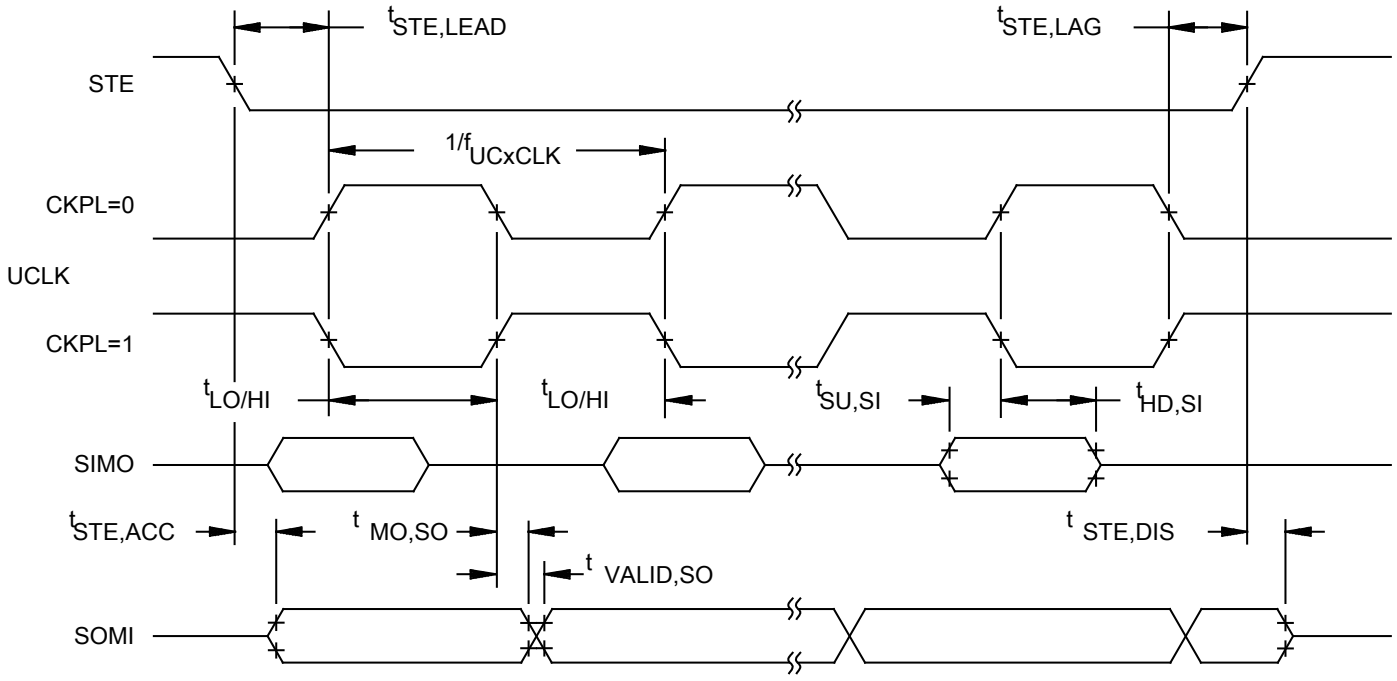


FIGURE 8. SPI slave mode, CKPH = 1.

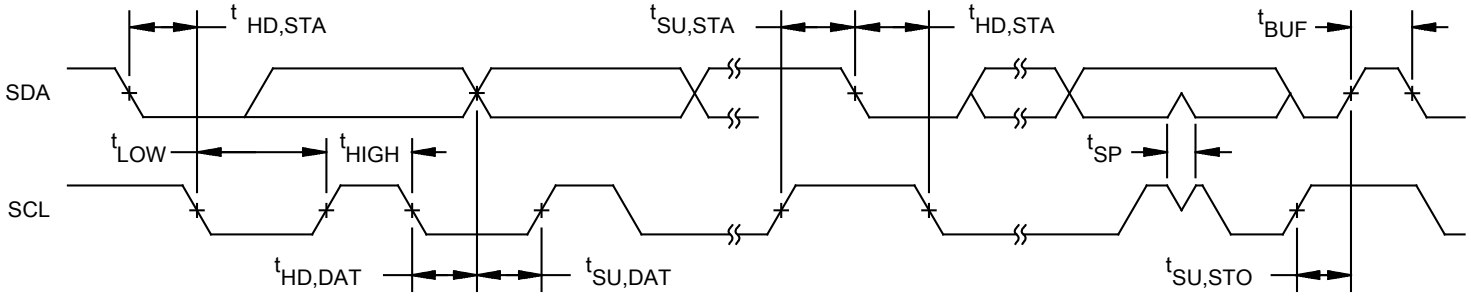


FIGURE 9. I2C mode timing.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Transport media	Vendor part number	Top Side marking
V62/14608-01XE	01295	Tape and reel	MSP430F5438AQGQWREP	MF5438AQEP
V62/14608-02XE	01295	Tube	MSP430F5438AMGQWTEP	MF5438AMEP
V62/14608-02YE	01295	Tape and reel	MSP430F5438AMPZREP	MF5438AMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243