

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single bus buffer gate with three state output microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/14605</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74AHC1G126-EP	Single bus buffer gate with three state output

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	5	MO-203-AA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 2

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7 V
Input voltage range (V_I)	-0.5 V to 7 V 2/
Output voltage range (V_O)	-0.5 V to $V_{CC} + 0.5$ V 2/
Input clamp current (I_{IK}) ($V_I < 0$)	-20 mA
Output clamp current (I_{OK}) ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 3/ 4/

Supply voltage (V_{CC})	2 V to 5.5 V
High level input voltage (V_{IH}):	
$V_{CC} = 2$ V	1.5 V minimum
$V_{CC} = 3$ V	2.1 V minimum
$V_{CC} = 5.5$ V	3.85 V minimum
Low level input voltage (V_{IL}):	
$V_{CC} = 2$ V	0.5 V maximum
$V_{CC} = 3$ V	0.9 V maximum
$V_{CC} = 5.5$ V	1.65 V maximum
Input voltage range (V_I)	0 V to 5.5 V
Output voltage range (V_O)	0 V to V_{CC}
High level output current (I_{OH}):	
$V_{CC} = 2$ V	-50 μ A maximum
$V_{CC} = 3.3 \pm 0.3$ V	-4 mA maximum
$V_{CC} = 5 \pm 0.5$ V	-8 mA maximum
Low level output current (I_{OL}):	
$V_{CC} = 2$ V	-50 μ A maximum
$V_{CC} = 3.3 \pm 0.3$ V	4 mA maximum
$V_{CC} = 5 \pm 0.5$ V	8 mA maximum

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

3/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 3

1.4 Recommended operating conditions - continued. 3/ 4/

Input transition rise or fall rate ($\Delta t/\Delta V$):

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ 100 ns/V maximum

$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ 20 ns/V maximum

Operating junction temperature range (T_J) -55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient <u>5/</u>	θ_{JA}	282.8	°C/W
Thermal resistance, junction-to-case (top) <u>6/</u>	$\theta_{JC(TOP)}$	91.1	°C/W
Thermal resistance, junction-to-board <u>7/</u>	θ_{JB}	60.1	°C/W
Characterization parameter, junction-to-top <u>8/</u>	ψ_{JT}	1.6	°C/W
Characterization parameter, junction-to-board <u>9/</u>	ψ_{JB}	59.2	°C/W

5/ The thermal resistance, junction-to-ambient under natural convection is obtained in a simulation on a JEDEC standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

6/ The thermal resistance, junction-to-case (top) is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7/ The thermal resistance, junction-to-board is obtained by simulating in an environment with a ring cold plate fixture to control the printed circuit board (PCB) temperature, as described in JESD51-8.

8/ Characterization parameter, junction-to-top (ψ_{JT}) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

9/ Characterization parameter, junction-to-board (ψ_{JB}) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 4

2. APPLICABLE DOCUMENTS

- EIA/JESD 51-2a - Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
- EIA/JEDEC 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- EIA/JESD 51-8 - Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
- JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

AMERICAN NATIONAL STANDARDS INSTITUTE

ANSI SEMI STANDARD G30-88 - Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Applications for copies should be addressed to the American National Standards Institute, Semiconductor Equipment and Materials International, 1819 L Street, NW, 6 th floor, Washington, DC 20036 or online at <http://www.ansi.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 5

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	V _{CC} = 2 V, I _{OH} = -50 μA	-55°C to +125°C	01	1.9		V
		V _{CC} = 3 V, I _{OH} = -50 μA	-55°C to +125°C		2.9		
		V _{CC} = 4.5 V, I _{OH} = -50 μA	-55°C to +125°C		4.4		
		V _{CC} = 3 V, I _{OH} = -4 mA	-55°C to +125°C		2.48		
		V _{CC} = 4.5 V, I _{OH} = -8 mA	-55°C to +125°C		3.8		
Low level output voltage	V _{OL}	V _{CC} = 2 V, I _{OL} = 50 μA	-55°C to +125°C	01		0.1	V
		V _{CC} = 3 V, I _{OL} = 50 μA	-55°C to +125°C			0.1	
		V _{CC} = 4.5 V, I _{OL} = 50 μA	-55°C to +125°C			0.1	
		V _{CC} = 3 V, I _{OL} = 4 mA	-55°C to +125°C			0.44	
		V _{CC} = 4.5 V, I _{OL} = 8 mA	-55°C to +125°C			0.44	
Input current	I _I	V _{CC} = 0 V to 5.5 V, V _I = 5.5 V or GND	-55°C to +125°C	01		±1	μA
Output impedance	I _{OZ}	V _{CC} = 5.5 V, V _O = V _{CC} or GND	-55°C to +125°C	01		±2.5	μA
Supply current	I _{CC}	V _{CC} = 5.5 V, V _I = V _{CC} or GND, I _O = 0	-55°C to +125°C	01		10	μA
Input capacitance	C _I	V _{CC} = 5 V, V _I = V _{CC} or GND	-55°C to +125°C	01		10	pF

See footnote at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 6

TABLE I. Electrical performance characteristics – Continued. 1/

Switching characteristics.						
$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$.						
Parameter	From (input)	To (output)	Load capacitance	$T_J = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
				Minimum	Maximum	
t _{PLH}	A	Y	C _L = 50 pF	1	13	ns
t _{PHL}				1	13	
t _{PZH}	OE	Y	C _L = 50 pF	1	13	ns
t _{PZL}				1	13	
t _{PHZ}	OE	Y	C _L = 50 pF	1	15	ns
t _{PLZ}				1	15	

Switching characteristics.						
$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$.						
Parameter	From (input)	To (output)	Load capacitance	$T_J = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
				Minimum	Maximum	
t _{PLH}	A	Y	C _L = 50 pF	1	8.5	ns
t _{PHL}				1	8.5	
t _{PZH}	OE	Y	C _L = 50 pF	1	8	ns
t _{PZL}				1	8	
t _{PHZ}	OE	Y	C _L = 50 pF	1	10	ns
t _{PLZ}				1	10	

Operating characteristics.			
$V_{CC} = 5 \text{ V}, T_J = +25^\circ\text{C}$			
Parameter	Test conditions	Typical	Unit
Power dissipation capacitance (C _{PD})	No load, f = 1 MHz	14	pF

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 7

Case X

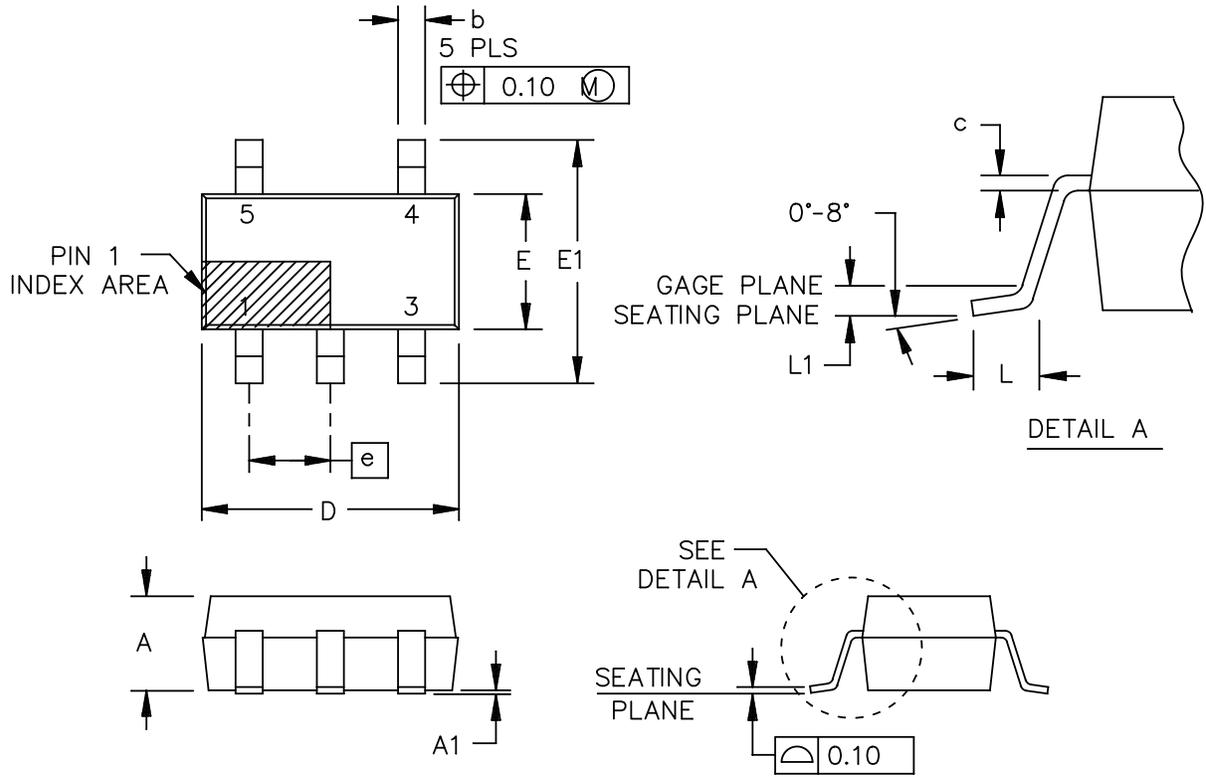


FIGURE 1. Case outline.

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/14605</p>
		<p>REV</p>	<p>PAGE 8</p>

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.031	.043	0.80	1.10
A1	.000	.003	0.00	0.10
b	.005	.011	0.15	0.30
c	.003	.008	0.08	0.22
D	.072	.084	1.85	2.15
E	.043	.055	1.10	1.40
E1	.070	.094	1.80	2.40
e	.025 BSC		0.65 BSC	
L	.010	.018	0.26	0.46
L1	.005 BSC		0.15 BSC	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm (0.005 inch) per side.
3. Falls within JEDEC MO-203-AA.

FIGURE 1. Case outline - Continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 9

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OE
2	A
3	GND
4	Y
5	V _{CC}

FIGURE 2. Terminal connections.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 10

Inputs		Output
OE	A	Y
H	H	H
H	L	L
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = Tri-state / floating

FIGURE 3. Truth table.

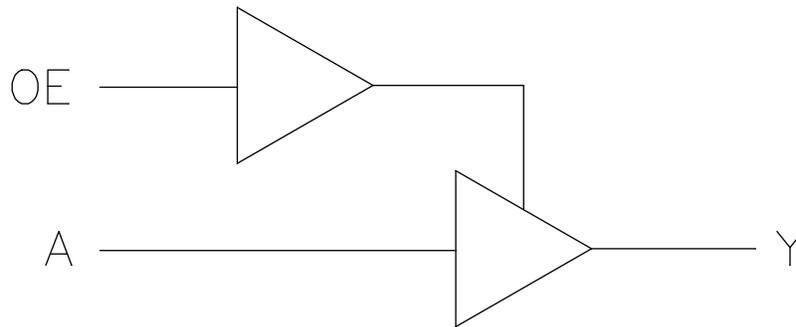
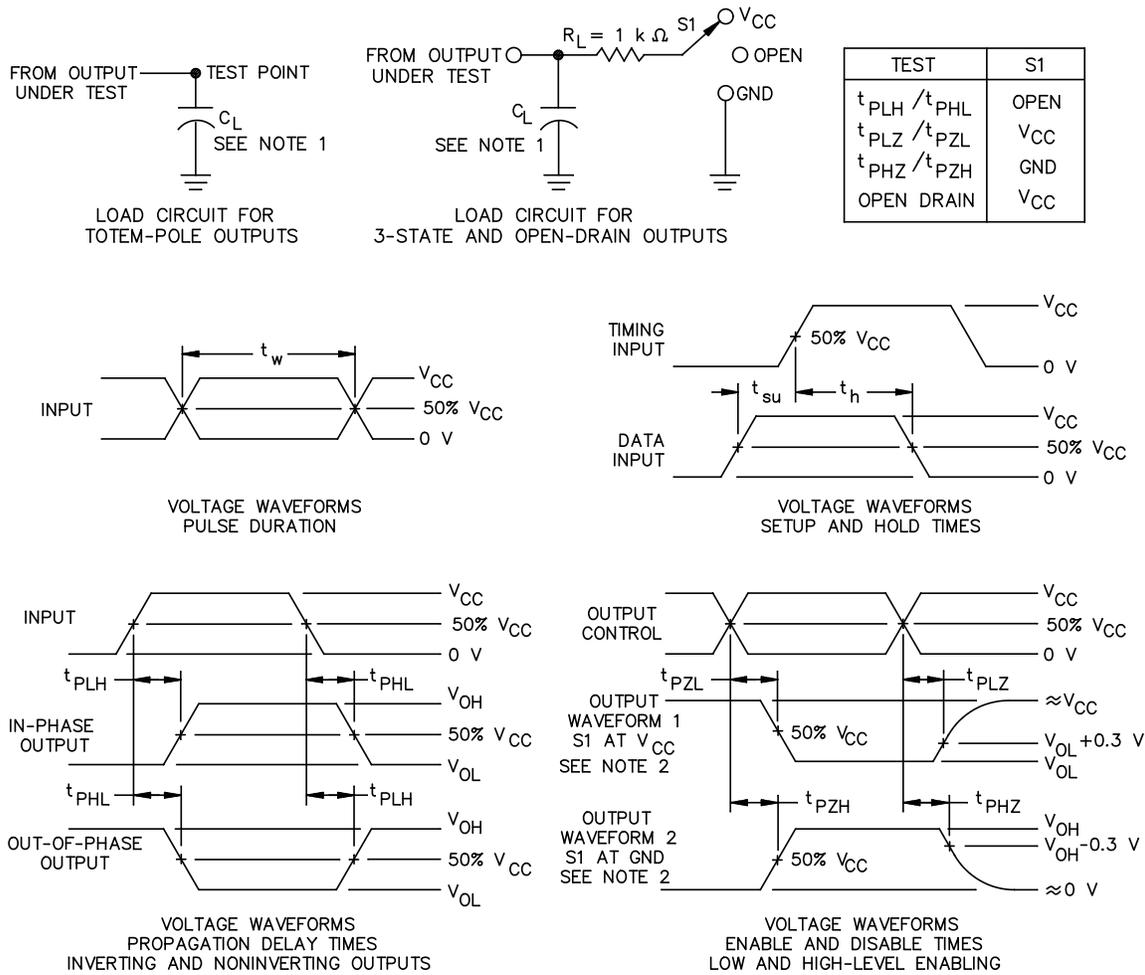


FIGURE 4. Logic diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 11



Notes:

1. C_L includes probe and jig capacitance. See table I for values.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, and $t_f \leq 3\text{ ns}$.
4. The outputs are measured one at a time with one input transition per measurement.
5. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Timing waveforms and test circuit.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 12

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u> <u>2/</u> <u>3/</u>	Device manufacturer CAGE code	Transportation mode and quantity	Top side marking	Vendor part number
V62/14605-01XE	01295	Reel of 250	SLI	SN74HC1G126MDCKTEP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.
- 3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/14605
		REV	PAGE 13