| REVISIONS | | | |
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| LTR | DESCRIPTION | DATE | APPROVED |
| A | Update document paragraph to current requirements. - ro | 20-02-04 | J. ESCHMEYER |

Prepared in accordance with ASME Y14.24

Vendor item drawing

| | | | | | | | | | | | | | | | | | | | | | |
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| REV STATUS OF PAGES | REV | | A | A | A | A | A | A | A | A | A | A | A | | | | | | | | |
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| PMIC N/A | PREPARED BY<br>RICK OFFICER | DLA LAND AND MARITIME<br>COLUMBUS, OHIO 43218-3990<br>https://www.dla.mil/LandandMaritime |
| Original date of drawing<br>YY-MM-DD<br>14-03-04 | CHECKED BY<br>RAJESH PITHADIA<br>APPROVED BY<br>CHARLES F. SAFFLE | TITLE<br>MICROCIRCUIT, LINEAR, HIGH INPUT VOLTAGE BUCK BOOST CONVERTER WITH 2 AMP SWITCH CURRENT, MONOLITHIC SILICON |
| | SIZE<br>A<br>CODE IDENT. NO.<br>16236 | DWG NO.<br>V62/14602 |
| | REV A | PAGE 1 OF 11 |

1. SCOPE

Scope. This drawing documents the general requirements of a high performance high input voltage buck boost converter with 2 amp switch current microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/14602 | - | 01 | X | E |
|---|---|---|---|---|
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| Device type | Generic | Circuit function |
|---|---|---|
| 01 | TPS63060-EP | High input voltage buck boost converter with 2 amp switch current |

1.2.2 Case outline(s). The case outline(s) are as specified herein.

| Outline letter | Number of pins | JEDEC PUB 95 | Package style |
|---|---|---|---|
| X | 10 | See figure 1 | Plastic square leadless small outline with thermal pad |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| F | Tin-lead alloy (BGA/CGA) |
| Z | Other |

1.3 Absolute maximum ratings. 1/

Supply voltage range ($V_{CC}$) :
VIN, VOUT, PS/SYNC, EN, FB ..... -0.3 V to 17 V
L1, L2 ..... -0.3 V to $V_{IN}$ + 0.3 V
FB, VAUX ..... -0.3 V to 7.5 V
Operating virtual junction temperature range ($T_J$) ..... -55°C to +150°C
Storage temperature range ($T_{STG}$) ..... -65°C to +150°C
Electrostatic discharge (ESD): 2/
Human body model (HBM) ..... 3 kV maximum
Machine model (MM) ..... 200 V maximum
Charge device model (CDM) ..... 1.5 kV maximum

1.4 Recommended operating conditions. 3/

Supply voltage at $V_{IN}$ ..... 2.5 V to 12 V
Output current ($I_{OUT}$) with $V_{IN}$ = 10 V to 12 V ..... 1 Amp
Operating junction temperature range ($T_J$) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ ESD testing is performed according to the respective JESD22 JEDEC standard.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

1.5 Thermal characteristics.

| Thermal metric | Symbol | Case X | Unit |
|---|---|---|---|
| Thermal resistance, junction-to-ambient 4/ | $\theta_{JA}$ | 48.7 | °C/W |
| Thermal resistance, junction-to-case (top) 5/ | $\theta_{JC(TOP)}$ | 54.8 | °C/W |
| Thermal resistance, junction-to-board 6/ | $\theta_{JB}$ | 19.8 | °C/W |
| Characterization parameter, junction-to-top 7/ | $\psi_{JT}$ | 1.1 | °C/W |
| Characterization parameter, junction-to-board 8/ | $\psi_{JB}$ | 19.6 | °C/W |
| Thermal resistance, junction-to-case (bottom) 9/ | $\theta_{JC(BOTTOM)}$ | 4.2 | °C/W |

4/ The thermal resistance, junction-to-ambient under natural convection is obtained in a simulation on a JEDEC standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

5/ The thermal resistance, junction-to-case (top) is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6/ The thermal resistance, junction-to-board is obtained by simulating in an environment with a ring cold plate fixture to control the printed circuit board (PCB) temperature, as described in JESD51-8.

7/ Characterization parameter, junction-to-top ($\psi_{JT}$ ) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

8/ Characterization parameter, junction-to-board ($\psi_{JB}$ ) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

9/ The thermal resistance, junction-to-case (bottom) is obtained by simulating a cold plate test on the exposed power pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE, SEMICONDUCTOR EQUIPMENT and MATERIALS INTERNATIONAL

ANSI SEMI STANDARD G30-88 - Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Applications for copies are available online at https://www.ansi.org.)

JEDEC Solid State Technology Association

| | | |
|---|---|---|
| EIA/JESD 22 | – | Qualification Testing for Plastic Encapsulated Solid State Devices |
| EIA/JESD51-2a | – | Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air) |
| EIA/JEDEC 51-7 | – | High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages |
| EIA/JESD51-8 | – | Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board |
| JEDEC PUB 95 | – | Registered and Standard Outlines for Semiconductor Devices |

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions | Temperature, $T_J$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| DC/DC stage | | | | | | | |
| Input voltage range | $V_{IN}$ | | -55°C to +125°C | 01 | 2.5 | 12 | V |
| Minimum input voltage for startup | $V_{IIN}$ | | -55°C to +125°C | 01 | | 2.5 | V |
| Output voltage range | $V_{OUT}$ | | -55°C to +125°C | 01 | 2.5 | 8 | V |
| Minimum duty cycle in step down conversion | | | -55°C to +125°C | 01 | | 20% | |
| | | | +25°C | | 10% typical | | |
| Feedback voltage | $V_{FB}$ | PS/SYNC = $V_{IN}$ | -55°C to +125°C | 01 | 495 | 505 | mV |
| | | | +25°C | | 500 typical | | |
| | | PS/SYNC = GND referenced to 500 mV | -55°C to +125°C | | 0.6% | 6% | |
| Oscillator frequency | $f_{OSC}$ | | -55°C to +125°C | 01 | 1850 | 3000 | kHz |
| | | | | | 2400 typical | | |
| Frequency range for synchronization | $f_{SYN}$ | | -55°C to +125°C | 01 | 2200 | 2600 | kHz |
| | | | | | 2400 typical | | |
| Average inductance current limit | $I_{SW}$ | $V_{IN}$ = 5 V | +25°C | 01 | 2000 | 2500 | mA |
| | | | | | 2250 typical | | |
| High side switch on resistance | | $V_{IN}$ = 5 V | +25°C | 01 | 90 typical | | mΩ |
| Low side switch on resistance | | $V_{IN}$ = 5 V | +25°C | 01 | 95 typical | | mΩ |
| Line regulation | | Power save mode disabled | +25°C | 01 | 0.5% typical | | |
| Load regulation | | Power save mode disabled | +25°C | 01 | 0.5% typical | | |
| Quiescent current, $V_{IN}$ | $I_Q$ | $I_O$ = 0 mA, $V_{OUT}$ = 5 V, $V_{EN}$ = $V_{IN}$ = 5 V | -55°C to +125°C | 01 | | 64 | µA |
| | | | +25°C | | 30 typical | | |
| Quiescent current, $V_{OUT}$ | $I_Q$ | $I_O$ = 0 mA, $V_{OUT}$ = 5 V, $V_{EN}$ = $V_{IN}$ = 5 V | -55°C to +125°C | 01 | | 28 | µA |
| | | | +25°C | | 7 typical | | |

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions | Temperature, $T_J$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| DC/DC stage – continued. | | | | | | | |
| Shutdown current | $I_S$ | $V_{EN}$ = 0 V, $V_{IN}$ = 5 V | -55°C to +125°C | 01 | | 2 | µA |
| | | | +25°C | | 0.3 typical | | |
| Control stage | | | | | | | |
| Maximum bias voltage | $V_{AUX}$ | $V_{IN} > V_{OUT}$ | -55°C to +125°C | 01 | $V_{IN}$ | 7 | V |
| | | $V_{IN} < V_{OUT}$ | | | $V_{OUT}$ | 7 | |
| Load current at $V_{AUX}$ | $I_{AUX}$ | | -55°C to +125°C | 01 | | 1 | mA |
| Under voltage lockout threshold | UVLO | $V_{IN}$ voltage decreasing | -55°C to +125°C | 01 | 1.8 | 2.2 | V |
| | | | | | 1.9 typical | | |
| UVLO hysteresis | | | +25°C | 01 | 300 typical | | mV |
| EN, PS/SYNC input low voltage | VIL | | -55°C to +125°C | 01 | | 0.4 | V |
| EN, PS/SYNC input high voltage | $V_{IH}$ | | -55°C to +125°C | 01 | 1.2 | | V |
| EN, PS/SYNC input current | | Clamped on GND or $V_{IN}$ | -55°C to +125°C | 01 | | 0.2 | µA |
| | | | +25°C | | 0.01 typical | | |
| PG output low voltage | | $V_{OUT}$ = 5 V, $I_{PGL}$ = 10 µA | -55°C to +125°C | 01 | | 0.4 | V |
| | | | +25°C | | 0.04 typical | | |
| PG output leakage current | | | -55°C to +125°C | 01 | | 0.1 | µA |
| | | | +25°C | | 0.01 typical | | |
| Output overvoltage protection | | | -55°C to +125°C | 01 | 12 | 16 | V |
| Overtemperature protection | | | +25°C | 01 | 140 typical | | °C |
| Overtemperature hysteresis | | | +25°C | 01 | 20 typical | | °C |

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X

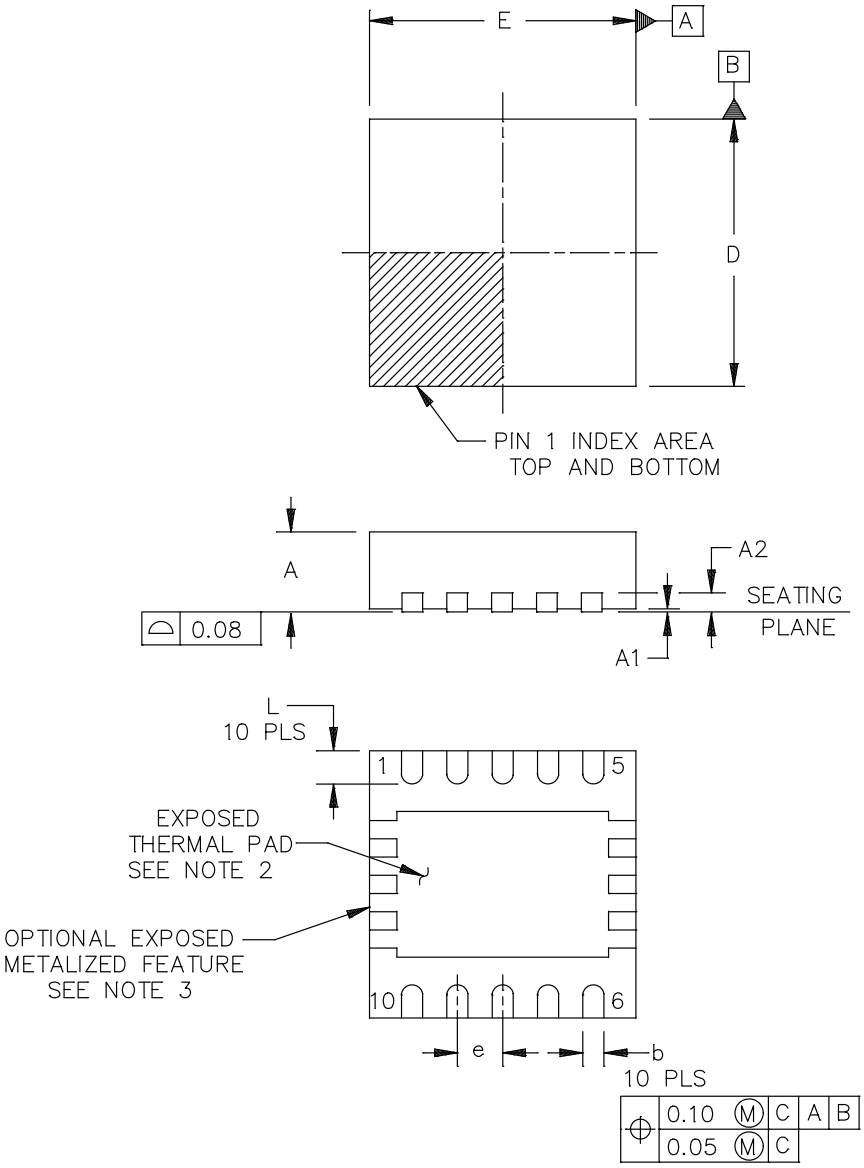


FIGURE 1. Case outline.

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | .023 | .031 | 0.60 | 0.80 |
| A1 | .000 | .001 | 0.00 | 0.05 |
| A2 | .0078 REF | | 0.20 REF | |
| b | .0070 | .011 | 0.18 | 0.30 |
| D | .112 | .124 | 2.85 | 3.15 |
| E | .112 | .124 | 2.85 | 3.15 |
| e | .019 BSC | | 0.50 BSC | |
| L | .011 | .019 | 0.30 | 0.50 |

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The package thermal pad must be soldered to the board for thermal and mechanical performance.
3. See product data sheet for details regarding the exposed thermal pad features and dimensions.

FIGURE 1. Case outline - continued.

| Device type | 01 | | |
|---|---|---|---|
| Case outline | X | | |
| Terminal number | Terminal symbol | I/O | Description |
| 1 | L1 | I | Connection for inductor. |
| 2 | $V_{IN}$ | I | Supply voltage for power stage. |
| 3 | EN | I | Enable input. (1 enabled, 0 disabled) |
| 4 | PS/SYNC | I | Enable/disable power save mode (1 disabled, 0 enabled, clock signal for synchronization) |
| 5 | PG | O | Output power good (1 good, 0 failure; open drain) |
| 6 | $V_{AUX}$ | --- | Connection for capacitor. |
| 7 | GND | --- | Control / logic ground. |
| 8 | FB | I | Voltage feedback of adjustable versions, must be connected to $V_{OUT}$ on fixed output voltage versions. |
| 9 | $V_{OUT}$ | O | Buck boost converter output. |
| 10 | L2 | I | Connection for inductor. |
| Thermal pad | --- | --- | Must be soldered to achieve appropriate power dissipation. Must be connected to PGND. |

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

| Vendor item drawing administrative control number 1/ 2/ 3/ | Device manufacturer CAGE code | Top side marking | Vendor part number |
|---|---|---|---|
| V62/14602-01XE | 01295 | TPS63060MDSCTEP | TPS63060MDSCTEP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

| CAGE code | Source of supply |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Lane<br>P.O. Box 660199<br>Dallas, TX 75243 |