

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add Device 02. Correct operating junction temperature range T_J in section 1.3. Add temperature test conditions in Table I.	15-04-03	Thomas M. Hess
B	Change Devices Lead Finish to "F". Update boilerplate to current MIL-PRF-38535 requirements. - PHN	17-08-25	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - PHN	23-05-22	Muhammad A. Akbar



**CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990**

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV	C	C	C																			
SHEET	45	46	47																			
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil/
Original date of drawing YY MM DD 14-08-14	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, DIGITAL, 16 AND 32 BIT RISC FLASH MICROCONTROLLER, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A	CAGE CODE 16236
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16 and 32 bit RISC Flash microcontroller microcircuit, with an operating temperature range of -40°C to +125°C (Device 01) and -55°C to +125°C (Device 02) .

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/13629</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Operating Temp</u>	<u>Circuit function</u>
01	TMS570LS3137 -EP	-40°C to +125°C	16 and 32 bit RISC Flash microcontroller
02	TMS570LS3137 -EP	-55°C to +125°C	16 and 32 bit RISC Flash microcontroller

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	337	JEDEC MO-275	Plastic Ball Grid Array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA) <u>1/</u>
Z	Other

1/ Devices listed on this drawing are supplied to lead finish "F". The solder ball material contains compositions of: Sn = 63%, Pb = 34.5%, Ag = 2%, and Sb = 0.5% .

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1.3 Absolute maximum ratings. 2/

Supply voltage range:		
V _{CC}	-0.3 V to 1.43 V	3/
V _{CCIO} , V _{CCP}	-0.3 V to 4.6 V	3/
V _{CCAD}	-0.3 V to 5.5 V	
Input voltage range:		
All input pins	-0.3 V to 4.6 V	
ADC input pins	-0.3 V to 5.5 V	
Input clamp current:		
I _{IK} (V _I < 0 or V _I > V _{CCIO}) All pins, except AD1IN[23:0] and AD2IN[15:0]	±20 mA	
I _{IK} (V _I < 0 or V _I > V _{CCAD}) AD1IN[23:0] and AD2IN[15:0]	±10 mA	
Operating junction temperature range, (T _J)		
Device 01	-40°C to 150°C	
Device 02	-55°C to 150°C	
Storage temperature range, (T _{stg})		-65°C to 150°C

1.4 Recommended operating conditions. 4/

Digital logic supply voltage (Core) (V _{CC})	1.14 V to 1.32 V
PLL supply voltage, (V _{CCPLL})	1.14 V to 1.32 V
Digital logic supply voltage (I/O) (V _{CCIO})	3.0 V to 3.6 V
MibADC supply voltage, (V _{CCAD})	3.0 V to 5.25 V
Flash pump supply voltage (V _{CCP})	3.0 V to 3.6 V
Digital logic supply ground (V _{SS})	0 V
MibADC supply ground (V _{SSAD})	-0.1 V to 0.1 V
A to D high voltage reference source (V _{ADREFHI})	V _{SSAD} to V _{CCAD}
A to D low voltage reference source (V _{ADREFLO})	V _{SSAD} to V _{CCAD}
Maximum positive slew rate for all supplies (V _{SLEW})	10 ⁵ V/s
Operating free air temperature (T _A)	
Device 01	-40°C to +125°C
Device 02	-55°C to +125°C
Operating junction temperature (T _J)	
Device 01	-40°C to +125°C
Device 02	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org>).

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE 802.3... – Defines the MAC layer for bus networks that use CSMA/CD.

(Copies of these documents are available online at <http://www.ieee.org>).

- 2/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- 3/ Maximum -rated conditions for extended periods may affect device reliability. All voltage values are with respect to their associated grounds.
- 4/ All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}.
- 5/ Reliability data is based upon a temperature profile that is equivalent to 100,000 power-on hours at 105°C junction temperature.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 TTL-level inputs. The TTL level inputs shall be as shown in figure 4.

3.5.5 CMOS level outputs. The CMOS level output shall be as shown in figure 5.

3.5.6 nPORRST timing diagram. The nPORRST timing diagram shall be as shown in figure 6.

3.5.7 Asynchronous memory Read timing. The asynchronous memory Reading timing shall be as shown in figure 7.

3.5.8 EMIFnWAIT Read timing requirements. The EMIFnWAIT Read timing requirements shall be as shown in figure 8.

3.5.9 Asynchronous memory Write timing. The Asynchronous memory Write timing shall be as shown in figure 9.

3.5.10 EMIFnWAIT Write timing requirements. The EMIFnWAIT Write timing requirements shall be as shown in figure 10.

3.5.11 Basic SDRAM Read operation. The basic SDRAM Read operation shall be as shown in figure 11.

3.5.12 Basic SDRAM Write operation. The basic SDRAM Write operation shall be as shown in figure 12.

3.5.13 JTAG timing. The JTAG timing shall be as shown in figure 13.

3.5.14 ETMTRACECLKOUT timing. The ETMTRACECLKOUT timing shall be as shown in figure 14.

3.5.15 ETMDATA timing. The ETMDATA timing shall be as shown in figure 15.

3.5.16 RTPCLK timing. The RTPCLK timing shall be as shown in figure 16.

3.5.17 RTPDATA timing. The RTPDATA timing shall be as shown in figure 17.

3.5.18 RTPnENA timing. The RTPnENA timing shall be as shown in figure 18.

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- 3.5.19 DMMCLK timing. The DMMCLK timing shall be as shown in figure 19.
- 3.5.20 DMMDATA timing. The DMMDATA timing shall be as shown in figure 20.
- 3.5.21 DMMnENA timing. The DMMnENA timing shall be as shown in figure 21.
- 3.5.22 MibADC input equivalent circuit. The MibADC input equivalent circuit shall be as shown in figure 22.
- 3.5.23 N2HET input capture timings. The N2HET input capture timings shall be as shown in figure 23.
- 3.5.24 FlexRay inputs. The FlexRay inputs shall be as shown in figure 24.
- 3.5.25 I2C timings. The I2C timings shall be as shown in figure 25.
- 3.5.26 SPI Master mode external timing (Clock phase = 0). The SPI Master mode external timing (CLOCK phase = 0) shall be as shown in figure 26.
- 3.5.27 SPI Master mode chip select timing (Clock phase = 0). The SPI Master mode chip select timing (CLOCK phase = 0) shall be as shown in figure 27.
- 3.5.28 SPI Master mode external timing (Clock phase = 1). The SPI Master mode external timing (CLOCK phase = 1) shall be as shown in figure 28.
- 3.5.29 SPI Master mode chip select timing (Clock phase = 0). The SPI Master mode chip select timing (CLOCK phase = 0) shall be as shown in figure 29.
- 3.5.30 SPI Slave mode external timing (Clock phase = 0). The SPI Slave mode external timing (CLOCK phase = 0) shall be as shown in figure 30.
- 3.5.31 SPI Slave mode Enable timing (Clock phase = 0). The SPI Slave mode Enable timing (CLOCK phase = 0) shall be as shown in figure 31.
- 3.5.32 SPI Slave mode external timing (Clock phase = 1). The SPI Slave mode external timing (CLOCK phase = 1) shall be as shown in figure 32.
- 3.5.33 SPI Slave mode Enable timing (Clock phase = 1). The SPI Slave mode Enable timing (CLOCK phase = 1) shall be as shown in figure 33.
- 3.5.34 MII Receive timing. The MII Receive timing shall be as shown in figure 34.
- 3.5.35 MII Transmit timing. The MII Transmit timing shall be as shown in figure 35.
- 3.5.36 RMII timing diagram. The RMII timing diagram shall be as shown in figure 36.
- 3.5.37 MDIO input timing. The MDIO input timing shall be as shown in figure 37.
- 3.5.38 MDIO output timing. The MDIO output timing shall be as shown in figure 38.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
SWITCHING CHARACTERISTICS FOR CLOCK DOMAINS						
Clock domain timing specifications						
HCLK – System clock frequency	f _{HCLK}	Pipeline mode enabled			180	MHz
		Pipeline mode disabled			50	
GCLK – CPU clock frequency	f _{GCLK}				f _{HCLK}	
VCLK - Primary peripheral clock frequency	f _{VCLK}				100	
VCLK2 - Secondary peripheral clock frequency	f _{VCLK2}				100	
VCLK3 - Secondary peripheral clock frequency	f _{VCLK3}				100	
VCLKA1 - Primary asynchronous peripheral clock frequency	f _{VCLKA1}				100	
VCLKA2 - Secondary asynchronous peripheral clock frequency	f _{VCLKA2}				100	
VCLKA4 - Secondary asynchronous peripheral clock frequency	f _{VCLKA4}				50	
RTICKL - clock frequency	f _{RTICKL}				f _{VCLK}	
Power consumption						
V _{CC} Digital supply current (operating mode)	I _{CC} , I _{CCPLL}	f _{HCLK} = 180 MHz, f _{VCLK} = 90 MHz, Flash in pipelined mode, V _{CCmax}		220 3/	440 4/	mA
V _{CC} Digital supply current (LBIST mode)		LBIST clock rate = 90 MHz			700 5/ 6/	
V _{CC} Digital supply current (PBIST mode)		PBIST ROM clock frequency = 90 MHz			700 5/ 6/	
V _{CC} Digital supply current (operating mode)		f _{HCLK} = 160 MHz, f _{VCLK} = 80MHz, Flash in pipelined mode, V _{CCmax}		200 3/	420 4/	
V _{CC} Digital supply current (LBIST mode)		LBIST clock rate = 80 MHz			665 5/ 6/	
V _{CC} Digital supply current (PBIST mode)		PBIST ROM clock frequency = 80 MHz			665 5/ 6/	
V _{CCIO} supply current (operating mode).	I _{CCIO}	No DC load, V _{CCmax}			10	
V _{CCAD} supply current (operating mode)	I _{CCAD}	Single ADC operational, V _{CCADmax}			15	
		Both ADCs operational, V _{CCADmax}			30	
AD _{REFHI} supply current (operating mode)	I _{CCREFHI}	Single ADC operational, AD _{REFHI} max			3	
		Both ADCs operational, AD _{REFHI} max			6	
V _{CCP} pump supply current	I _{CCP}	Read from 1 bank and program or erase another bank, V _{CCPmax}			60	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit		
			Min	Typ	Max			
Input/Output electrical characteristics 7/								
Low level output voltage	V _{OL}	I _{OL} = I _{OLmax}			0.2 V _{CCIO}	V		
		I _{OL} = 50 μA, standard output mode			0.2			
		I _{OL} = 50 μA, low-EMI output mode 8/			0.2 V _{CCIO}			
High level output voltage	V _{OH}	I _{OH} = I _{OHmax}	0.8 V _{CCIO}					
		I _{OH} = 50 μA, standard output mode	V _{CCIO} - 0.3					
		I _{OH} = 50 μA, low-EMI output mode 8/	0.8 V _{CCIO}					
Input clamp current (I/O pins)	I _{IC}	V _I < V _{SSIO} - 0.3 or V _I > V _{CCIO} + 0.3	-3.5		3.5	mA		
Input current (I/O pins)	I _{IH} Pulldown 20 μA	V _I = V _{CCIO}	01	5		40	μA	
			02	5		40		
	I _{IH} Pulldown 100 μA	V _I = V _{CCIO}	01	40		195		
			02	30		195		
	I _{IL} Pullup 20 μA	V _I = V _{SS}	01	-40		-5		
			02	-60		-2		
	I _{IL} Pullup 100 μA	V _I = V _{SS}	01	-195		-40		
			02	-195		-40		
	All other pins	No pullup or pulldown	01	-1		1		
			02	-1.5		1.5		
	Input capacitance	C _I		01		2		pF
				02		2		
Output capacitance	C _O		01		3			
			02		3			

INPUT TIMING

Timing requirements for inputs 9/ see FIGURE 4

Input minimum pulse width 10/	t _{pw}	2/	t _{c(VCLK)} + 10	ns

Output timings

Switching characteristics for output timings versus Load capacitance C_L

Rise time	t _r	8 mA low EMI pins	T _A = T _J = -40°C to 125°C	C _L = 15 pF	2.5	ns	
				C _L = 50 pF	4		
				C _L = 100 pF	7.2		
				T _A = T _J = -55°C to 125°C	C _L = 150 pF	12.5	
Fall time	t _f	11/	T _A = T _J = -40°C to 125°C	C _L = 15 pF	2.5		
				C _L = 50 pF	4		
				C _L = 100 pF	7.2		
				C _L = 150 pF	12.5		
				4 mA low	T _A = T _J = -40°C to 125°C	C _L = 15 pF	5.6
						C _L = 50 pF	10.4
C _L = 100 pF	16.8						
Rise time	t _r			C _L = 150 pF	23.2		
				EMI pins 11/	T _A = T _J = -40°C to 125°C	C _L = 15 pF	5.6
						C _L = 50 pF	10.4
C _L = 100 pF	16.8						
Fall time	t _f			C _L = 150 pF	23.2		
					T _A = T _J = -55°C to 125°C	C _L = 15 pF	5.6
						C _L = 50 pF	10.4
C _L = 100 pF	16.8						
				C _L = 150 pF	23.2		

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition <u>2/</u>	Limits			Unit
			Min	Typ	Max	

Output timings-Continued

Switching characteristics for output timings versus Load capacitance C_L – Continued

Rise time	t_r	2 mA-z low EMI pins <u>11/</u>		$T_A = T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$C_L = 15 \text{ pF}$			8	ns	
					$C_L = 50 \text{ pF}$			15		
					$C_L = 100 \text{ pF}$			23		
Fall time	t_f			$T_A = T_J = -55^\circ\text{C to } 125^\circ\text{C}$	$C_L = 150 \text{ pF}$			33		
					$T_A = T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$C_L = 15 \text{ pF}$				8
						$C_L = 50 \text{ pF}$				15
$C_L = 100 \text{ pF}$			23							
			$T_A = T_J = -55^\circ\text{C to } 125^\circ\text{C}$	$C_L = 150 \text{ pF}$			33			
Rise time	t_r	Selectable 8 mA/2 mA-z pins <u>11/</u>	8 mA mode	$T_A = T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$C_L = 15 \text{ pF}$			2.5		
Fall time	t_f					$T_A = T_J = -55^\circ\text{C to } 125^\circ\text{C}$	$C_L = 50 \text{ pF}$			4
							$C_L = 100 \text{ pF}$			7.2
				$T_A = T_J = -40^\circ\text{C to } 125^\circ\text{C}$			$C_L = 150 \text{ pF}$			12.5
$C_L = 15 \text{ pF}$						2.5				
$C_L = 50 \text{ pF}$						4				
				$T_A = T_J = -55^\circ\text{C to } 125^\circ\text{C}$	$C_L = 100 \text{ pF}$			7.2		
				$T_A = T_J = -55^\circ\text{C to } 125^\circ\text{C}$	$C_L = 150 \text{ pF}$			12.5		
Rise time	t_r	2 mA-z mode		$T_A = T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$C_L = 15 \text{ pF}$			8		
Fall time	t_f					$T_A = T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$C_L = 50 \text{ pF}$			15
							$C_L = 100 \text{ pF}$			23
				$T_A = T_J = -55^\circ\text{C to } 125^\circ\text{C}$			$C_L = 150 \text{ pF}$			33
$C_L = 15 \text{ pF}$						8				
$C_L = 50 \text{ pF}$						15				
				$T_A = T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$C_L = 100 \text{ pF}$			23		
				$T_A = T_J = -55^\circ\text{C to } 125^\circ\text{C}$	$C_L = 150 \text{ pF}$			33		

Output timings-Continued

Timing requirements for Outputs 12/ See FIGURE 5

Delay between low to high, or high to low transition of general-purpose output signals that can be configured by an application in parallel, e.g. all signals in a GIOA port, or all N2HET1 signals, etc.	$t_{d(\text{parallel_out})}$						5	ns
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See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test conditions 2/	Limits			Unit
				Min	Typ	Max	

Voltage Monitoring Specifications

Voltage monitoring threshold	VCC low - VCC level below this threshold is detected as too low.	V _{MON}		0.75	0.9	1.13	V
	VCC low – VCC level below this threshold is detected as too low.			1.40	1.7	2.1	
	VCCIO low – VCCIO level below this threshold is detected as too low.			1.85	2.4	2.9	

VMON supply glitch filtering capability

Width of glitch on VCC that can be filtered				250 ns		1 μs	
Width of glitch on VCCIO that can be filtered				250 ns		1 μs	

POWER DOWN SEQUENCE

Electrical Requirements for nPORRST see FIGURE 6

	VCC low supply level when nPORRST must be active during power-up	V _{CCPORL}				0.5	V
	VCC high supply level when nPORRST must remain active during power-up and become active during power down	V _{CCPORH}		1.14			
	VCCIO / VCCP low supply level when nPORRST must be active during power-up	V _{CCIOPORL}				1.1	
	VCCIO / VCCP high supply level when nPORRST must remain active during power-up and become active during power down	V _{CCIOPORH}		3.0			
	Low-level input voltage of nPORRST VCCIO > 2.5V	V _{IL(PORRST)}				0.2 * V _{CCIO}	
	Low-level input voltage of nPORRST VCCIO < 2.5V					0.5	
3	Setup time, nPORRST active before VCCIO and VCCP > VCCIOPORL 0 ms during power-up	t _{su(PORRST)}		0			ms
6	Hold time, nPORRST active after VCC > VCCPORH	t _{h(PORRST)}		1			
7	Setup time, nPORRST active before VCC < VCCPORH during power down	t _{su(PORRST)}		2			μs
8	Hold time, nPORRST active after VCCIO and VCCP > VCCIOPORH	t _{h(PORRST)}		1			ms
9	Hold time, nPORRST active after VCC < VCCPORL	t _{h(PORRST)}		0			
	Filter time nPORRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset.	t _{f(nPORRST)}		500		2000	ns

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
nRST Timing Requirements 13/						
Valid time, nRST active after nPORRST inactive	$t_{v(RST)}$		2252 $t_{c(OSC)}$			ns
Valid time, nRST active (all other System reset conditions)			32 $t_{c(VCLK)}$			
Filter time nRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset	$t_{f(nRST)}$		475		2000	
CLOCKS						
Timing Requirements for Main Oscillator						
Cycle time, OSCIN (when using a sine-wave input)	$t_{c(OSC)}$		50		200	ns
Cycle time, OSCIN, (when input to the OSCIN is a square wave)	$t_{c(OSC_SQR)}$		50		200	
Pulse duration, OSCIN low (when input to the OSCIN is a square wave)	$t_{w(OSCIL)}$		6			
Pulse duration, OSCIN high (when input to the OSCIN is a square wave)	$t_{w(OSCIH)}$		6			
LPO Specifications						
LPO - HF oscillator		Untrimmed frequency	5.5	9.6	19.5	MHz
		Startup time from STANDBY (LPO BIAS_EN High for 10 μ s at least 900 μ s)			10	μ s
		Cold startup time			900	
LPO - LF oscillator		Untrimmed frequency	36	85	180	MHz
		Startup time from STANDBY (LPO BIAS_EN High for 10 μ s at least 900 μ s)			100	μ s
		Cold startup time			2000	
PLL Timing Specifications						
PLL1 Reference Clock frequency	f_{INTCLK}		1		20	MHz
Post-ODCLK – PLL1 Post-divider input clock frequency	f_{post_ODCLK}				400	
VCOCLK – PLL1 Output Divider (OD) input clock frequency	f_{VCOCLK}		150		550	
PLL2 Reference Clock frequency	$f_{INTCLK2}$		1		20	
Post-ODCLK – PLL2 Post-divider input clock frequency	f_{post_ODCLK2}				400	
VCOCLK – PLL2 Output Divider (OD) input clock frequency	$f_{VCOCLK2}$		150		550	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit	
			Min	Typ	Max		
External Clock Timing and Electrical Specifications							
External clock input frequency	$f_{EXTCLKx}$				80	MHz	
EXTCLK high-pulse duration	$t_{w(EXTCLKIN)H}$		6			ns	
EXTCLK low-pulse duration	$t_{w(EXTCLKIN)L}$		6				
Low-level input voltage	$V_{IL(EXTCLKIN)}$		-0.3		0.8	V	
High-level input voltage	$V_{IH(EXTCLKIN)}$		2		VCCIO + 0.3		
CLOCK MONITORING							
LPO and Clock Detection							
Clock Detection		oscillator fail frequency - lower threshold, using untrimmed LPO output	1.375	2.4	4.875	MHz	
		oscillator fail frequency - higher threshold, using untrimmed LPO output	22	38.4	78		
LPO - HF oscillator		untrimmed frequency	5.5	9.6	19.5	μ s	
		startup time from STANDBY (LPO BIAS_EN High for at least 900ms)			10		
		cold startup time			900		
		ICC, CLK10M and CLK80K active			150		μ A
LPO - LF oscillator		untrimmed frequency	36	85	180	MHz	
		startup time from STANDBY (LPO BIAS_EN High for at least 900ms)			100		μ s
		cold startup time			2000		
		ICC, only CLK80K active			27		μ A
LPO		total ICC STANDBY current			20		
GLITCH FILTERS							
Glitch Filter Timing Specifications							
Filter time nPORRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset 14/	$t_{r(nPORRST)}$		01	500		2000	ns
			02	475		2000	
Filter time nRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset	$t_{r(nRST)}$		01	475		2000	
			02	450		2000	
Filter time TEST pin; pulses less than MIN will be filtered out, pulses greater than MAX will pass through	$t_{r(TEST)}$		01	500		2000	
			02	475		2000	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test conditions 2/	Limits			Unit
				Min	Typ	Max	

FLASH MEMORY

Timing Specifications for Program Flash

	Wide Word (144bit) programming time	t_{prog} (144bit)			40	300	μs
	3M Byte programming time 15/	t_{prog} (Total)				32	ms
			0°C to 60°C, for first 25 cycles		8	16	
	Sector/Bank erase time 16/	t_{erase}			0.03	4	ms
			0°C to 60°C, for first 25 cycles		16	100	
	Write/erase cycles with 15 year Data Retention requirement	t_{wec}				1000	cycles

Timing Specifications for Data Flash

	Wide Word (144bit) programming time	t_{prog} (144bit)			40	300	μs
	64 KB Byte programming time 15/	t_{prog} (Total)				600	ms
			0°C to 60°C, for first 25 cycles		165	330	
	Sector/Bank erase time 16/	t_{erase}			0.2	8	
			0°C to 60°C, for first 25 cycles		14	100	ms
	Write/erase cycles with 15 year Data Retention requirement	t_{wec}				100000	cycles

EXTERNAL MEMORY INTERFACE (EMIF)

EMIF Asynchronous Memory Timing Requirements See FIGURE 7 to FIGURE 10

Reads and Writes							
	EMIF clock period	E					ns
2	Pulse duration, EMIFnWAIT assertion and deassertion	$t_{w(EM_WAIT)}$		2E			
Reads							
12	Setup time, EMIFDATA[15:0] valid before EMIFnOE high	$t_{su(EMDV-EMOEH)}$		30			ns
13	Hold time, EMIFDATA[15:0] valid after EMIFnOE high	$t_h(EMOEH-EMDIV)$		0.5			
14	Setup Time, EMIFnWAIT 4E+30 ns asserted before end of Strobe Phase 17/	$t_{su(EMOEL-EMWAIT)}$		4E + 30			
Writes							
28	Setup Time, EMIFnWAIT 4E+30 ns asserted before end of Strobe Phase 17/	$t_{su(EMWEL-EMWAIT)}$		4E + 30			ns

Asynchronous Memory Switching Characteristics 18/ 19/ 20/

Reads and Writes							
1	Turn around time	$t_{d(TURNAROUND)}$		(TA)*E - 4	(TA)*E	(TA)*E + 3	ns

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test conditions 2/	Limits			Unit
				Min	Typ	Max	
EXTERNAL MEMORY INTERFACE (EMIF) – Continued.							
Asynchronous Memory Switching Characteristics - Continued See FIGURE 7 to FIGURE 10 18/ 19/ 20/							
Reads							
3	EMIF read cycle time (EW = 0)	$t_{c(EMRCYCLE)}$		$(RS+RST+RH)^*E - 3$	$(RS+RST+RH)^*E$	$(RS+RST+RH)^*E + 3$	ns
	EMIF read cycle time (EW = 1)			$(RS+RST+RH+(EWC*16))^*E - 3$	$(RS+RST+RH+(EWC*16))^*E$	$(RS+RST+RH+(EWC*16))^*E + 3$	
4	Output setup time, EMIFnCS[4:2] low to EMIFnOE low (SS = 0)	$t_{su(EMCEL-EMOEL)}$		$(RS)^*E - 4$	$(RS)^*E$	$(RS)^*E + 3$	
	Output setup time, EMIFnCS[4:2] low to EMIFnOE low (SS = 1)			-3	0	+3	
5	Output hold time, EMIFnOE high to EMIFnCS[4:2] high (SS = 0)	$t_{h(EMOEH-EMCEH)}$		$(RH)^*E - 4$	$(RH)^*E$	$(RH)^*E + 3$	
	Output hold time, EMIFnOE high to EMIFnCS[4:2] high (SS = 1)			-3	0	+3	
6	Output setup time, EMIFBA[1:0] valid to EMIFnOE low	$t_{su(EMBAV-EMOEL)}$		$(RS)^*E - 4$	$(RS)^*E$	$(RS)^*E + 3$	
7	Output hold time, EMIFnOE high to EMIFBA[1:0] invalid	$t_{h(EMOEH-EMBAIV)}$		$(RH)^*E - 4$	$(RH)^*E$	$(RH)^*E + 3$	
8	Output setup time, EMIFADDR[21:0] valid to EMIFnOE low	$t_{su(EMAV-EMOEL)}$		$(RS)^*E - 4$	$(RS)^*E$	$(RS)^*E + 3$	
9	Output hold time, EMIFnOE high to EMIFADDR[21:0] invalid	$t_{h(EMOEH-EMAIV)}$		$(RH)^*E - 4$	$(RH)^*E$	$(RH)^*E + 3$	
10	EMIFnOE active low width (EW = 0)	$t_{w(EMOEL)}$		$(RS)^*E - 3$	$(RS)^*E$	$(RS)^*E + 3$	
	EMIFnOE active low width (EW = 1)			$(RST+(EWC*16))^*E - 3$	$(RST+(EWC*16))^*E$	$(RST+(EWC*16))^*E + 3$	
11	Delay time from EMIFnWAIT deasserted to EMIFnOE high	$t_{d(EMWAITH-EMOEH)}$		3E - 3	4E	4E + 30	
29	Output setup time, EMIFnDQM[1:0] valid to EMIFnOE low	$t_{su(EMDQMV-EMOEL)}$		$(RS)^*E - 4$	$(RS)^*E$	$(RS)^*E + 3$	
30	Output hold time, EMIFnOE high to EMIFnDQM[1:0] invalid	$t_{h(EMOEH-EMDQMV)}$		$(RH)^*E - 4$	$(RH)^*E$	$(RH)^*E + 3$	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test conditions 2/	Limits			Unit
				Min	Typ	Max	

EXTERNAL MEMORY INTERFACE (EMIF) – Continued.

Asynchronous Memory Switching Characteristics - Continued See FIGURE 7 to FIGURE 10 18/ 19/ 20/

Writes							
15	EMIF write cycle time (EW = 0)	$t_{c(EMWCYCLE)}$		$(WS+WST+WH) * E-3$	$(WS+WST+WH)* E$	$(WS+WST+WH)*E+3$	ns
	EMIF write cycle time (EW = 1)			$(WS+WST+WH+(EWC*16))*E-3$	$(WS+WST+WH+(EWC*16))*E$	$(WS+WST+WH+(EWC*16))*E+3$	
16	Output setup time, EMIFnCS[4:2] low to EMIFnWE low (SS = 0)	$t_{su(EMCEL-EMWEL)}$		$(WS)*E - 4$	$(WS)*E$	$(WS)*E + 3$	
	Output setup time, EMIFnCS[4:2] low to EMIFnWE low (SS = 0)			-4	0	+3	
17	Output hold time, EMIFnWE high to EMIFnCS[4:2] high (SS = 0)	$t_{h(EMWEH-EMCEH)}$		$(WH)*E - 4$	$(WH)*E$	$(WH)*E + 3$	
	Output hold time, EMIFnWE high to EMIFnCS[4:2] high (SS = 1)			-4	0	+3	
18	Output setup time, EMIFBA[1:0] valid to EMIFnWE low	$t_{su(EMDQMV-EMWEL)}$		$(WS)*E - 4$	$(WS)*E$	$(WS)*E + 3$	
19	Output hold time, EMIFnWE high to EMIFBA[1:0] invalid	$t_{h(EMWEH-EMDQMV)}$		$(WH)*E - 4$	$(WH)*E$	$(WH)*E + 3$	
20	Output setup time, EMIFBA[1:0] valid to EMIFnWE low	$t_{su(EMBAV-EMWEL)}$		$(WS)*E - 4$	$(WS)*E$	$(WS)*E + 3$	
21	Output hold time, EMIFnWE high to EMIFBA[1:0] invalid	$t_{h(EMWEH-EMBAIV)}$		$(WH)*E - 4$	$(WH)*E$	$(WH)*E + 3$	
22	Output setup time, EMIFADDR[21:0] valid to EMIFnWE low	$t_{su(EMAV-EMWEL)}$		$(WS)*E - 4$	$(WS)*E$	$(WS)*E + 3$	
23	Output hold time, EMIFnWE high to EMIFADDR[21:0] invalid	$t_{h(EMWEH-EMAIV)}$		$(WH)*E - 4$	$(WH)*E$	$(WH)*E + 3$	
24	EMIFnWE active low width (EW = 0)	$t_w(EMWEL)$		$(WST)*E - 3$	$(WST)*E$	$(WST)*E + 3$	
	EMIFnWE active low width (EW = 1)			$(WST+(EWC*1))*E-3$	$(WST+(EWC*1))*E$	$(WST+(EWC*1))*E+3$	
25	Delay time from EMIFnWAIT deasserted to EMIFnWE high	$t_d(EMWAITH-EMWEH)$		3E - 4	4E	4E + 30	
26	Output setup time, EMIFDATA[15:0] valid to EMIFnWE low	$t_{su(EMDV-EMWEL)}$		$(WS)*E - 4$	$(WS)*E$	$(WS)*E + 3$	
27	Output hold time, EMIFnWE high to EMIFDATA[15:0] invalid	$t_{h(EMWEH-EMDIV)}$		$(WH)*E - 4$	$(WH)*E$	$(WH)*E + 3$	
31	Output setup time, EMIFnDQM[1:0] valid to EMIFnWE low	$t_{su(EMDQMV-EMWEL)}$		$(WS)*E - 4$	$(WS)*E$	$(WS)*E + 3$	
32	Output hold time, EMIFnWE high to EMIFnDQM[1:0] invalid	$t_{h(EMWEH-EMDQMV)}$		$(WH)*E - 4$	$(WH)*E$	$(WH)*E + 3$	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test conditions 2/	Limits			Unit
				Min	Typ	Max	
EXTERNAL MEMORY INTERFACE (EMIF) – Continued.							
EMIF Synchronous Memory Timing Requirements see FIGURE 11 and FIGURE 12							
19	Input setup time, read data valid on EMIFDATA[15:0] before EMIF_CLK rising	$t_{su}(EMIFDV-EM_CLKH)$		2			ns
20	Input hold time, read data valid on EMIFDATA[15:0] after EMIF_CLK rising	$t_h(CLKH-DIV)$		1.5			
EMIF Synchronous Memory Switching Characteristics see FIGURE 11 and FIGURE 12							
1	Cycle time, EMIF clock EMIF_CLK	$t_c(CLK)$					ns
2	Pulse width, EMIF clock EMIF_CLK high or low	$t_w(CLK)$		5			
3	Delay time, EMIF_CLK rising to EMIFnCS[0] valid	$t_d(CLKH-CSV)$				13	
4	Output hold time, EMIF_CLK rising to EMIFnCS[0] invalid	$t_{oh}(CLKH-CSIV)$		1			
5	Delay time, EMIF_CLK rising to EMIFnDQM[1:0] valid	$t_d(CLKH-DQMV)$				13	
6	Output hold time, EMIF_CLK rising to EMIFnDQM[1:0] invalid	$t_{oh}(CLKH-DQMIV)$		1			
7	Delay time, EMIF_CLK rising to EMIFADDR[21:0] and EMIFBA[1:0] valid	$t_d(CLKH-AV)$				13	
8	Output hold time, EMIF_CLK rising to EMIFADDR[21:0] and EMIFBA[1:0] invalid	$t_{oh}(CLKH-AIV)$		1			
9	Delay time, EMIF_CLK rising to EMIFDATA[15:0] valid	$t_d(CLKH-DV)$				13	
10	Output hold time, EMIF_CLK rising to EMIFDATA[15:0] invalid	$t_{oh}(CLKH-DIV)$		1			
11	Delay time, EMIF_CLK rising to EMIFnRAS valid	$t_d(CLKH-RASV)$				13	
12	Output hold time, EMIF_CLK rising to EMIFnRAS invalid	$t_{oh}(CLKH-RASIV)$		1			
13	Delay time, EMIF_CLK rising to EMIFnCAS valid	$t_d(CLKH-CASV)$				13	
14	Output hold time, EMIF_CLK rising to EMIFnCAS invalid	$t_{oh}(CLKH-CASIV)$		1			
15	Delay time, EMIF_CLK rising to EMIFnWE valid	$t_d(CLKH-WEV)$				13	
16	Output hold time, EMIF_CLK rising to EMIFnWE invalid	$t_{oh}(CLKH-WEIV)$		1			
17	Delay time, EMIF_CLK rising to EMIFDATA[15:0] tri-stated	$t_{dis}(CLKH-DHZ)$				7	
18	Output hold time, EMIF_CLK rising to EMIFDATA[15:0] driving	$t_{ena}(CLKH-DLZ)$		1			

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test conditions 2/	Limits			Unit	
				Min	Typ	Max		
DEBUG SUBSYSTEM								
JTAG Scan Interface Timing 21/ see FIGURE 13								
	TCK frequency (at HCLKmax)	f_{TCK}				12	MHz	
	RTCK frequency (at TCKmax and HCLKmax)	f_{RTCK}		10			MHz	
1	Delay time, TCK to RTCK	$t_{d(TCK-RTCK)}$				24	ns	
2	Setup time, TDI, TMS before RTCK rise (RTCKr)	$t_{su(TDI/TMS-RTCKr)}$		26				
3	Hold time, TDI, TMS after RTCKr	$t_{h(RTCKr-TDI/TMS)}$		0				
4	Hold time, TDO after RTCKf	$t_{h(RTCKr-TDO)}$		0				
5	Delay time, TDO valid after RTCK fall (RTCKf)	$t_{d(TCKf-TDO)}$				12		
ETMTRACECLK Timing see FIGURE 14								
	Clock period	$t_{cyc(ETM)}$		$t_{(HCLK)} * 4$			ns	
	Low pulse width	$t_{l(ETM)}$		20				
	High pulse width	$t_{h(ETM)}$		20				
	Clock and data rise time	$t_{r(ETM)}$				3		
	Clock and data fall time	$t_{f(ETM)}$				3		
ETM DATA Timing see FIGURE 15								
	Delay time from ETM trace clock high to ETM data valid	$t_{d(ETMTRACECLKH-ETM DATAV)}$		01	1.5		7	ns
				02	1.3		7	
	Delay time from ETM trace clock low to ETM data valid	$t_{d(ETMTRACECLKL-ETM DATAV)}$		01	1.5		7	
				02	1.3		7	
RTPCLK Timing see FIGURE 16								
	Clock period, prescaled from HCLK; must not be faster than HCLK / 2	$t_{cyc(RTP)}$		11ns (90MHz)			ns	
	High pulse width	$t_{h(RTP)}$		$((t_{cyc(RTP)})/2) - ((t_r+t_f)/2)$				
	Low pulse width	$t_{l(RTP)}$		$((t_{cyc(RTP)})/2) - ((t_r+t_f)/2)$				
RTP DATA Timing see FIGURE 17								
	SYNC delay time	$t_{d(RTPCLKH-RTPSYNCV)}$		-5		4	ns	
	Data delay time	$t_{d(RTPCLKH-RTPDATAV)}$		-5		4		
RTPnENA timing see FIGURE 18								
	time RTPnENA must go high before what would be the next RTPSYNC, to guarantee delaying the next packet	$t_{dis(RTP)}$		$3t_{c(HCLK)} + t_{r(RTPSYNC)} + 12ns$			ns	
	time after RTPnENA goes low before a packet that has been halted, resumes	$t_{ena(RTP)}$		$4t_{c(HCLK)} + t_{r(RTPSYNC)}$		$4t_{c(HCLK)} + t_{r(RTPSYNC)} + 12$		

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits		Unit	
			Min	Max		
DEBUG SUBSYSTEM – Continued.						
DMMCLK Timing see FIGURE 19						
Clock period	$t_{cyc(DMM)}$		$t_{c(HCLK)} * 2$		ns	
High pulse width	$t_{h(DMM)}$		$((t_{cyc(DMM)})/2) - ((t_r+t_f)/2)$			
Low pulse width	$t_{l(DMM)}$		$((t_{cyc(DMM)})/2) - ((t_r+t_f)/2)$			
MULTI BUFFERED 12 BIT ANALOG TO DIGITAL CONVERTER						
MibADC Recommended Operating Conditions						
A-to-D high-voltage reference source			ADREFLO	VCCAD	V	
A-to-D low-voltage reference source			VSSAD	ADREFHI		
Analog input voltage			ADREFLO	ADREFHI		
Analog input clamp current		$V_{AI} < V_{SSAD} - 0.3 V$ or $V_{AI} > V_{CCAD} + 0.3 V$	-2	2	mA	
MibADC Electrical Characteristics						
Analog input mux on-resistance		see FIGURE 22		250	Ω	
ADC sample switch on-resistance				250		
Input mux capacitance				16	pF	
ADC sample capacitance				13		
Analog off state input leakage current	I_{AIL}	VCCAD = 3.6 V maximun	$V_{SSAD} \leq V_{IN} < V_{SSAD} + 100mV$	-300	200	nA
			$V_{SSAD} + 100mV \leq V_{IN} \leq V_{CCAD} - 200mV$	-200	200	
			$V_{CCAD} - 200mV < V_{IN} \leq V_{CCAD}$	-200	500	
Analog off state input leakage current	I_{AIL}	VCCAD = 5.5 V maximun	$V_{SSAD} \leq V_{IN} < V_{SSAD} + 300mV$	-1000	250	nA
			$V_{SSAD} + 300mV \leq V_{IN} \leq V_{CCAD} - 300mV$	-250	250	
			$V_{CCAD} - 300mV < V_{IN} \leq V_{CCAD}$	-250	1000	
ADC1 Analog on-state input bias current	I_{AOSB1} 22/	VCCAD = 3.6 V maximun	$V_{SSAD} \leq V_{IN} < V_{SSAD} + 100mV$	-8	2	μA
			$V_{SSAD} + 100mV \leq V_{IN} \leq V_{CCAD} - 200mV$	-4	2	
			$V_{CCAD} - 200mV < V_{IN} \leq V_{CCAD}$	-4	12	
ADC2 Analog on-state input bias current	I_{AOSB2} 22/	VCCAD = 3.6 V maximun	$V_{SSAD} \leq V_{IN} < V_{SSAD} + 100mV$	-7	2	μA
			$V_{SSAD} + 100mV \leq V_{IN} \leq V_{CCAD} - 200mV$	-4	2	
			$V_{CCAD} - 200mV < V_{IN} \leq V_{CCAD}$	-4	10	
ADC1 Analog on-state input bias current	I_{AOSB1} 22/	VCCAD = 5.5 V maximun	$V_{SSAD} \leq V_{IN} < V_{SSAD} + 300mV$	-10	3	μA
			$V_{SSAD} + 300mV \leq V_{IN} \leq V_{CCAD} - 300mV$	-5	3	
			$V_{CCAD} - 300mV < V_{IN} \leq V_{CCAD}$	-5	14	
ADC2 Analog on-state input bias current	I_{AOSB2} 22/	VCCAD = 5.5 V maximun	$V_{SSAD} \leq V_{IN} < V_{SSAD} + 300mV$	-8	3	μA
			$V_{SSAD} + 300mV \leq V_{IN} \leq V_{CCAD} - 300mV$	-5	3	
			$V_{CCAD} - 300mV < V_{IN} \leq V_{CCAD}$	-5	12	
ADREFHI input current	$I_{ADREFHI}$	ADREFHI = VCCAD, ADREFLO = VSSAD		3	mA	
Static supply current	I_{CCAD}	Normal operating mode		15		
		ADC core in power down mode		5	μA	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
MULTI BUFFERED 12 BIT ANALOG TO DIGITAL CONVERTER – Continued.						
MibADC Timing Specifications						
Cycle time, MibADC clock	$t_{c(ADCLK)}$ 23/		0.033			μs
Delay time, sample and hold time	$t_{d(SH)}$ 24/		0.2			
Delay time from ADC power on until first input can be sampled	$t_{d(PU-ADV)}$		1			
MibADC Timing Specifications -12 bit mode						
Delay time, conversion time	$t_{d(c)}$		0.4			μs
Delay time, total sample/hold and conversion time	$t_{d(SHC)}$ 25/		0.6			
MibADC Timing Specifications -10 bit mode						
Delay time, conversion time	$t_{d(c)}$		0.33			μs
Delay time, total sample/hold and conversion time	$t_{d(SHC)}$ 25/		0.53			
MibADC Operating Characteristics						
Conversion range over which specified accuracy is maintained	CR		3		5.5	V
Zero Scale Offset	Z_{SET}	Difference between the first ideal transition (from code 000h to 001h) and the actual transition	10-bit mode		1	LSB 26/
			12-bit mode		2	LSB 27/
Full Scale Offset	F_{SET}	Difference between the range of the measured code transitions (from first to last) and the range of the ideal code transitions	10-bit mode		2	LSB
			12-bit mode		3	
Differential nonlinearity error	E_{DNL}	Difference between the actual step width and the ideal value. (See Figure 76)	10-bit mode		± 1.5	
			12-bit mode		± 2	
Integral nonlinearity error	E_{INL}	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error	10-bit mode		± 2	
			12-bit mode		± 2	
Total unadjusted error	E_{TOT}	Maximum value of the difference between an analog value and the ideal midstep value.	10-bit mode		± 2	
			12-bit mode		± 4	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test conditions 2/	Limits		Unit
				Min	Max	

GENERAL PURPOSE INPUT/OUTPUT

Input Timing Requirements for the N2HET Input Capture Functionality 28/ 29/ see FIGURE 23

1	Input signal period, PCNT or WCAP for rising edge to rising edge			2 (hr) (lr) tc(VCLK2) + 2	2 ²⁵ (hr) (lr) tc(VCLK2) - 2	ns
2	Input signal period, PCNT or WCAP for falling edge to falling edge			2 (hr) (lr) tc(VCLK2) + 2	2 ²⁵ (hr) (lr) tc(VCLK2) - 2	
3	Input signal high phase, PCNT or WCAP for rising edge to falling edge			(hr) (lr) tc(VCLK2) + 2	2 ²⁵ (hr) (lr) tc(VCLK2) - 2	
4	Input signal low phase, PCNT or WCAP for falling edge to rising edge			(hr) (lr) tc(VCLK2) + 2	2 ²⁵ (hr) (lr) tc(VCLK2) - 2	

Input Timing Requirements for N2HET Channels with Enhanced Pulse Capture 28/ 29/

1	Input signal period, PCNT or WCAP for rising edge to rising edge			(hr) (lr) tc(VCLK2) + 2	2 ²⁵ (hr) (lr) tc(VCLK2) - 2	ns
2	Input signal period, PCNT or WCAP for falling edge to falling edge			(hr) (lr) tc(VCLK2) + 2	2 ²⁵ (hr) (lr) tc(VCLK2) - 2	
3	Input signal high phase, PCNT or WCAP for rising edge to falling edge			2 (hr) tc(VCLK2) + 2	2 ²⁵ (hr) (lr) tc(VCLK2) - 2	
4	Input signal low phase, PCNT or WCAP for falling edge to rising edge			2 (hr) tc(VCLK2) + 2	2 ²⁵ (hr) (lr) tc(VCLK2) - 2	

FLEXRAY INTERFACE

Timing Requirements for FlexRay Inputs see FIGURE 24

	Input minimum pulse width to meet the FlexRay sampling requirement	t _{pw}		t _c (AVCLK2) + 2.5 30/		ns
--	--	-----------------	--	--------------------------------------	--	----

FlexRay Jitter Timing

	Clock jitter and signal symmetry	t _{Tx1bit}		98	102	ns
	FlexRay BSS (byte start sequence) to BSS	t _{Tx10bit}		999	1001	
	Average over 10000 samples	t _{Tx10bitAvg}		999.5	1000.5	
	Delay difference between rise and fall from Rx pin to sample point in FlexRay core	t _{RxAsymDelay}			2.5	
	Jitter for the 80MHz Sample Clock generated by the PLL	t _{jit} (SCLK)			0.5	

CONTROLLER AREA NETWORK (DCAN)

Dynamic Characteristics for the DCANx TX and RX pins

	Delay time, transmit shift register to CANnTX pin 31/	t _d (CANnTX)			15	ns
	Delay time, CANnRX pin to receive shift register	t _d (CANnRX)			5	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
INTER-INTEGRATED CIRCUIT (I2C)							
I2C Signals (SDA and SCL) Switching Characteristics 32/ see FIGURE 25							
Cycle time, Internal Module clock for I2C, prescaled from VCLK	$t_{c(I2CCLK)}$		75.2	149	75.2	149	ns
SCL Clock frequency	$f_{(SCL)}$		0	100	0	400	kHz
Cycle time, SCL	$t_{c(SCL)}$		10		2.5		
Setup time, SCL high before SDA low (for a repeated START condition)	$t_{su(SCLH-SDAL)}$		4.7		0.6		
Hold time, SCL low after SDA low (for a repeated START condition)	$t_{h(SCLL-SDAL)}$		4		0.6		
Pulse duration, SCL low	$t_{w(SCLL)}$		4.7		1.3		
Pulse duration, SCL high	$t_{w(SCLH)}$		4		0.6		
Setup time, SDA valid before SCL high	$t_{su(SDA-SCLH)}$		250		100		
Hold time, SDA valid after SCL low (for I2C bus devices)	$t_{h(SDA-SCLL)}$		0	3.45 33/	0	0.9	μs
Pulse duration, SDA high between STOP and START conditions	$t_{w(SDAH)}$		4.7		1.3		
Setup time, SCL high before SDA high (for STOP condition)	$t_{su(SCLH-SDAH)}$		4.0		0.6		
Pulse duration, spike (must be suppressed)	$t_{w(SP)}$				0	50	ns
Capacitive load for each bus line	C_b 34/			400		400	pF

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits		Unit	
			Min	Max		
MULTI-BUFFERED / STANDARD SERIAL PERIPHERAL INTERFACE						
SPI Master Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)						
2/ 35/ 36/ 37/ see FIGURE 26 and FIGURE 27						
1	Cycle time, SPICLK 38/	$t_{c(SPC)M}$	40	$256t_c(VCLK)$	ns	
2	Pulse duration, SPICLK high (clock polarity = 0) -40°C to 125°C	$t_{w(SPCH)M}$	$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$		
39/	Pulse duration, SPICLK low (clock polarity = 1) -40°C to 125°C	$t_{w(SPCL)M}$	$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$		
3	Pulse duration, SPICLK low (clock polarity = 0) -40°C to 125°C	$t_{w(SPCL)M}$	$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$		
39/	Pulse duration, SPICLK high (clock polarity = 1) -40°C to 125°C	$t_{w(SPCH)M}$	$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$		
4	Delay time, SPISIMO valid before SPICLK low (clock polarity = 0)	$t_{d(SPCH-SIMO)M}$	$0.5t_{c(SPC)M} - 6$			
39/	Delay time, SPISIMO valid before SPICLK high (clock polarity = 1)	$t_{d(SPCL-SIMO)M}$	$0.5t_{c(SPC)M} - 6$			
5	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$t_{v(SPCL-SIMO)M}$	$0.5t_{c(SPC)M} - t_{r(SPC)M} - 4$			
39/	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCH-SIMO)M}$	$0.5t_{c(SPC)M} - t_{r(SPC)M} - 4$			
6	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	$t_{su(SOMI-SPCL)M}$	$t_{r(SPC)} + 2.2$			
39/	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	$t_{su(SOMI-SPCH)M}$	$t_{r(SPC)} + 2.2$			
7	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$t_{h(SPCL-SOMI)M}$	10			
39/	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$t_{h(SPCH-SOMI)M}$	10			
8	Setup time CS active until	CSHOLD = 0	$t_{C2TDELAY}$	$C2TDELAY * t_{c(VCLK)} + 2 * t_{c(VCLK)} - t_{r(SPICS)} + t_{r(SPC)} - 7$	$(C2TDELAY + 2) * t_{c(VCLK)} - t_{r(SPICS)} + t_{r(SPC)} + 5.5$	
	40/	SPICLK high (clock polarity = 0)		CSHOLD = 1	$C2TDELAY * t_{c(VCLK)} + 3 * t_{c(VCLK)} - t_{r(SPICS)} + t_{r(SPC)} - 7$	$(C2TDELAY + 3) * t_{c(VCLK)} - t_{r(SPICS)} + t_{r(SPC)} + 5.5$
		Setup time CS active until		CSHOLD = 0	$C2TDELAY * t_{c(VCLK)} + 2 * t_{c(VCLK)} - t_{r(SPICS)} + t_{r(SPC)} - 7$	$(C2TDELAY + 2) * t_{c(VCLK)} - t_{r(SPICS)} + t_{r(SPC)} + 5.5$
		SPICLK low (clock polarity = 1)		CSHOLD = 1	$C2TDELAY * t_{c(VCLK)} + 3 * t_{c(VCLK)} - t_{r(SPICS)} + t_{r(SPC)} - 7$	$(C2TDELAY + 3) * t_{c(VCLK)} - t_{r(SPICS)} + t_{r(SPC)} + 5.5$
9	40/	Hold time SPICLK low until CS inactive (clock polarity = 0)	$t_{T2CDELAY}$	$0.5 * t_{c(SPC)M} + T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 7$	$0.5 * t_{c(SPC)M} + T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$	
		Hold time SPICLK high until CS inactive (clock polarity = 1)		$0.5 * t_{c(SPC)M} + T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 7$	$0.5 * t_{c(SPC)M} + T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$	
10	SPIENAn Sample point	t_{SPIENA}		$(C2TDELAY + 1) * t_{c(VCLK)} - t_{r(SPICS)} - 29$	$(C2TDELAY + 1) * t_{c(VCLK)}$	
11	SPIENAn Sample point from write to buffer -40°C to 125°C	$t_{SPIENAW}$			$(C2TDELAY + 2) * t_{c(VCLK)}$	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits		Unit
			Min	Max	
MULTI-BUFFERED / STANDARD SERIAL PERIPHERAL INTERFACE- Continued.					
SPI Master Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)					
2/ 35/ 36/ 37/ see FIGURE 28 and FIGURE 29					
1	Cycle time, SPICLK 38/	$t_{c(SPC)M}$	40	256tc(VCLK)	ns
2	Pulse duration, SPICLK high (clock polarity = 0) -40°C to 125°C	$t_{w(SPCH)M}$	$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
39/	Pulse duration, SPICLK low (clock polarity = 1) -40°C to 125°C	$t_{w(SPCL)M}$	$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
3	Pulse duration, SPICLK low (clock polarity = 0) -40°C to 125°C	$t_{w(SPCL)M}$	$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
39/	Pulse duration, SPICLK high (clock polarity = 1) -40°C to 125°C	$t_{w(SPCH)M}$	$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
4	Valid time, SPICLK high after SPISIMO data valid (clock polarity = 0)	$t_d(SPCH-SIMO)M$	$0.5t_{c(SPC)M} - 6$		
39/	Valid time, SPICLK low after SPISIMO data valid (clock polarity = 1)	$t_d(SPCL-SIMO)M$	$0.5t_{c(SPC)M} - 6$		
5	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$t_v(SPCL-SIMO)M$	$0.5t_{c(SPC)M} - t_{f(SPC)M} - 4$		
39/	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$t_v(SPCH-SIMO)M$	$0.5t_{c(SPC)M} - t_{r(SPC)M} - 4$		
6	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$t_{su}(SOMI-SPCL)M$	$t_{r(SPC)} + 2.2$		
39/	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	$t_{su}(SOMI-SPCH)M$	$t_{r(SPC)} + 2.2$		
7	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$t_h(SPCL-SOMI)M$	10		
39/	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$t_h(SPCH-SOMI)M$	10		
8	Setup time CS active until SPICLK high	CSHOLD = 0	$t_{C2DELAY}$	$0.5*t_{c(SPC)M} + (C2DELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2DELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$
40/	(clock polarity = 0)	CSHOLD = 1		$0.5*t_{c(SPC)M} + (C2DELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2DELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$
	Setup time CS active until SPICLK low	CSHOLD = 0		$0.5*t_{c(SPC)M} + (C2DELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2DELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$
	(clock polarity = 1)	CSHOLD = 1		$0.5*t_{c(SPC)M} + (C2DELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2DELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$
9	Hold time SPICLK low until CS inactive (clock polarity = 0)	$t_{T2CDELAY}$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 7$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$	
40/	Hold time SPICLK high until CS inactive (clock polarity = 1)		$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 7$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$	
10	SPIENAn Sample point	t_{SPIENA}	$(C2DELAY+1) * t_{c(VCLK)} - t_{f(SPICS)} - 29$	$(C2DELAY+1)*t_{c(VCLK)}$	
11	SPIENAn Sample point from write to buffer -40°C to 125°C	$t_{SPIENAW}$		$(C2DELAY+2)*t_{c(VCLK)}$	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits		Unit
			Min	Max	
MULTI-BUFFERED / STANDARD SERIAL PERIPHERAL INTERFACE – Continued.					
SPI Slave Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = input, SPISIMO = input, and SPISOMI = output)					
2/ 35/ 36/ 37/ 41/ see FIGURE 30 and 31					
1	Cycle time, SPICLK 42/	$t_{c(SPC)S}$	40		ns
2	Pulse duration, SPICLK high (clock polarity = 0) -40°C to 125°C	$t_{w(SPCH)S}$	14		
39/	Pulse duration, SPICLK low (clock polarity = 1) -40°C to 125°C	$t_{w(SPCL)S}$	14		
3	Pulse duration, SPICLK low (clock polarity = 0) -40°C to 125°C	$t_{w(SPCL)S}$	14		
39/	Pulse duration, SPICLK high (clock polarity = 1) -40°C to 125°C	$t_{w(SPCH)S}$	14		
4	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)	$t_{d(SPCH-SOMI)S}$		$t_{r(SOMI)} + 20$	
39/	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)	$t_{d(SPCL-SOMI)S}$		$t_{r(SOMI)} + 20$	
5	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$t_{h(SPCH-SOMI)S}$	2		
39/	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$t_{h(SPCL-SOMI)S}$	2		
6	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	$t_{su(SIMO-SPCL)S}$	4		
39/	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	$t_{su(SIMO-SPCH)S}$	4		
7	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$t_{h(SPCL-SIMO)S}$	2		
39/	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{h(SPCH-SIMO)S}$	2		
8	Delay time, SPIENAn high after last SPICLK low (clock polarity = 0)	$t_{d(SPCL-SENAH)S}$	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)} + t_{r(ENAn)} + 22$	
40/	Delay time, SPIENAn high after last SPICLK high (clock polarity = 1)	$t_{d(SPCH-SENAH)S}$	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)} + t_{r(ENAn)} + 22$	
9	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{d(SCSL-SENAL)S}$	$t_{r(ENAn)}$	$t_{c(VCLK)} + t_{r(ENAn)} + 27$	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits		Unit
			Min	Max	
MULTI-BUFFERED / STANDARD SERIAL PERIPHERAL INTERFACE – Continued.					
SPI Slave Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = input, SPISIMO = input, and SPISOMI = output)					
2/ 35/ 36/ 37/ 43/ see FIGURE 32 and FIGURE 33					
1	Cycle time, SPICLK 42/	$t_c(\text{SPC})_S$	40		ns
2	Pulse duration, SPICLK high (clock polarity = 0) -40°C to 125°C	$t_w(\text{SPCH})_S$	14		
39/	Pulse duration, SPICLK low (clock polarity = 1) -40°C to 125°C	$t_w(\text{SPCL})_S$	14		
3	Pulse duration, SPICLK low (clock polarity = 0) -40°C to 125°C	$t_w(\text{SPCL})_S$	14		
39/	Pulse duration, SPICLK high (clock polarity = 1) -40°C to 125°C	$t_w(\text{SPCH})_S$	14		
4	Delay time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$t_d(\text{SOMI-SPCL})_S$		$t_{r(\text{SOMI})} + 20$	
39/	Delay time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$t_d(\text{SOMI-SPCH})_S$		$t_{r(\text{SOMI})} + 20$	
5	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$t_h(\text{SPCL-SOMI})_S$	2		
39/	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$t_h(\text{SPCH-SOMI})_S$	2		
6	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	$t_{su}(\text{SIMO-SPCH})_S$	4		
39/	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	$t_{su}(\text{SIMO-SPCL})_S$	4		
7	High time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$t_v(\text{SPCH-SIMO})_S$	2		
39/	High time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$t_v(\text{SPCL-SIMO})_S$	2		
8	Delay time, SPIENAn high after last SPICLK high (clock polarity = 0)	$t_d(\text{SPCL-SENAH})_S$	$1.5t_c(\text{VCLK})$	$2.5t_c(\text{VCLK}) + t_{r(\text{ENAn})} + 22$	
40/	Delay time, SPIENAn high after last SPICLK low (clock polarity = 1)	$t_d(\text{SPCH-SENAH})_S$	$1.5t_c(\text{VCLK})$	$2.5t_c(\text{VCLK}) + t_{r(\text{ENAn})} + 22$	
9	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_d(\text{SCSL-SENAL})_S$	$t_{r(\text{ENAn})}$	$t_c(\text{VCLK}) + t_{r(\text{ENAn})} + 27$	
10	Delay time, SOMI valid after SPICSn low (if new data has been written to the SPI buffer)	$t_d(\text{SCSL-SOMI})_S$	$t_c(\text{VCLK})$	$2t_c(\text{VCLK}) + t_{r(\text{SOMI})} + 28$	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/ 2/

No	Test	Symbol	Limits			Unit
			Min	Typ	Max	
ETHERNET MEDIA ACCESS CONTROLLER						
MII Receive Timing see FIGURE 34						
	Setup time, MIIMRXD to MIIMRCLK rising edge	$t_{su}(MIIMRXD)$	8			ns
	Setup time, MIIMRXDV to MIIMRCLK rising edge	$t_{su}(MIIMRXDV)$	8			
	Setup time, MIIMRXER to MIIMRCLK rising edge	$t_{su}(MIIMRXER)$	8			
	Hold time, MIIMRXD valid after MIIRCLK rising edge	$t_h(MIIMRXD)$	8			
	Hold time, MIIMRXDV valid after MIIRCLK rising edge	$t_h(MIIMRXDV)$	8			
	Hold time, MIIMRXDV valid after MIIRCLK rising edge	$t_h(MIIMRXER)$	8			
MII Transmit Timing see FIGURE 35						
	Delay time, MIIMTCLK rising edge to MIIMTXD	$t_d(MIIMTXD)$	5		25	ns
	Delay time, MIIMTCLK rising edge to MIIMTXEN	$t_d(MIIMTXEN)$	5		25	
RMII Timing Requirements see FIGURE 36						
1	Cycle time, RMII_REF_CLK	$t_c(REFCLK)$		20		
2	Pulse width, RMII_REF_CLK High	$t_w(REFCLKH)$	7		13	
3	Pulse width, RMII_REF_CLK Low	$t_w(REFCLKL)$	7		13	
6	Input setup time, RMII_RXD valid before RMII_REF_CLK High	$t_{su}(RXD-REFCLK)$	4			
7	Input hold time, RMII_RXD valid after RMII_REF_CLK High	$t_h(REFCLK-RXD)$	2			
8	Input setup time, RMII_CRSDV valid before RMII_REF_CLK High	$t_{su}(CRSDV-REFCLK)$	4			
9	Input hold time, RMII_CRSDV valid after RMII_REF_CLK High	$t_h(REFCLK-CRSDV)$	2			
10	Input setup time, RMII_RXER valid before RMII_REF_CLK High	$t_{su}(RXER-REFCLK)$	4			
11	Input hold time, RMII_RXER valid after RMII_REF_CLK High	$t_h(REFCLK-RXER)$	2			
4	Output delay time, RMII_REF_CLK High to RMII_TXD valid	$t_d(REFCLK-TXD)$	2			
5	Output delay time, RMII_REF_CLK High to RMII_TX_EN valid	$t_d(REFCLK-TXEN)$	2			
MDIO Input Timing Requirements see FIGURE 37						
1	Cycle time, MDCLK	$t_c(MDCLK)$	400			ns
2	Pulse duration, MDCLK high/low	$t_w(MDCLK)$	180			
3	Transition time, MDCLK	$t_t(MDCLK)$			5	
4	Setup time, MDIO data input valid before MDCLK High	$t_{su}(MDIO-MDCLKH)$	33 44			
5	Hold time, MDIO data input valid after MDCLK High	$t_h(MDCLKH-MDIO)$	10			
MDIO Output Timing Requirements see FIGURE 38						
1	Cycle time, MDCLK	$t_c(MDCLK)$	400			
7	Delay time, MDCLK low to MDIO data output valid	$t_d(MDCLKL-MDIO)$	-7		100	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/ 2/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over operating conditions (unless otherwise noted). $T_A \leq +85^\circ\text{C}$
- 3/ The typical value is the average current for the nominal process corner and junction temperature of 25°C .
- 4/ The maximum I_{CC} , value can be derated
- linearly with voltage
 - by 1mA/MHz for lower operating frequency when $f_{HCLK} = 2 * f_{VCLK}$
 - for lower junction temperature by the equation below where T_{JK} is the junction temperature in Kelvin and the result is in milliamperes. $235 - 0.15 e^{0.0174 T_{JK}}$
- 5/ The maximum I_{CC} , value can be derated
- linearly with voltage
 - by 1.7ma/MHz for lower operating frequency when $f_{HCLK} = 2 * f_{VCLK}$
- for lower junction temperature by the equation below where T_{JK} is the junction temperature in Kelvin and the result is in milliamperes. $235 - 0.15 e^{0.0174 T_{JK}}$
- 6/ LBIST and PBIST currents are for a short duration, typically less than 10ms. They are usually ignored for thermal calculations for the device and the voltage regulator.
- 7/ Source currents (out of the device) are negative while sink currents (into the device) are positive.
- 8/ See section 3.10 from manufacturer data sheet.
- 9/ $t_{c(VCLK)} = \text{peripheral VBUS clock cycle time} = 1 / f_{(VCLK)}$.
- 10/ The timing shown above is only valid for pin used in GIO mode.
- 11/ See table 3-5 from manufacturer data sheet.
- 12/ This specification does not account for any output buffer drive strength differences or any external capacitive loading differences. Check Table 3-2 from manufacturer data sheet for output buffer drive strength information on each signal.
- 13/ Specified values do NOT include rise/fall times. For rise and fall timings, see Table 3-5 from manufacturer data sheet.
- 14/ The glitch filter design on the nPORRST signal is designed such that no size pulse will reset any part of the microcontroller (flash pump, I/O pins, etc.) without also generating a valid reset signal to the CPU.
- 15/ This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 144 bits at a time at the maximum specified operating frequency.
- 16/ During bank erase, the selected sectors are erased simultaneously. The time to erase the bank is specified as equal to the time to erase a sector.
- 17/ Setup before end of STROBE phase (if no extended wait states are inserted) by which EMIFnWAIT must be asserted to add extended wait states. Figure 8 to Figure 10 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.
- 18/ TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4–1], RS[16–1], RST[64–1], RH[8–1], WS[16–1], WST[64–1], WH[8–1], and MEWC[1–256]. See the for more information.
- 19/ E = EMIF_CLK period in ns.
- 20/ EWC = external wait cycles determined by EMIFnWAIT input signal. EWC supports the following range of values. EWC[256–1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See manufacturer data sheet for more information.
- 21/ Timings for TDO are specified for a maximum of 50 pF load on TDO.
- 22/ If a shared channel is being converted by both ADC converters at the same time, the on-state leakage is equal to $I_{AOSL1} + I_{AOSL2}$.

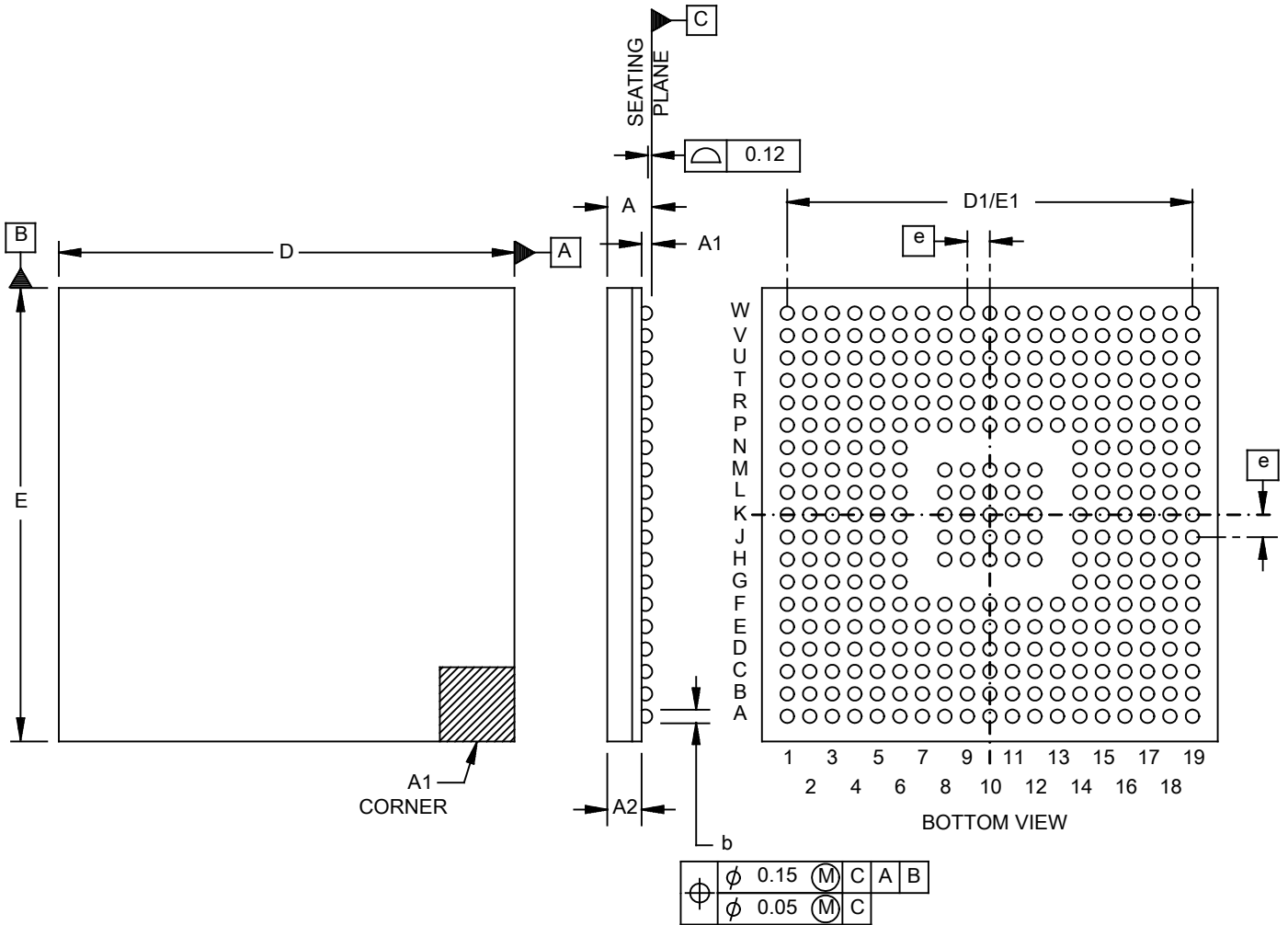
DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13629
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TABLE I. Electrical performance characteristics - Continued. 1/ 2/

- 23/ The MibADC clock is the ADCLK, generated by dividing down the VCLK by a prescale factor defined by the ADCLOCKCR register bits 4:0.
- 24/ The sample and hold time for the ADC conversions is defined by the ADCLK frequency and the AD<GP>SAMP register for each conversion group. The sample time needs to be determined by accounting for the external impedance connected to the input channel as well as the ADC's internal impedance.
- 25/ This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors, e.g the prescale settings.
- 26/ $1 \text{ LSB} = (\text{ADREFHI} - \text{ADREFLO}) / 2^{10}$ for 10-bit mode.
- 27/ $1 \text{ LSB} = (\text{ADREFHI} - \text{ADREFLO}) / 2^{12}$ for 12-bit mode.
- 28/ hr = High-resolution prescaler, configured using the HRPFC field of the Prescale Factor Register (HETPFR).
- 29/ lr = Loop-resolution prescaler, configured using the LFPRC field of the Prescale Factor Register (HETPFR).
- 30/ $t_{\text{RxAsymDelay}}$ parameter.
- 31/ These values do not include rise/fall times of the output buffer.
- 32/ The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
- 33/ The maximum $t_{\text{h}}(\text{SDA-SCLL})$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_{\text{w}}(\text{SCLL})$) of the SCL signal.
- 34/ C_{b} = The total capacitance of one bus line in pF.
- 35/ The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
- 36/ $t_{\text{c}}(\text{VCLK})$ = interface clock cycle time = $1 / f_{\text{VCLK}}$.
- 37/ For rise and fall timings, see Table 3-5 from manufacturer data sheet.
- 38/ When the SPI is in Master mode, the following must be true:
 For PS values from 1 to 255: $t_{\text{c}}(\text{SPC})_{\text{M}} \geq (\text{PS} + 1)t_{\text{c}}(\text{VCLK}) \geq 40\text{ns}$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
 For PS values of 0: $t_{\text{c}}(\text{SPC})_{\text{M}} = 2t_{\text{c}}(\text{VCLK}) \geq 40\text{ns}$.
 The external load on the SPICLK pin must be less than 60pF.
- 39/ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
- 40/ C2TDELAY and T2CDELAY is programmed in the SPIDELAY register.
- 41/ If the SPI is in slave mode, the following must be true: $t_{\text{c}}(\text{SPC})_{\text{S}} \geq (\text{PS} + 1) t_{\text{c}}(\text{VCLK})$, where PS = prescale value set in SPIFMTx.[15:8].
- 42/ When the SPI is in Slave mode, the following must be true:
 For PS values from 1 to 255: $t_{\text{c}}(\text{SPC})_{\text{S}} \geq (\text{PS} + 1)t_{\text{c}}(\text{VCLK}) \geq 40\text{ns}$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
 For PS values of 0: $t_{\text{c}}(\text{SPC})_{\text{S}} = 2t_{\text{c}}(\text{VCLK}) \geq 40\text{ns}$.
- 43/ If the SPI is in slave mode, the following must be true: $t_{\text{c}}(\text{SPC})_{\text{S}} \leq (\text{PS} + 1) t_{\text{c}}(\text{VCLK})$, where PS = prescale value set in SPIFMTx.[15:8].
- 44/ This is a discrepancy to IEEE 802.3, but is compatible with many PHY devices.

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Case X



Dimensions

Symbol	Millimeter		Symbol	Millimeter	
	Min	Max		Min	Max
A	1.19	1.40	D/E	15.90	16.10
A1	0.35	0.45	D1/E1	14.40	TYP
A2	0.84	0.95	e	0.80	BSC
b	0.45	0.55			

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.
4. Falls within JEDEC MO-275.

FIGURE 1. Case outline.

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	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W																														
19	VSS	VSS	TMS	N2HET1 [10]	MIBSP15 NCS[0]	MIBSP11 SMO	MIBSP11 NENA	MIBSP16 CLK	MIBSP16 SMO[0]	N2HET1 [28]	DMM_DATA[0]	CAN3RX	AD1EV7	AD1N11R / AD2N11R	AD1N22R / AD2N22R	AD1N [06]	AD1N11R / AD2N11R	VSSAD	VSSAD	19																													
18	VSS	TCK	TDO	nTRST	N2HET1 [08]	MIBSP11 CLK	MIBSP11 SOMI	MIBSP16 NENA	MIBSP16 SOMI[0]	N2HET1 [30]	DMM_DATA[1]	CAN3TX	NC	AD1N11R / AD2N11R	AD1N11R / AD2N11R	AD1N11R / AD2N11R	AD1N [04]	AD1N [02]	VSSAD	18																													
17	TDI	RST	EMF_ADDR[2]	EMF_nWE	MIBSP16 SOM[1]	DMM_CLK	MIBSP16 SIMO[3]	MIBSP16 SIMO[2]	N2HET1 [31]	EMF_nCS[3]	EMF_nCS[2]	EMF_nCS[4]	EMF_nCS[0]	NC	AD1N [05]	AD1N [03]	AD1N11R / AD2N11R	AD1N [01]	AD1N11R / AD2N11R	17																													
16	RTCK	FRAY_TXEN1	EMF_ADDR[2]	EMF_BA[1]	MIBSP16 SIMO[1]	DMM_NENA	MIBSP16 SOM[3]	MIBSP16 SOMI[2]	DMM_SYNC	NC	NC	NC	NC	NC	AD1N23R / AD2N23R	AD1N11R / AD2N11R	AD1N11R / AD2N11R	ADREFLO	VSSAD	16																													
15	FRAY_RX1	FRAY_TX1	EMF_ADDR[19]	EMF_ADDR[18]	ETM_DATA[0]	ETM_DATA[0]	ETM_DATA[4]	ETM_DATA[3]	ETM_DATA[2]	ETM_DATA[18] / EMP_DATA[0]	ETM_DATA[17] / EMP_DATA[1]	ETM_DATA[16] / EMP_DATA[2]	ETM_DATA[15] / EMP_DATA[3]	NC	NC	AD1N21R / AD2N21R	AD1N20R / AD2N20R	ADREFH	VCCAD	15																													
14	N2HET1 [26]	nERROR	EMF_ADDR[17]	EMF_ADDR[16]	ETM_DATA[0]	VCCIO	VCCIO	VCCIO	VCC	VCC	VCCIO	VCCIO	VCCIO	VCCIO	NC	NC	AD1N11R / AD2N11R	AD1N [07]	AD1N [0]	14																													
13	N2HET1 [17]	N2HET1 [19]	EMF_ADDR[15]	NC	ETM_DATA[12] / EMP_BA[0]	VCCIO	<table border="1"> <tr> <td>VSS</td> <td>VSS</td> <td>VCC</td> <td>VSS</td> <td>VSS</td> </tr> <tr> <td>VSS</td> <td>VSS</td> <td>VSS</td> <td>VSS</td> <td>VSS</td> </tr> <tr> <td>VCC</td> <td>VSS</td> <td>VSS</td> <td>VSS</td> <td>VCC</td> </tr> <tr> <td>VSS</td> <td>VSS</td> <td>VSS</td> <td>VSS</td> <td>VSS</td> </tr> <tr> <td>VSS</td> <td>VSS</td> <td>VCC</td> <td>VSS</td> <td>VSS</td> </tr> <tr> <td>VSS</td> <td>VSS</td> <td>VCC</td> <td>VSS</td> <td>VSS</td> </tr> </table>						VSS	VSS	VCC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC	VSS	VSS	VSS	VCC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC	VSS	VSS	VSS	VSS	VCC	VSS	VSS	VCCIO	ETM_DATA[0]	NC	AD1N11R / AD2N11R	AD1N11R / AD2N11R	NC	13
VSS	VSS	VCC	VSS	VSS																																													
VSS	VSS	VSS	VSS	VSS																																													
VCC	VSS	VSS	VSS	VCC																																													
VSS	VSS	VSS	VSS	VSS																																													
VSS	VSS	VCC	VSS	VSS																																													
VSS	VSS	VCC	VSS	VSS																																													
12	ECLK	N2HET1 [04]	EMF_ADDR[14]	NC	ETM_DATA[13] / EMP_nCS	VCCIO	VCCIO	ETM_DATA[0]	MIBSP15 NCS[3]	NC	NC	NC	12																																				
11	N2HET1 [14]	N2HET1 [30]	EMF_ADDR[13]	NC	ETM_DATA[14] / EMP_nCS[1]	VCCIO	VCCIO	VCCPLL	ETM_TRACE_CTL	NC	NC	NC	11																																				
10	CAN1TX	CAN1RX	EMF_ADDR[12]	NC	ETM_DATA[15] / EMP_nCS[2]	VCC	VCC	VCC	VSS	VSS	VCC	VCC	VCCIO	ETM_TRACE_CLKOUT	NC	NC	MIBSP16 NCS[2]	GPIO[3]	10																														
9	N2HET1 [27]	FRAY_TXEN2	EMF_ADDR[11]	NC	ETM_DATA[0] / EMP_ADDR[0]	VCC	VCCIO	ETM_TRACE_CLKIN	NC	NC	MIBSP16 CLK	MIBSP16 NENA	9																																				
8	FRAY_RX2	FRAY_TX2	EMF_ADDR[10]	NC	ETM_DATA[0] / EMP_ADDR[4]	VCCP	VCCIO	VCCIO	ETM_DATA[0] / EMP_DATA[10]	NC	NC	MIBSP16 SOMI	MIBSP16 SMO	8																																			
7	LINRX	LINTX	EMF_ADDR[9]	NC	ETM_DATA[0] / EMP_ADDR[8]	VCCIO	VCCIO	VCCIO	ETM_DATA[0] / EMP_DATA[14]	NC	NC	N2HET1 [09]	nPORST	7																																			
6	GPIO[4]	MIBSP16 NCS[1]	EMF_ADDR[8]	NC	ETM_DATA[1] / EMP_DATA[2]	VCCIO	VCCIO	VCCIO	VCC	VCC	VCCIO	VCCIO	VCCIO	VCCIO	ETM_DATA[2] / EMP_DATA[13]	NC	NC	N2HET1 [05]	MIBSP16 NCS[2]	6																													
5	GPIO[3]	GPIO[5]	EMF_ADDR[7]	EMF_ADDR[6]	ETM_DATA[0] / EMP_DATA[4]	ETM_DATA[2] / EMP_DATA[5]	ETM_DATA[2] / EMP_DATA[6]	FLTP2	FLTP1	ETM_DATA[23] / EMP_DATA[7]	ETM_DATA[24] / EMP_DATA[8]	ETM_DATA[25] / EMP_DATA[9]	ETM_DATA[26] / EMP_DATA[10]	ETM_DATA[27] / EMP_DATA[11]	ETM_DATA[28] / EMP_DATA[12]	NC	NC	MIBSP16 NCS[1]	N2HET1 [02]	5																													
4	N2HET1 [16]	N2HET1 [12]	EMF_ADDR[6]	EMF_ADDR[5]	NC	NC	NC	N2HET1 [21]	N2HET1 [23]	NC	NC	NC	NC	NC	EMF_nCS[5]	NC	NC	NC	NC	4																													
3	N2HET1 [29]	N2HET1 [22]	MIBSP16 NCS[5]	SP12 NENA	N2HET1 [11]	MIBSP11 NCS[1]	MIBSP11 NCS[2]	GPIO[8]	MIBSP11 NCS[3]	EMF_CLK	EMF_CK[2]	N2HET1 [25]	SP12 NCS[0]	EMF_nWAIT	EMF_nRAS	NC	NC	NC	N2HET1 [06]	3																													
2	VSS	MIBSP16 NCS[2]	GPIO[1]	SP12 SOMI	SP12 CLK	GPIO[2]	GPIO[5]	CAN2TX	GPIO[8]	GPIO[1]	KELVIN_GND	GPIO[9]	N2HET1 [13]	N2HET1 [20]	MIBSP11 NCS[3]	NC	TEST	N2HET1 [01]	VSS	2																													
1	VSS	VSS	GPIO[2]	SP12 SMO	GPIO[3]	GPIO[7]	GPIO[4]	CAN2RX	N2HET1 [18]	OSCON	OSCOU7	GPIO[7]	N2HET1 [15]	N2HET1 [24]	NC	N2HET1 [07]	N2HET1 [03]	VSS	VSS	1																													

FIGURE 2. Terminal connections.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13629
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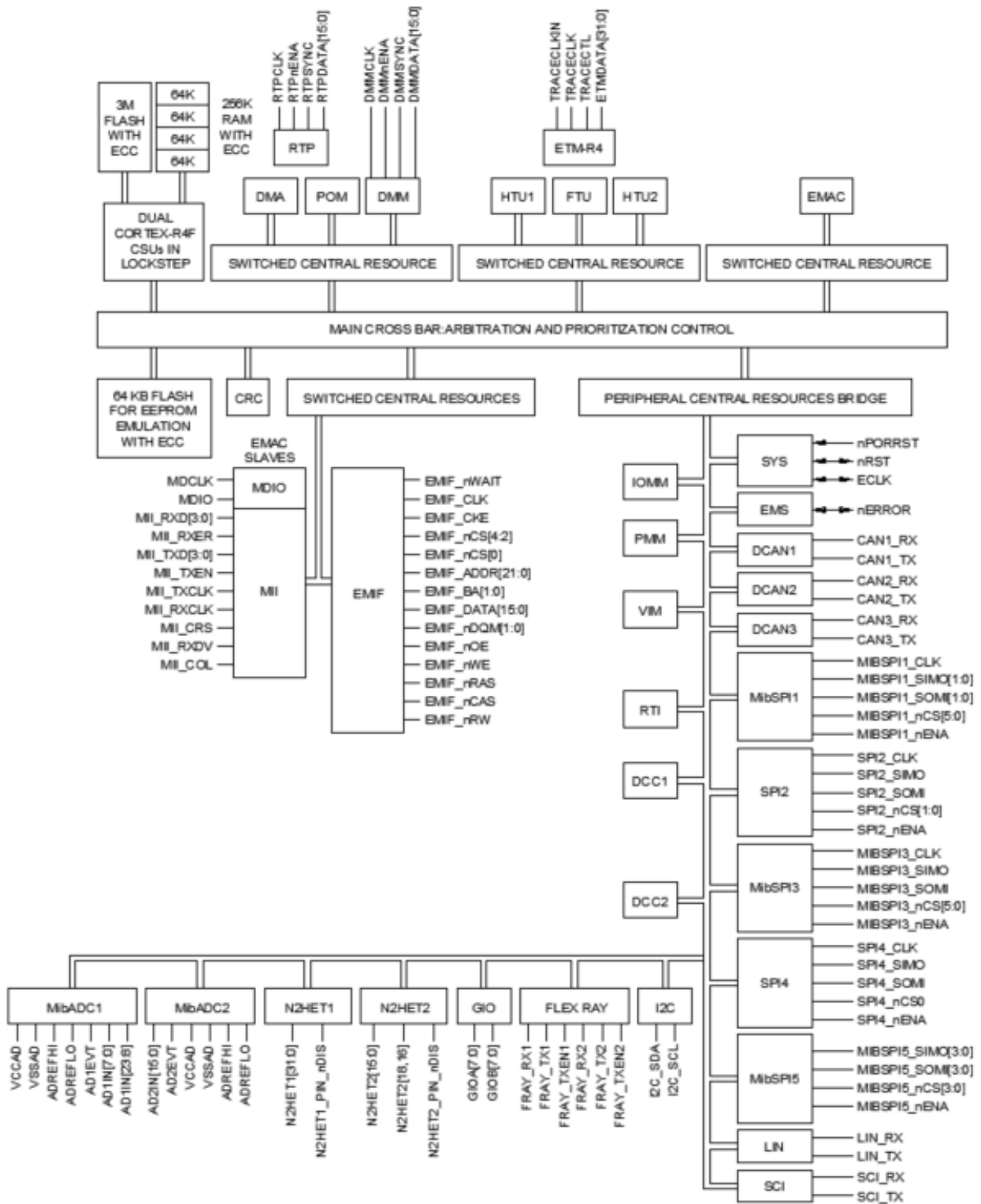


FIGURE 3. Functional block diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13629
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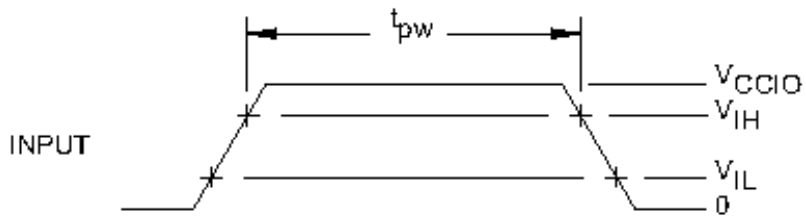


FIGURE 4. TTL-Level inputs

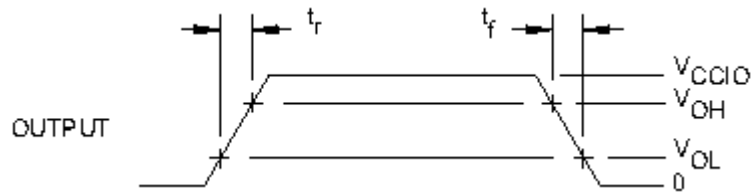


FIGURE 5. CMOS level outputs.

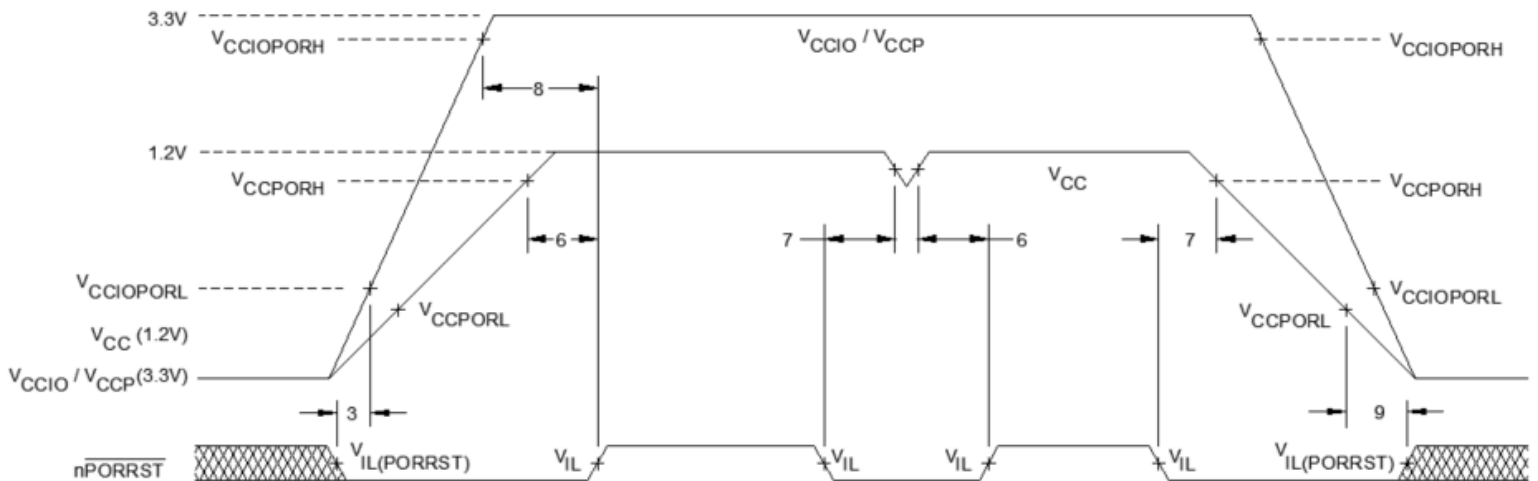


FIGURE 6. nPORRST timing diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13629
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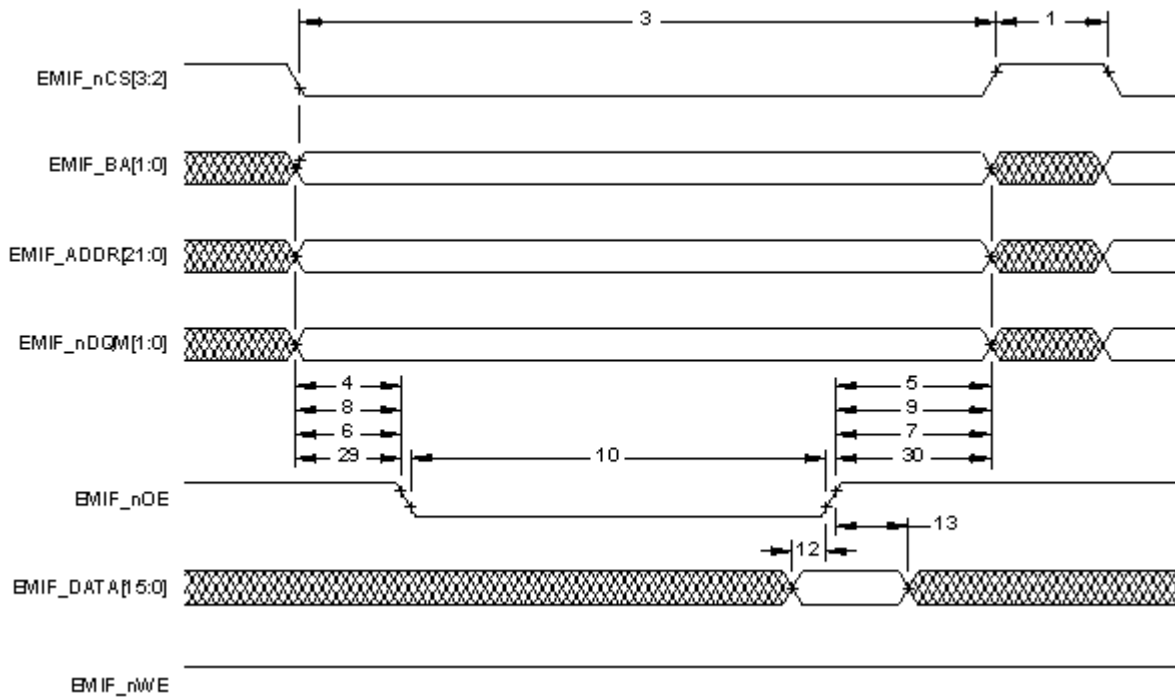


FIGURE 7. Asynchronous memory Read timing.

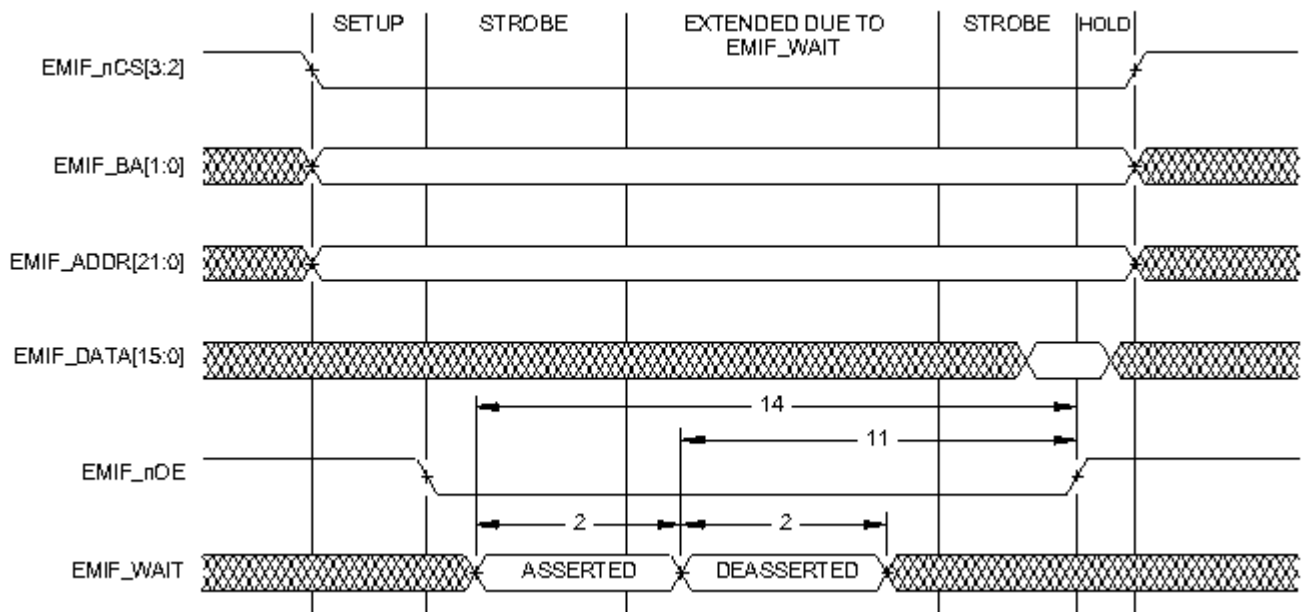


FIGURE 8. EMIFnWAIT Read timing requirements.

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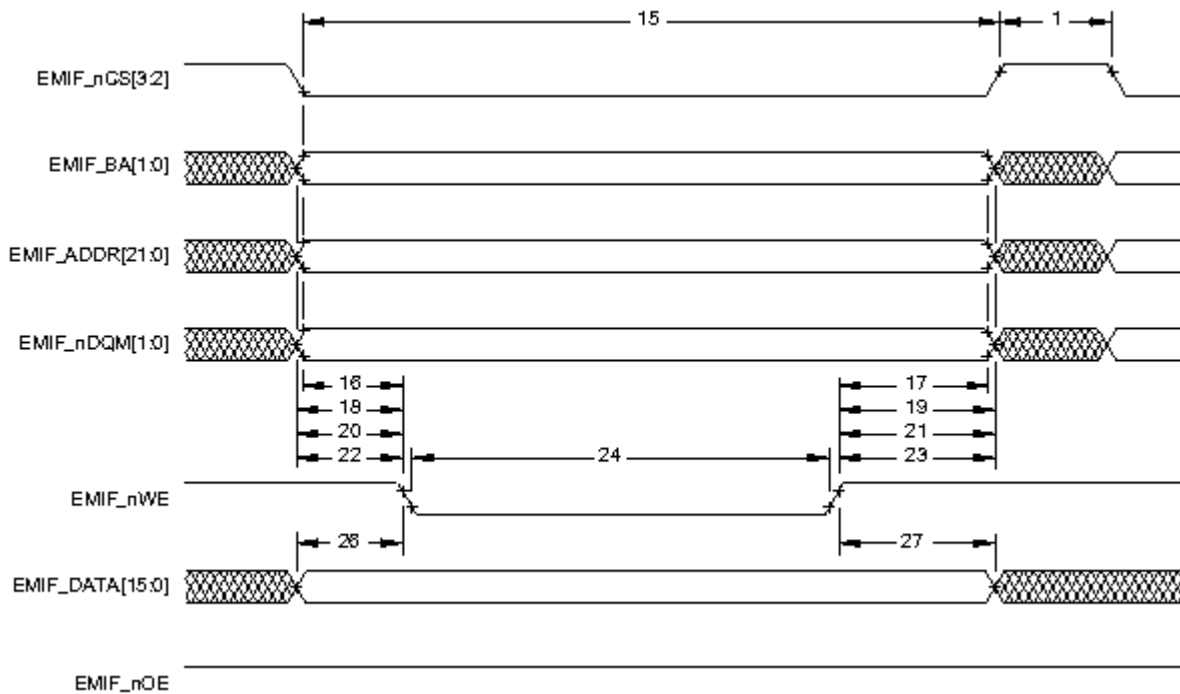


FIGURE 9. Asynchronous memory Write timing.

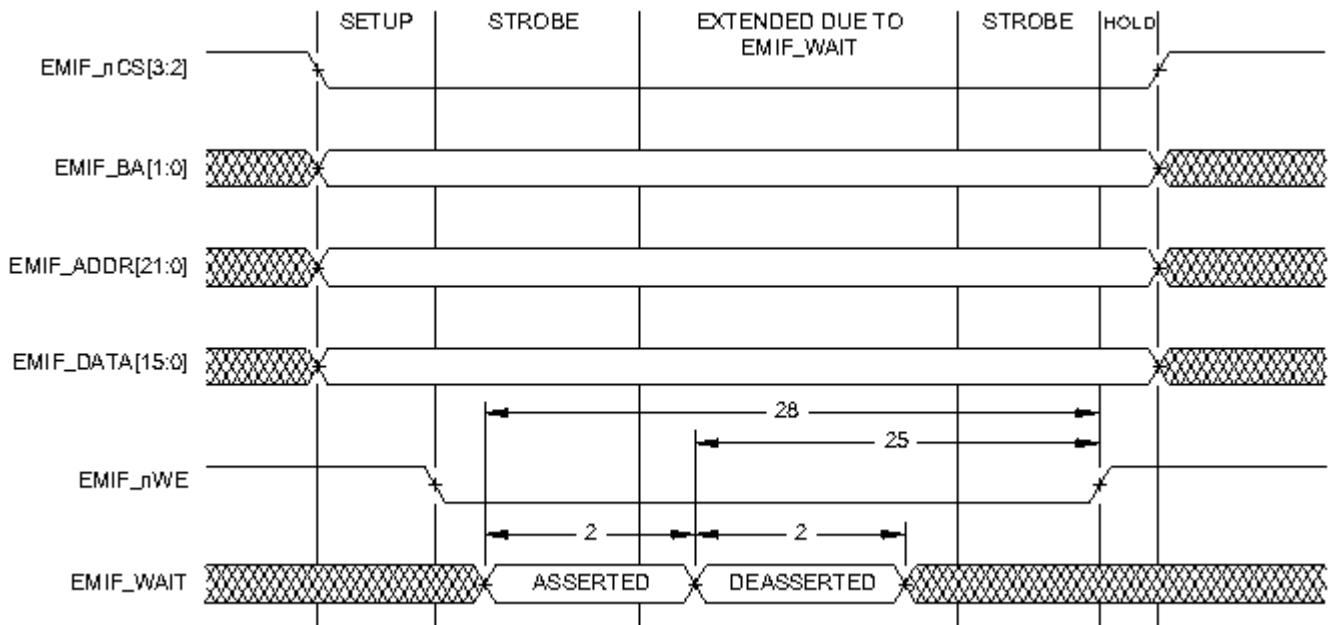


FIGURE 10. EMIFnWAIT Write timing requirements.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13629
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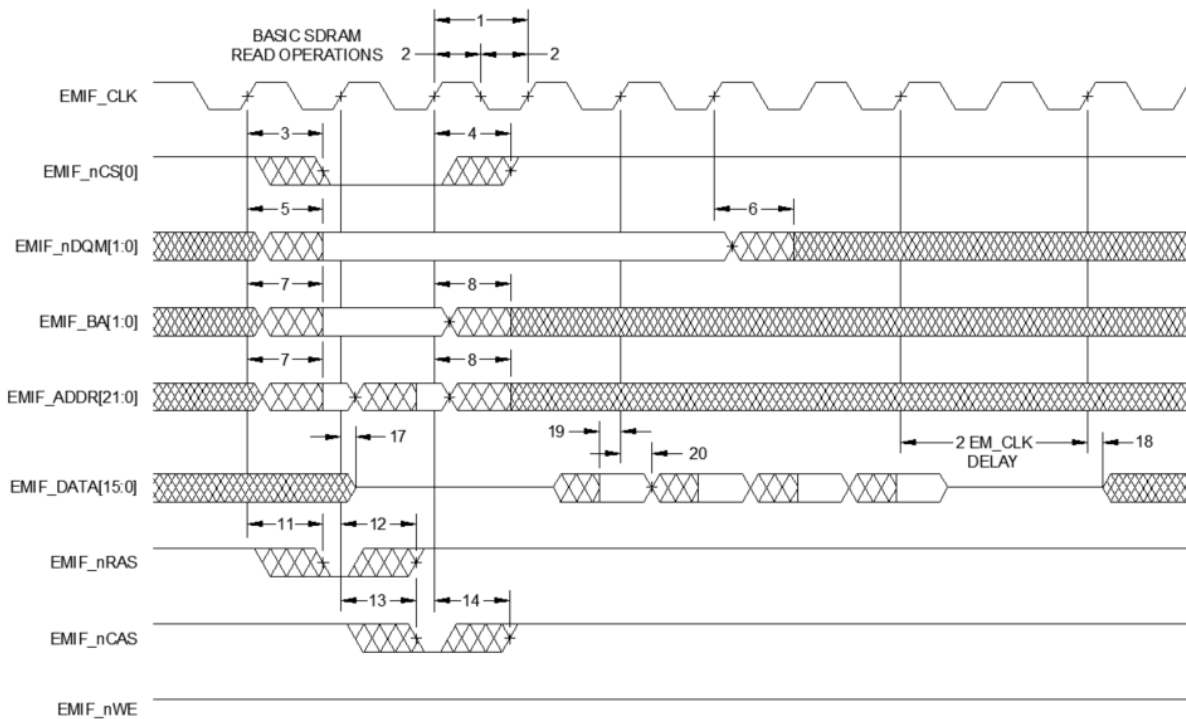


FIGURE 11. Basic SDRAM Read operation.

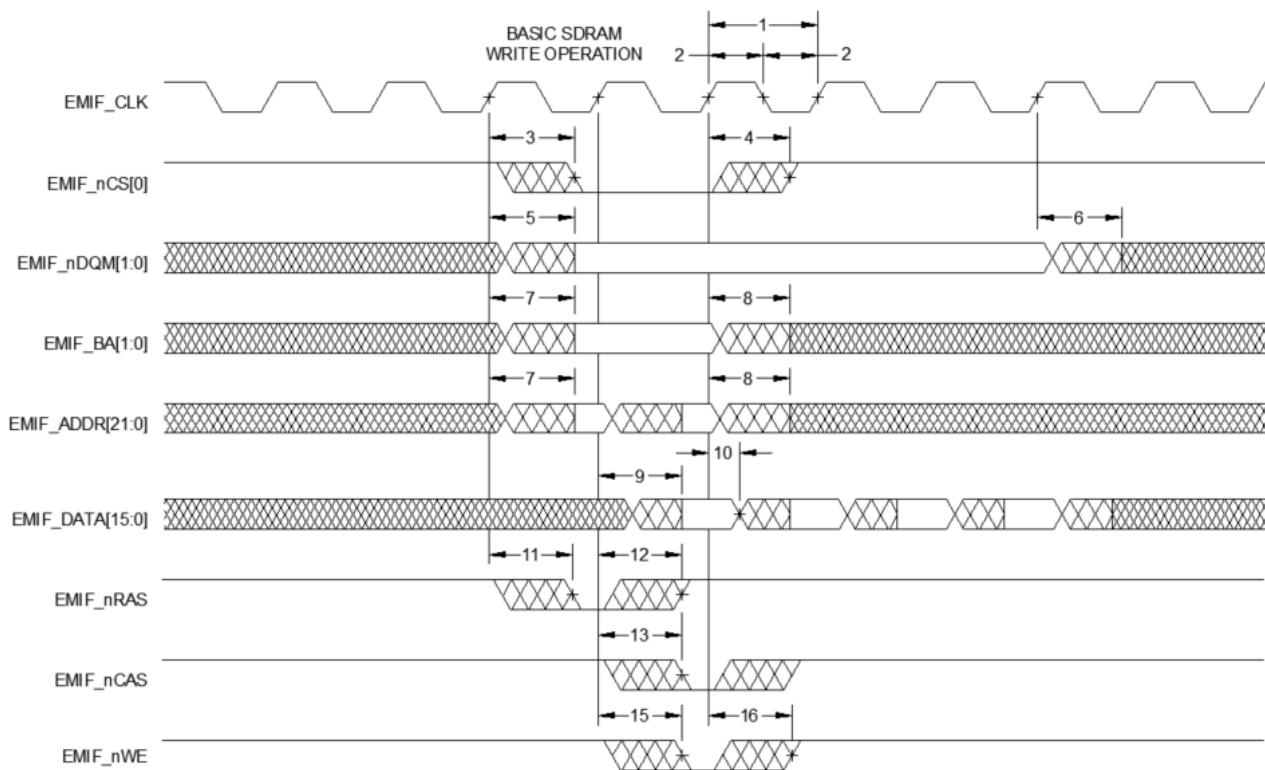


FIGURE 12. Basic SDRAM Write operation.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13629
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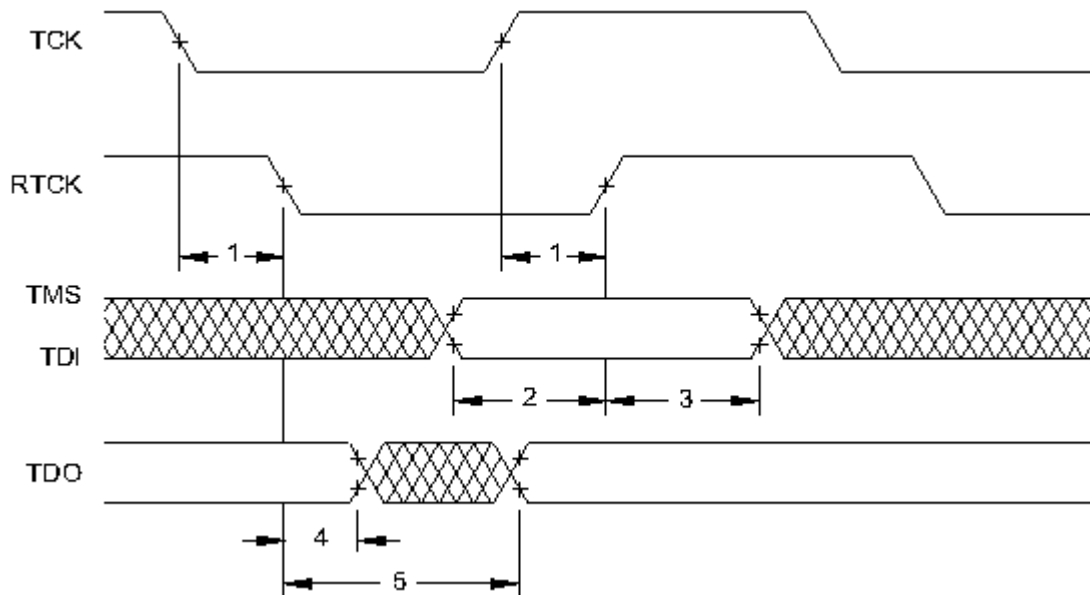


FIGURE 13. JTAG timing.

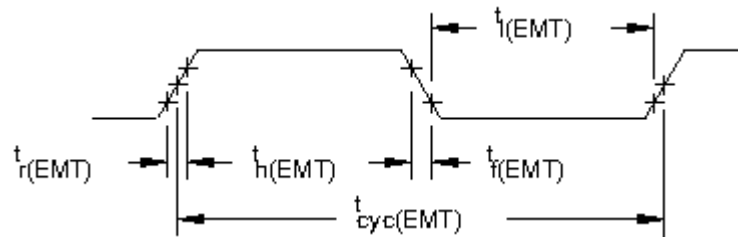


FIGURE 14. ETMTRACECLK timing.

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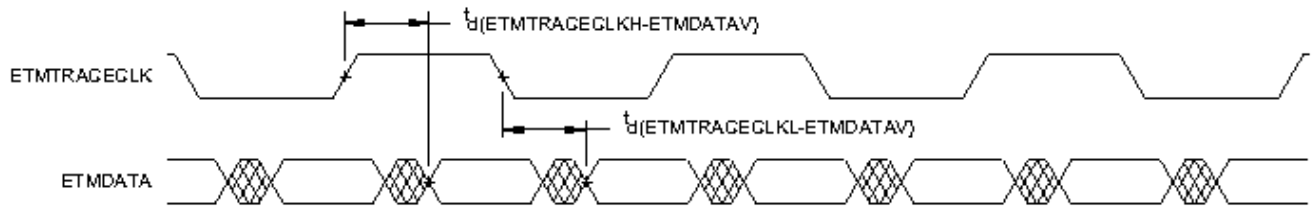


FIGURE 15. ETMDATA timing.

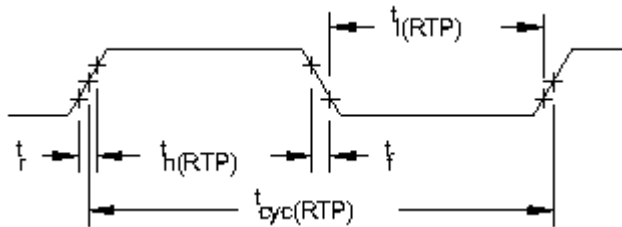


FIGURE 16. RTPCLK timing.

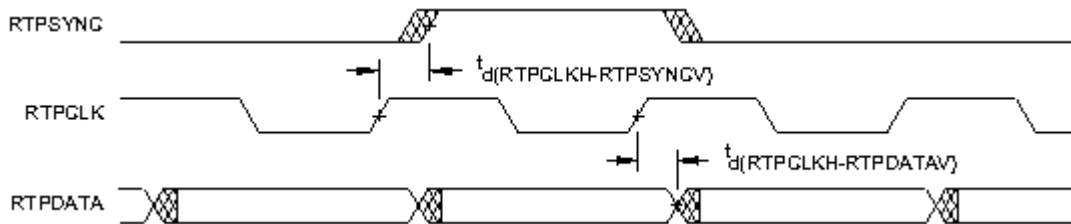


FIGURE 17. RTPDATA timing.

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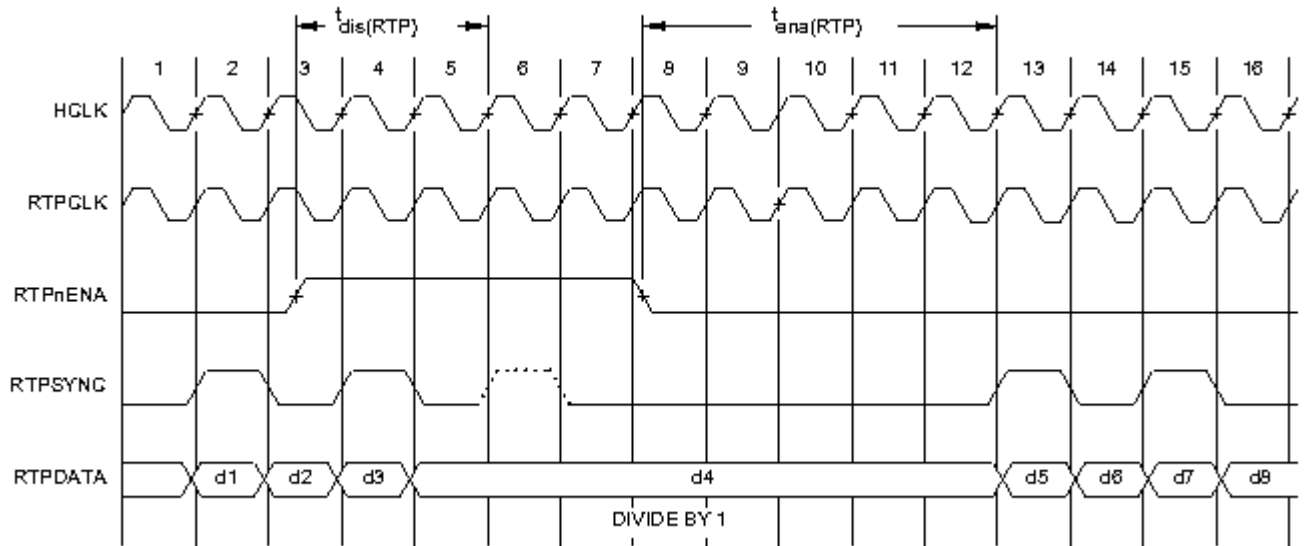


FIGURE 18. RTPnENA timing.

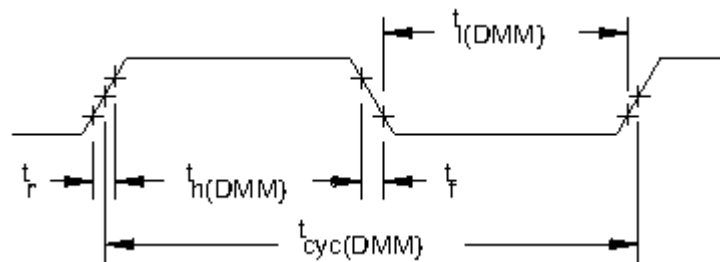


FIGURE 19. DMMCLK timing.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13629
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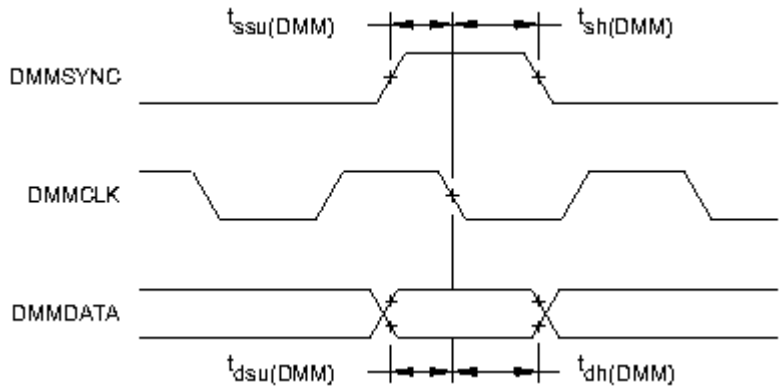


FIGURE 20. DMMDATA timing.

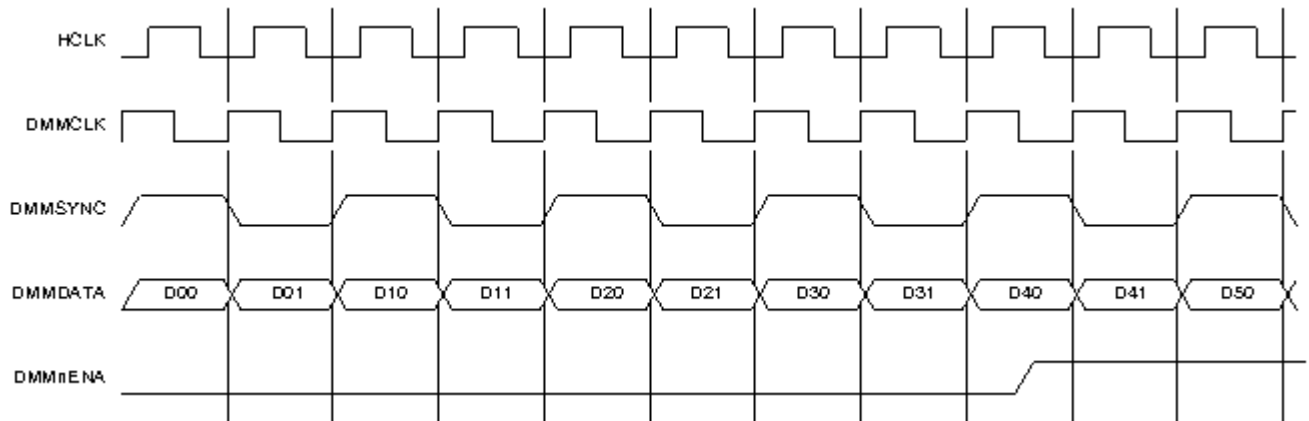


FIGURE 21. DMMnENA timing.

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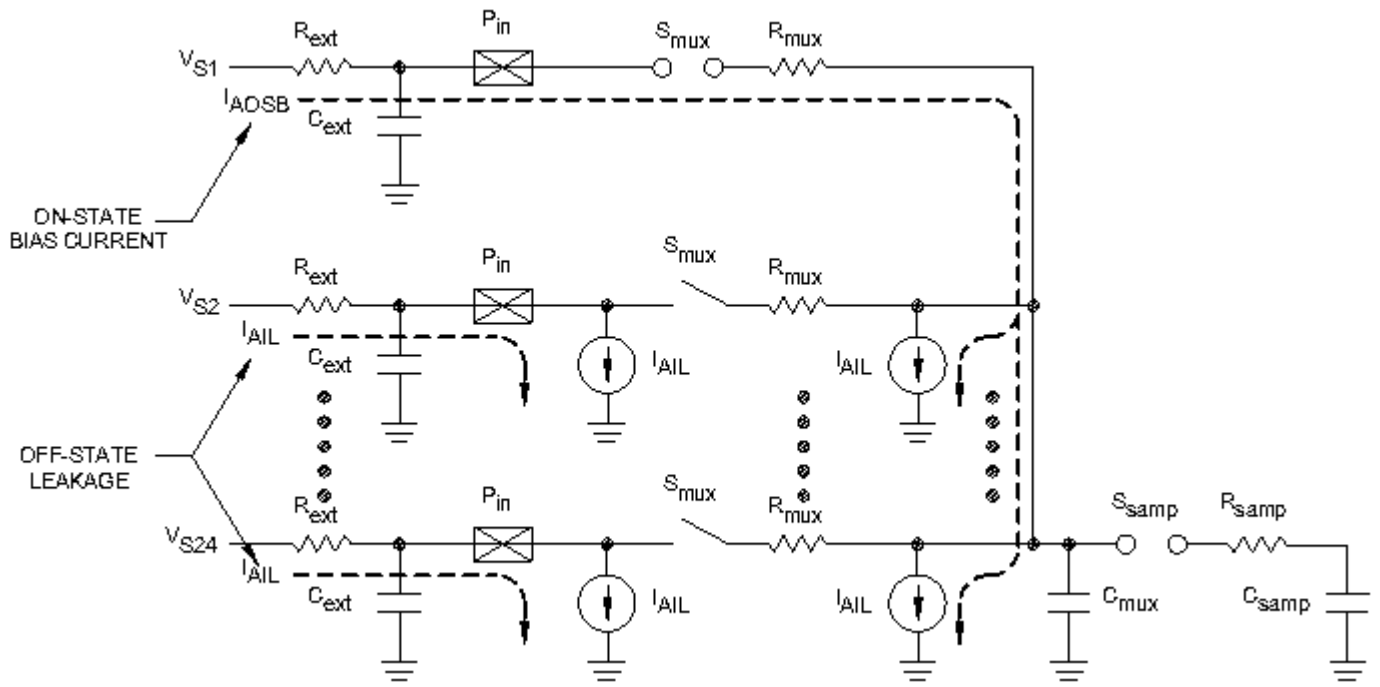


FIGURE 22. MibADC input equivalent circuit. Figure 5-1

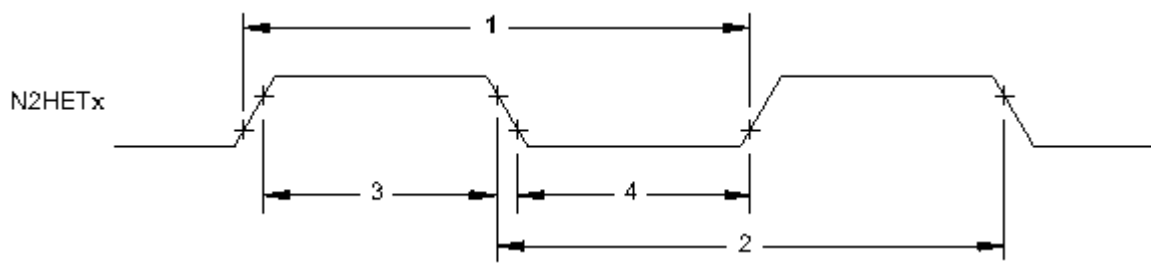


FIGURE 23. N2HET input captive timings.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13629
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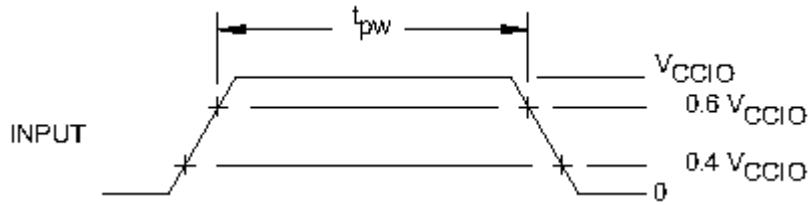


FIGURE 24. FlexRay inputs. Figure 5-8

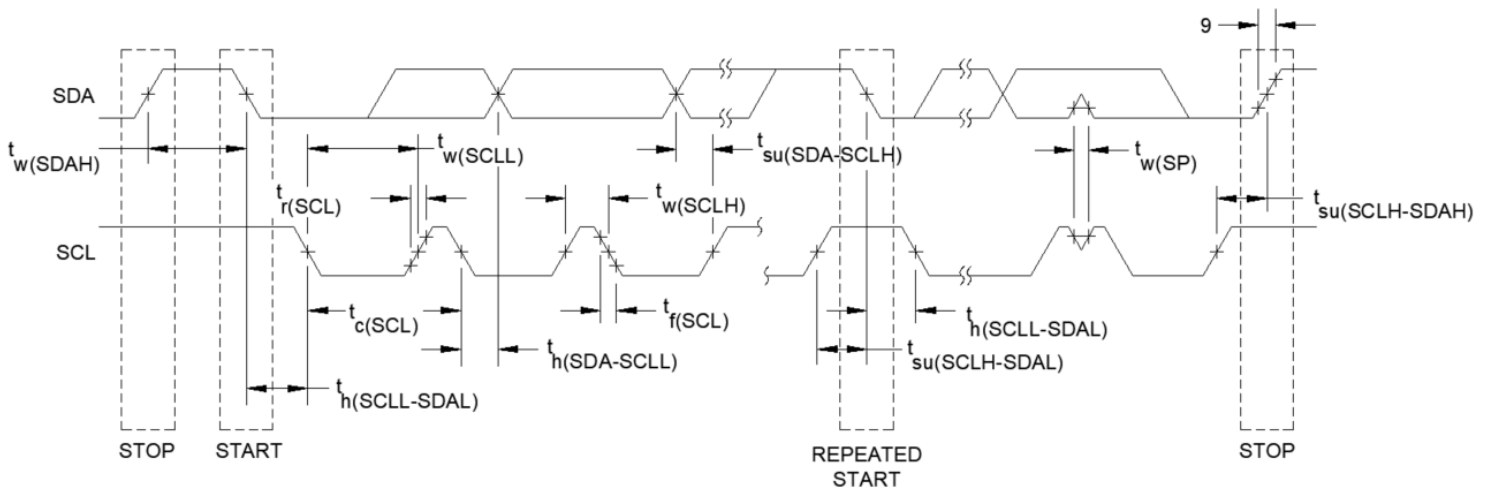


FIGURE 25. I2C timings.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13629
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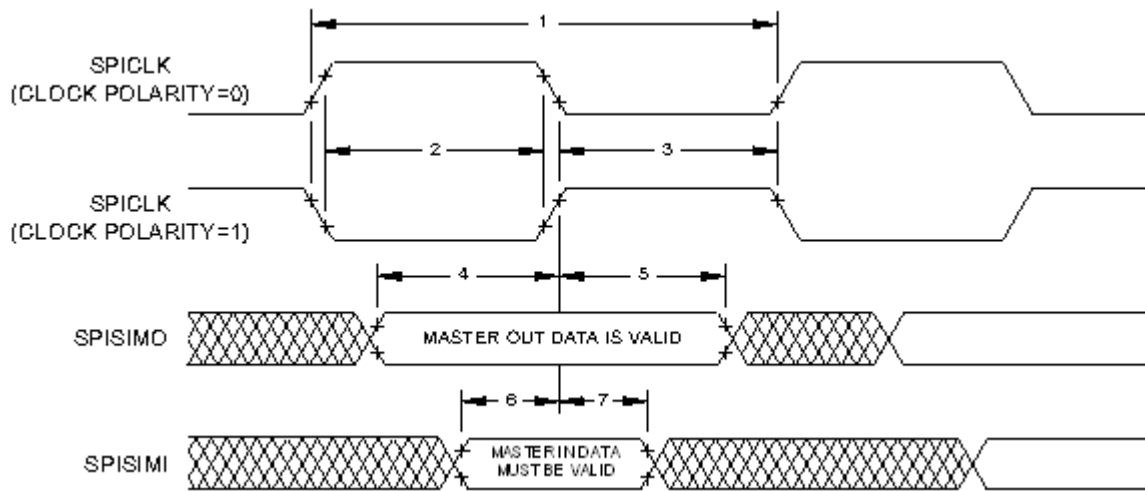


FIGURE 26. SPI Master mode external timing (Clock phase = 0).

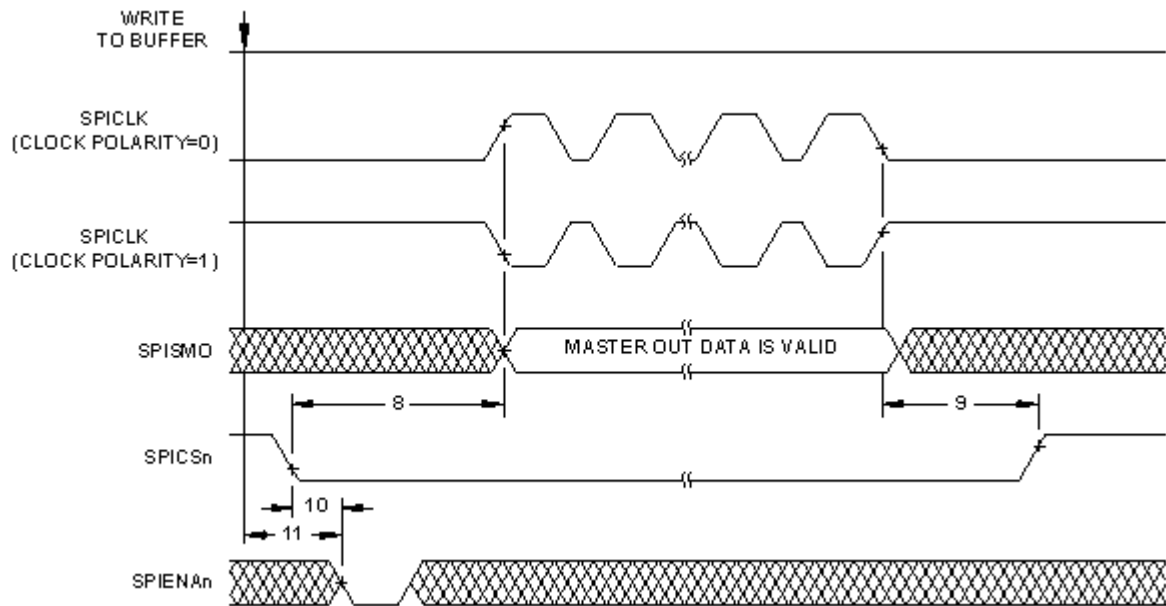


FIGURE 27. SPI Master mode chip select timing (Clock phase = 0).

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13629
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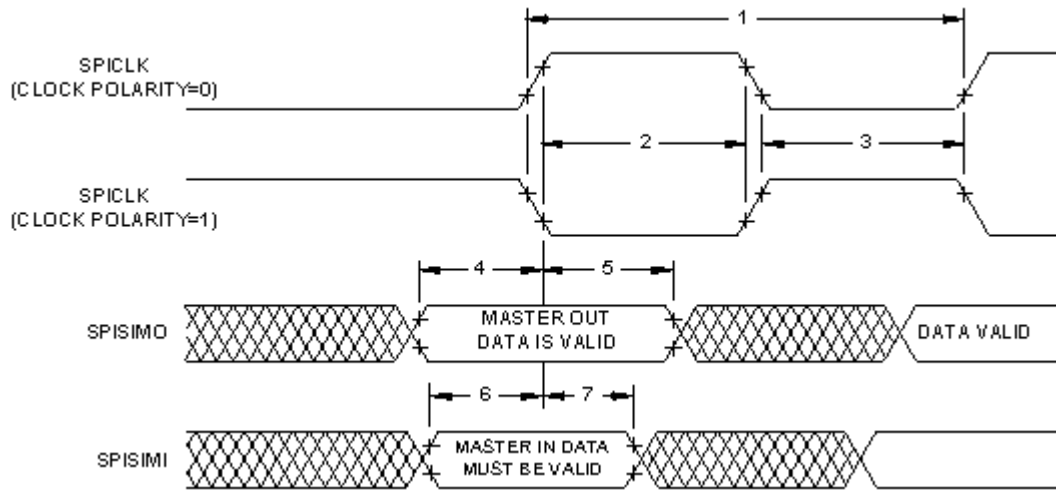


FIGURE 28. SPI Master mode external timing (clock phase = 1).

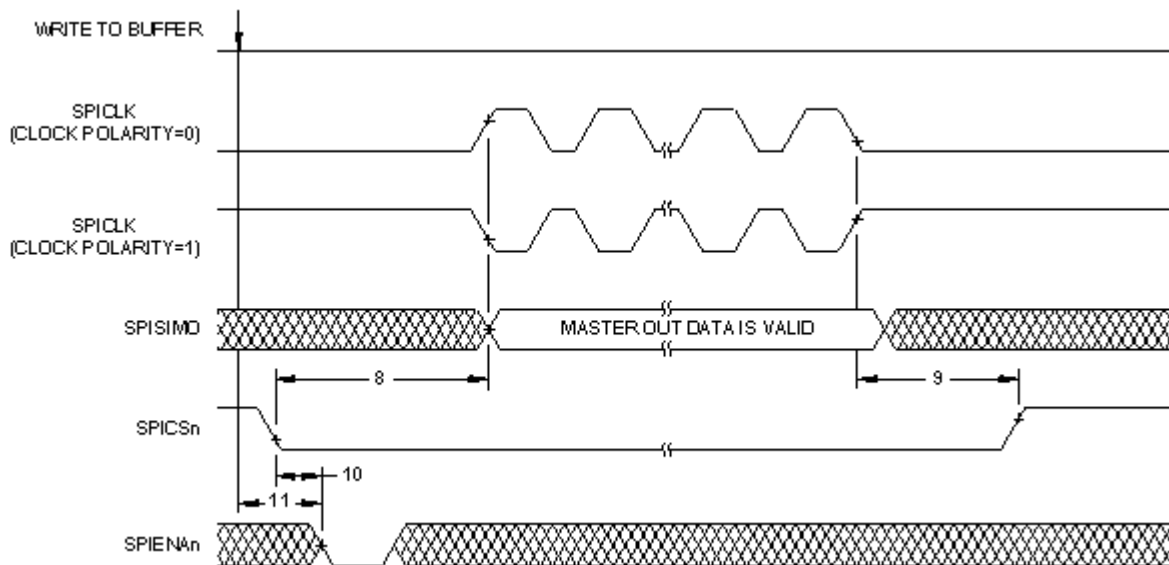


FIGURE 29. SPI Master mode chip select timing (clock phase = 1).

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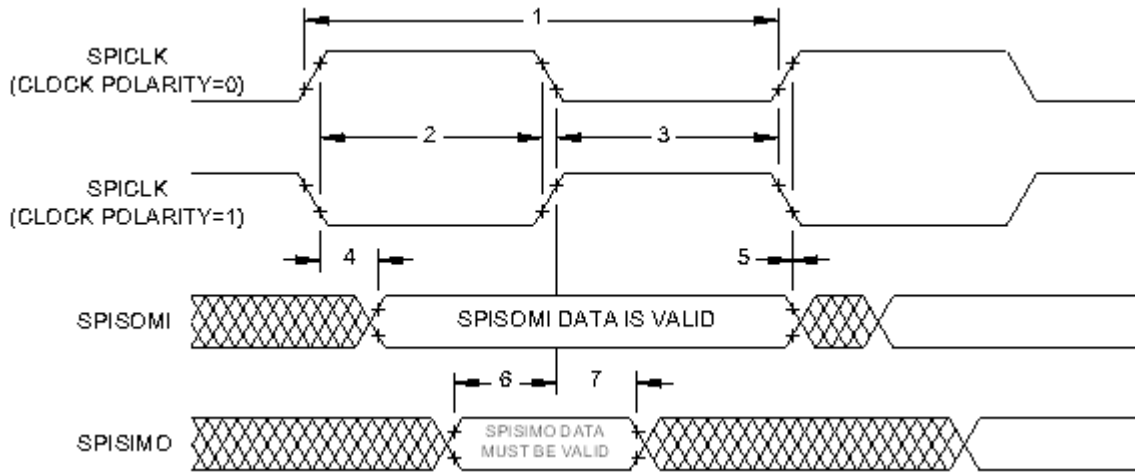


FIGURE 30. SPI Slave mode external timing (Clock phase = 0).

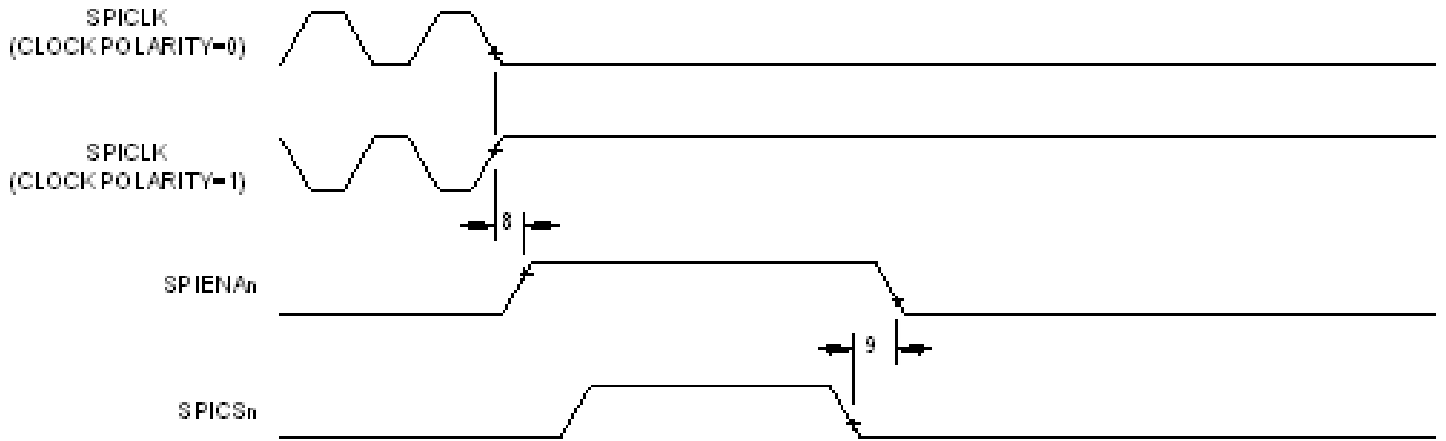


FIGURE 31. SPI Slave mode Enable timing (Clock phase = 0).

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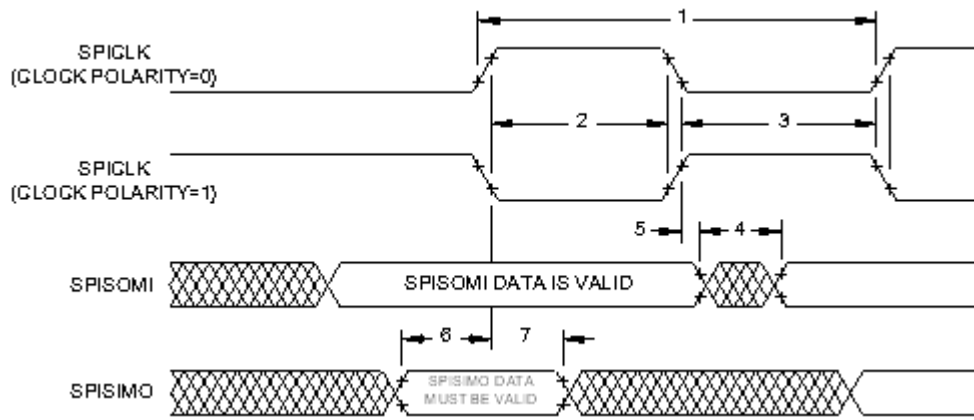


FIGURE 32. SPI Slave mode external timing (Clock phase = 1).

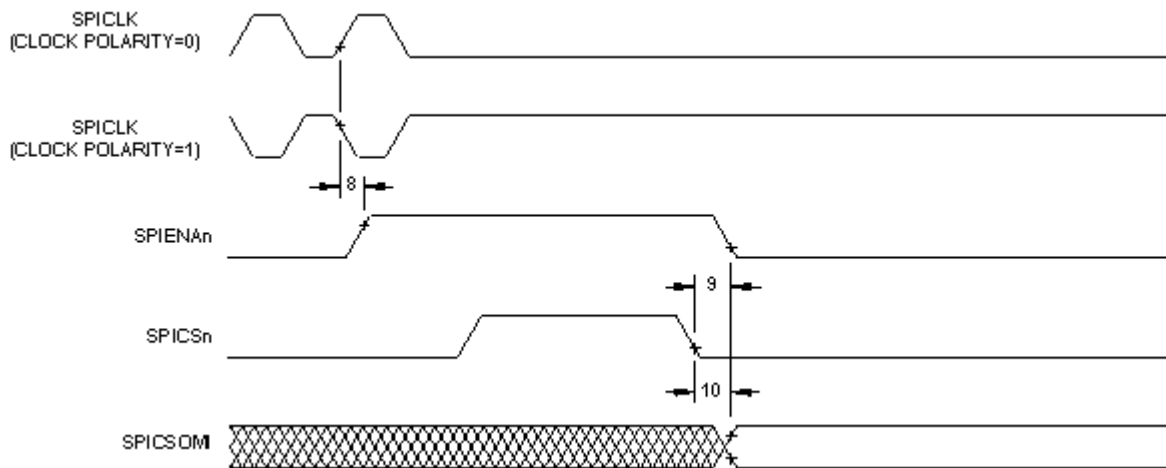


FIGURE 33. SPI Slave mode Enable timing (Clock phase = 1).

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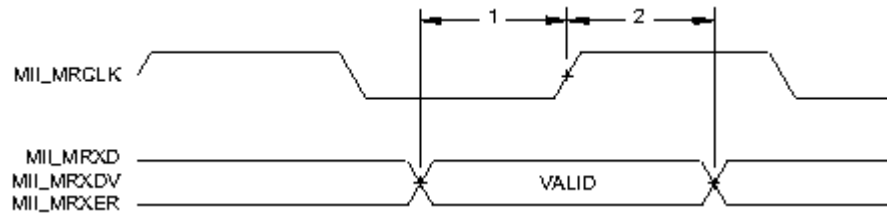


FIGURE 34. MII receive timings.

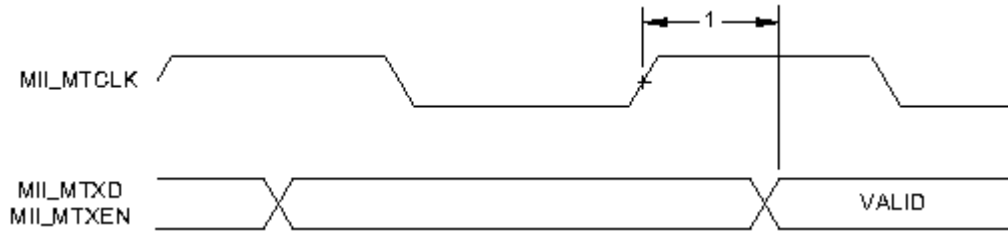


FIGURE 35. MII Transmit timing.

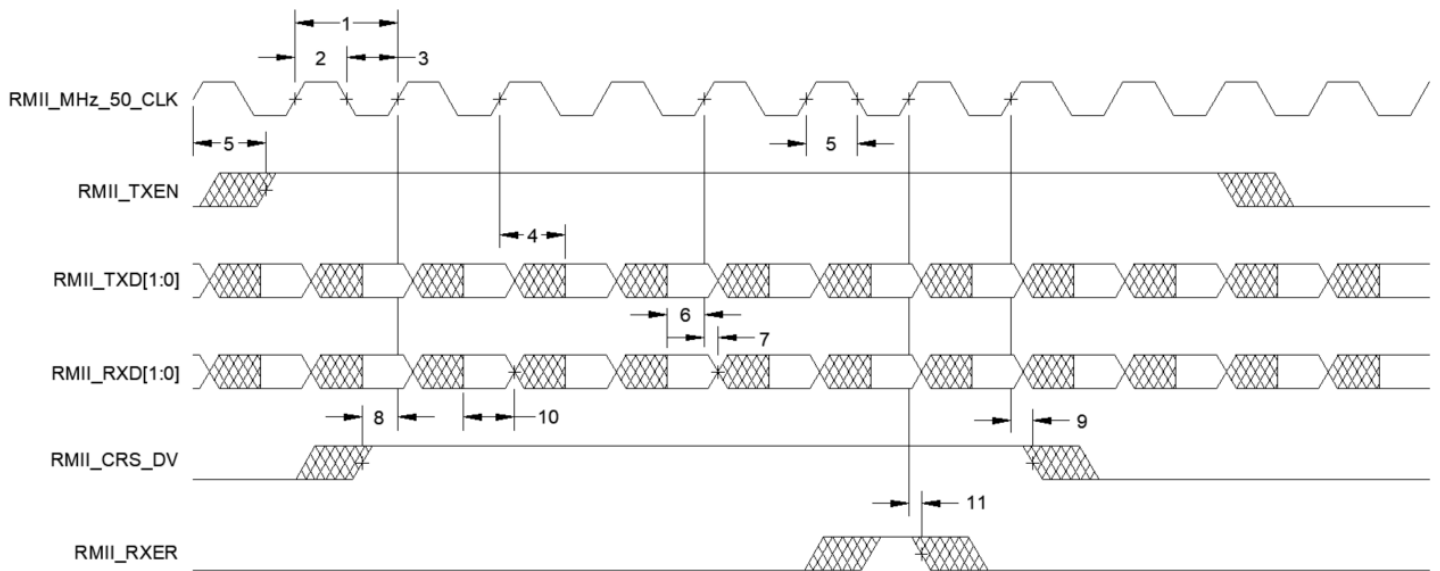


FIGURE 36. RMII timing diagram.

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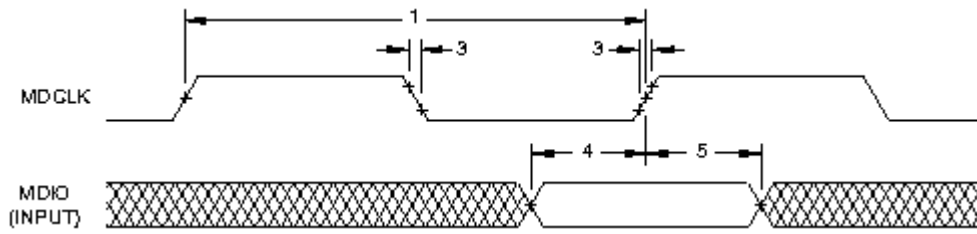


FIGURE 37. MDIO input timings.

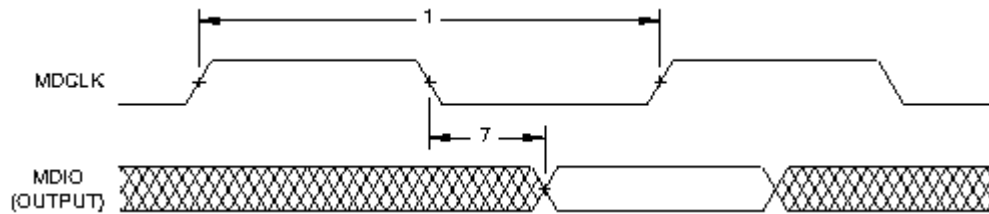


FIGURE 38 MDIO output timing.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/13629-01XE	<u>2/</u>	TMS5703137CZWTQEP
V62/13629-02XE	<u>2/</u>	TMS5703137CGWTMEP
V62/13629-01XF <u>3/</u>	01295	TMS5703137CZWTQEP
V62/13629-02XF <u>3/</u>	01295	TMS5703137CGWTMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Not available from an approved source of supply.

3/ Devices listed on this drawing are supplied to lead finish "F". The solder ball material contains compositions of: Sn = 63%, Pb = 34.5%, Ag = 2%, and Sb = 0.5% .

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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