REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update document paragraphs to current requirements. - ro	19-02-13	C. SAFFLE
B	Delete paragraph 1.5 and add the θ_{JA} limit to paragraph 1.3. Delete the COPLANARITY limit from A2 dimension as specified under Figure 1. Update document to current requirements. - ro	24-04-03	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B								
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14								

PMIC N/A

Original date of drawing
YY-MM-DD
13-09-18

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TITLE
MICROCIRCUIT, LINEAR, LOW POWER INSTRUMENTATION AMPLIFIER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/13625
REV B		PAGE 1 OF 14

AMSC N/A

5962-V033-24

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low power instrumentation amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13625	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type.

Device type	Generic	Circuit function
01	AD8421-EP	Low power instrumentation amplifier

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MO-187-AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_S)	±18 V
Output short circuit duration	Indefinite
Maximum voltage at –IN or +IN	$-V_S$ + 40 V 2/
Minimum voltage at –IN or +IN	$+V_S$ – 40 V
Maximum voltage at REF	$+V_S$ + 0.3 V 3/
Minimum voltage at REF	$-V_S$ – 0.3 V
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum junction temperature range (T_J)	+150°C
Thermal resistance, junction to ambient (θ_{JA})	138.6°C/W
Electrostatic discharge (ESD):	
Human body model (HBM)	2 kV
Charged device model (CDM)	1.25 kV
Machine model (MM)	0.2 kV

1.4 Recommended operating conditions. 4/

Supply voltage range (V_S)	±15 V
Operating temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ For voltages beyond these limits, use input protection resistors. See manufacturer’s data sheet for more information.

3/ There are ESD protection diodes from the reference input to each supply, so REF cannot be driven beyond the supplies in the same way that +IN and –IN can. See manufacturer’s data sheet for more information.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Common mode rejection ratio							
CMRR dc to 60 Hz with 1 kΩ source imbalance		G = 1, V_{CM} = -10 V to +10 V	+25°C	01	84		dB
			-55°C to +125°C		80		
		G = 10, V_{CM} = -10 V to +10 V	+25°C		104		
		G = 100, V_{CM} = -10 V to +10 V	+25°C		124		
		G = 1000, V_{CM} = -10 V to +10 V	+25°C		134		
CMRR at 20 kHz		G = 1, V_{CM} = -10 V to +10 V	+25°C		80		
		G = 10, V_{CM} = -10 V to +10 V	+25°C		90		
		G = 100, V_{CM} = -10 V to +10 V	+25°C		100		
		G = 1000, V_{CM} = -10 V to +10 V	+25°C		100		
Noise							
Voltage noise 3/							
Input voltage noise	e_{ni}	1 kHz, V_{IN+}, V_{IN-} = 0 V	+25°C	01		3.2	nV / $\sqrt{Hz}$
					3 typical		
Output voltage noise	e_{no}	1 kHz, V_{IN+}, V_{IN-} = 0 V	+25°C	01		60	nV / $\sqrt{Hz}$
Peak to peak	RTI	G = 1, f = 0.1 Hz to 10 Hz	+25°C	01	2 typical		μVp-p
		G = 10, f = 0.1 Hz to 10 Hz			0.5 typical		
		G = 100 to 1000, f = 0.1 Hz to 10 Hz			0.07 typical		
Current noise spectral density		f = 1 kHz	+25°C	01	200 typical		fA/ $\sqrt{Hz}$
Current noise peak to peak	RTI	f = 0.1 Hz to 10 Hz	+25°C	01	18 typical		pAp-p

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Voltage offset 4/							
Input offset voltage	V_{OSI}	V_S = ±5 V to ±15 V	+25°C	01		70	µV
			-55°C to +125°C			160	
Input offset voltage average temperature coefficient	ΔV_{OSI}		-55°C to +125°C	01		0.9	µV/°C
Output offset voltage	V_{OSO}	V_S = ±5 V to ±15 V	+25°C	01		600	µV
			-55°C to +125°C			1.5	mV
Output offset voltage average temperature coefficient	ΔV_{OSO}		-55°C to +125°C	01		9	µV/°C
Offset referred to input (RTI) versus supply	PSR	G = 1, V_S = ±2.5 V to ±18 V	+25°C	01	90		dB
					120 typical		
		G = 10, V_S = ±2.5 V to ±18 V			110		
					120 typical		
		G = 100, V_S = ±2.5 V to ±18 V			124		
					130 typical		
		G = 1000, V_S = ±2.5 V to ±18 V			130		
					140 typical		
Input current							
Input bias current	I_{IB}		+25°C	01		2	nA
					1 typical		
			-55°C to +125°C			8	
Input bias current average temperature coefficient	ΔI_{IB}		-55°C to +125°C	01	50 typical		pA/°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input current – continued.							
Input offset current	I_{IO}		+25°C	01		2	nA
					0.5 typical		
			-55°C to +125°C			3	
Input offset current average temperature coefficient	ΔI_{IO}		-55°C to +125°C	01	1 typical		pA/°C
Dynamic response							
Small signal bandwidth	SSBW	G = 1, -3 dB	+25°C	01	10 typical		MHz
		G = 10, -3 dB			10 typical		
		G = 100, -3 dB			2 typical		
		G = 1000, -3 dB			0.2 typical		
Settling time 0.01%	t_S	G = 1, 10 V step	+25°C	01	0.7 typical		µs
		G = 10, 10 V step			0.4 typical		
		G = 100, 10 V step			0.6 typical		
		G = 1000, 10 V step			5 typical		
Settling time 0.001%	t_S	G = 1, 10 V step	+25°C	01	1 typical		µs
		G = 10, 10 V step			0.6 typical		
		G = 100, 10 V step			0.8 typical		
		G = 1000, 10 V step			6 typical		
Slew rate	SR	G = 1 to 100	+25°C	01	35 typical		V/µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Gain 5/		G = 1 + (9.9 kΩ / R_G)					
Gain range			+25°C	01	1	10,000	V/V
Gain error		G = 1, V_{OUT} = ±10 V	+25°C	01		0.05	%
		G = 10 to 1,000, V_{OUT} = ±10 V				0.3	
Gain nonlinearity		G = 1, R_L ≥ 2 kΩ, V_{OUT} = -10 V to +10 V	+25°C	01		1	ppm
		G = 1, R_L = 600 Ω, V_{OUT} = -10 V to +10 V				3	
					1 typical		
		G = 10 to 1000, R_L ≥ 600 Ω, V_{OUT} = -10 V to +10 V				50	
					30 typical		
		G = 10 to 1000, R_L ≥ 600 Ω, V_{OUT} = -5 V to +5 V				10	
					5 typical		
Gain versus temperature 5/		G = 1	+25°C	01		5	ppm/°C
		G > 1				-80	
Input							
Differential input 6/ impedance			+25°C	01	30||3 typical		GΩ||pF
Common mode 6/ input impedance			+25°C	01	30||3 typical		GΩ||pF
Input operating 7/ voltage range over temperature	V_{IN}	V_S = ±2.5 V to ±18 V	+25°C	01	-V_S + 2.3	+V_S - 1.8	V
			-55°C		-V_S + 2.5	+V_S - 2.0	
			+125°C		-V_S + 2.1	+V_S - 1.8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output							
Output swing	V_{OUT}	V_S = ±2.5 V to ±18 V, R_L = 2 kΩ	+25°C	01	-V_S +1.2	+V_S -1.7	V
			-55°C to +125°C		-V_S +1.4	+V_S -1.9	
Short circuit current	I_{OS}		+25°C	01	65 typical		mA
Reference input							
Input resistance	R_{IN}		+25°C	01	20 typical		kΩ
Input current	I_{IN}	V_{IN+}, V_{IN-} = 0 V	+25°C	01		24	µA
					20 typical		
Voltage range	V_{REF}		+25°C	01	-V_S	+V_S	V
Reference gain to output			+25°C	01	1 ± 0.0001 typical		V/V
Power supply							
Operating range	V_S	Dual supply	+25°C	01	±2.5	±18	V
		Single supply			5	36	
Quiescent current	I_Q		+25°C	01		2.3	mA
					2 typical		
			-55°C to +125°C			2.8	
Temperature range for specified performance	T_A		-55°C to +125°C	01			

See footnotes at end of table.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, $V_S = \pm 15$ V, $V_{REF} = 0$ V, G = 1, and $R_L = 2\ k\Omega$.

3/ Total voltage noise = $\sqrt{\ }\ (e_{ni}^2 + (e_{no} / G)^2 + e_{RG}^2)$. See manufacturer's data sheet for more information.

4/ Total referred to input (RTI) $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$.

5/ These specifications do not include the tolerance of the external gain setting resistor, R_G. For $G > 1$, add R_G errors to the specifications given in this table.

6/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

7/ Input voltage range of the device input stage only. The input range can depend on the common mode voltage, differential voltage, gain, and reference voltage. See the typical performance characteristics section of the manufacturer's datasheet for more information.

Case X

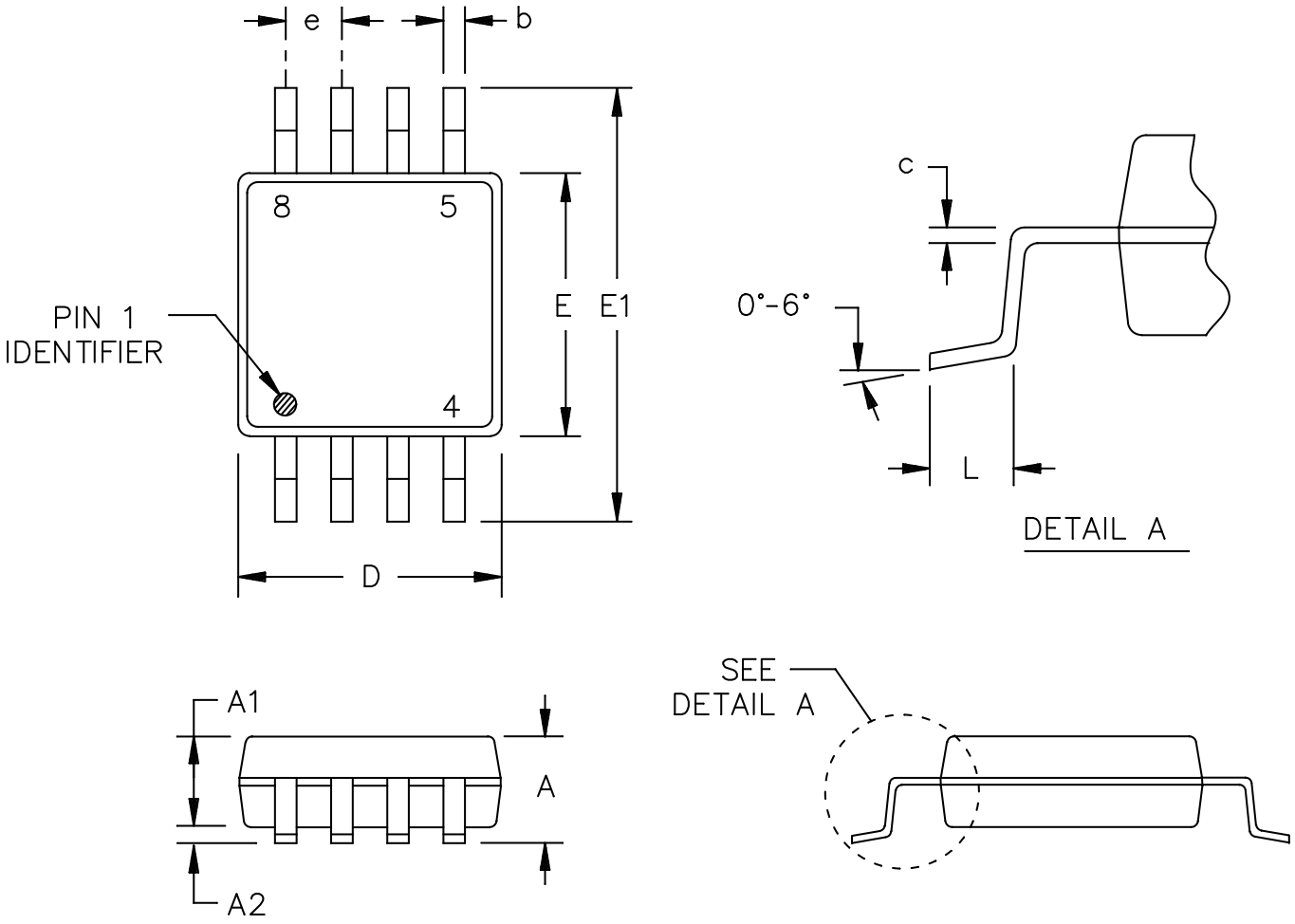

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13625
		REV B	PAGE 11

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	---	---	0.043	---	---	1.10
A1	0.029	0.033	0.037	0.75	0.85	0.95
A2	0.001	---	0.005	0.05	---	0.15
b	0.09	---	0.015	0.25	---	0.40
c	0.003	---	0.009	0.09	---	0.23
D	0.110	0.118	0.129	2.80	3.00	3.20
E	0.110	0.118	0.129	2.80	3.00	3.20
E1	0.183	0.192	0.202	4.65	4.90	5.15
e	0.025 BSC			0.65 BSC		
L	0.015	0.021	0.031	0.40	0.55	0.80

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls with JEDEC MO-187-AA.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	-IN	Negative input terminal.
2	R_G	Gain settling terminal. Place resistor across the R_G pins to set the gain. G = 1 + (9.9 kΩ / R_G).
3	R_G	Gain settling terminal. Place resistor across the R_G pins to set the gain. G = 1 + (9.9 kΩ / R_G).
4	+IN	Positive input terminal.
5	$-V_S$	Negative power supply terminal.
6	REF	Reference voltage terminal. Drive this terminal with a low impedance voltage source to level shift the output.
7	V_{OUT}	Output terminal.
8	$+V_S$	Positive power supply terminal.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Transportation mode and order quantity	Top side marking	Vendor part number
V62/13625-01XE	24355	Tube, 50	Y4T	AD8421TRMZ-EP
	24355	Reel, 1,000	Y4T	AD8421TRMZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123