REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Inactivate device type 01. Add device type 02 with temperature range of -55°C to +125°C. - ro	16-12-14	C. SAFFLE
B	Make correction to the VID control numbers as specified under paragraph 6.3. - ro	17-02-09	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	REV		B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B				
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16				

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 13-10-31	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/13623**
	REV B	**PAGE** 1 **OF** 16

AMSC N/A

5962-V028-17

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quadruple RS-485 differential line driver microcircuit, with an operating temperature range of -40°C to +85°C for device type 01 and -55°C to +125°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13623	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Temperature range	Circuit function
01	SN65LBC173A -EP	-40°C to +85°C	Quadruple RS-485 differential line driver
02	SN65LBC173A -EP	-55°C to +125°C	Quadruple RS-485 differential line driver

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MS-013-AA	Plastic Small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC}) ..... -0.3 V to 6.0 V 2/
Voltage range at any bus (DC) ..... -10 V to 15 V
Voltage range at any bus (transient pulse through 100 Ω) (see figure 8)..... -30 V to 30 V
Input voltage range at G and $\overline{G}$, V_I ..... -0.5 V to V_{CC} + 0.5 V
Receive output current, (I_O) ..... ±10 mA
Electronic discharge:
  Human body model: 3/
    A and B to GND ..... 6 kV
    All pins ..... 5 kV
  Charged device model: 4/
    All pins ..... 2 kV
Storage temperature range ..... -65°C to 150°C

1.4 Thermal characteristics.

Thermal metric 5/	Symbol	Case outline X	Units
Junction to ambient thermal resistance 6/	θ_{JA}	78	°C/W
Junction to case (top) thermal resistance 7/	θ_{JCtop}	39.5	°C/W
Junction to board thermal resistance 8/	θ_{JB}	35.4	°C/W
Junction to top characterization parameter 9/	Ψ_{JT}	8.5	°C/W
Junction to board characterization parameter 10/	Ψ_{JB}	35.1	°C/W

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltages, are with respect to GND.
3/ Tested in accordance with JEDEC standard 22, Test Method A 114-A.
4/ Tested in accordance with JEDEC standard 22, Test Method C101.
5/ For more information about traditional and new thermal metrics, see manufacturer data.
6/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.
7/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
8/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
9/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
10/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

1.5 Recommended operating conditions. 11/

Supply voltage, (V_{CC})	4.75 V to 5.25 V
Voltage at any bus terminal, (A, B)	-7 V to 12 V
High level input voltage, V_{IH} (G, $\overline{G}$)	2 V to V_{CC}
Low level input voltage, V_{IL} (G, $\overline{G}$)	0 V to 0.8 V
Output current, (Y)	-8 mA to 8 mA
Operating free air temperature, (T_A) :	
Device type 01	-40°C to +85°C
Junction temperature, (T_J) :	
Device type 02	-55°C to +125°C

2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE

ANSI SEMI STANDARD G30-88 - Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Applications for copies should be addressed to the American National Standards Institute, Semiconductor Equipment and Materials International, 1819 L Street, NW, 6 th floor, Washington, DC 20036 or online at http://www.ansi.org)

JEDEC Solid State Technology Association

EIA/JESD51-2a	-	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
EIA/JEDEC 51-7	-	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
EIA/JESD51-8	-	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD22-C101	-	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JESD22-A114	-	Electrostatic Discharge Sensitivity Testing Human Body Model (HBM)

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

11/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Voltage and current definitions. The voltage and current definitions shall be as shown in figure 4.

3.5.5 Switching test circuit and waveforms. The switching test circuit and waveforms shall be as shown in figure 5.

3.5.6 Test circuit waveforms, t_{PZH} and t_{PHZ}. The test circuit waveforms, t_{PZH} and t_{PHZ} shall be as shown in figure 6.

3.5.7 Test circuit waveforms, t_{PZL} and t_{PLZ}. The test circuit waveforms, t_{PZL} and t_{PLZ} shall be as shown in figure 7.

3.5.8 Test circuit waveforms, Transient over voltage test. The test circuit waveforms, Transient over voltage test shall be as shown in figure 8.

3.5.9 Equivalent input and output schematic diagrams. The equivalent input and output schematic diagrams shall be as shown in figure 9.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Electrical characteristics.							
Positive going differential input voltage threshold	V_{IT+}	-7 V ≤ V_{CM} ≤ 12 V, (V_{CM} = (V_A + V_B)/2)	-40°C to +85°C	01		-10	mV
					-80 typical		
			-55°C to +125°C	02		-10	
					-80 typical		
Negative going differential input voltage threshold	V_{IT-}	-7 V ≤ V_{CM} ≤ 12 V, (V_{CM} = (V_A + V_B)/2)	-40°C to +85°C	01	-200		mV
					-120 typical		
			-55°C to +125°C	02	-200		
					-120 typical		
Hysteresis voltage (V_{IT+} - V_{IT-})	V_{HYS}		-40°C to +85°C	01	40 typical		mV
			-55°C to +125°C	02	40 typical		
Input clamp voltage	V_{IK}	I_I = - 18 mA	-40°C to +85°C	01	-1.5		V
					-0.8 typical		
			-55°C to +125°C	02	-1.5		
					-0.8 typical		
High level output voltage	V_{OH}	V_{ID} = 200 mV, I_{OH} = -8 mA, see figure 4	-40°C to +85°C	01	2.7		V
					4.8 typical		
			-55°C to +125°C	02	2.7		
					4.8 typical		
Low level output voltage	V_{OL}	V_{ID} = 200 mV, I_{OL} = 8 mA, see figure 4	-40°C to +85°C	01		0.4	V
					0.2 typical		
			-55°C to +125°C	02		0.4	
					0.2 typical		
High impedance state output current	I_{OZ}	V_O = 0 V to V_{CC}	-40°C to +85°C	01	-1	1	μA
			-55°C to +125°C	02	-1	1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions		Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Electrical characteristics - continued.								
Line input current	I_I	Other input at 0 V, V_{CC} = 0 V or 5 V	V_I = 12 V	-40°C to +85°C	01		0.9	mA
			V_I = -7 V			-0.7		
		Other input at 0 V, V_{CC} = 0 V or 5 V	V_I = 12 V	-55°C to +125°C	02		0.9	
			V_I = -7 V			-0.7		
High level input current	I_{IH}	Enable input G, $\overline{G}$		-40°C to +85°C	01		100	mA
				-55°C to +125°C	02		110	
Low level input current	I_{IL}	Enable input G, $\overline{G}$		-40°C to +85°C	01	-100		mA
				-55°C to +125°C	02	-100		
Input resistance	R_I	A, B inputs		-40°C to +85°C	01	12		kΩ
				-55°C to +125°C	02	12		
Supply current	I_{CC}	V_{ID} = 5 V, G at 0 V, $\overline{G}$ at V_{CC}		-40°C to +85°C	01		32	μA
				-55°C to +125°C	02		32	
		No load, G at 0 V, $\overline{G}$ at 0 V		-40°C to +85°C	01		16	
						11 typical		
				-55°C to +125°C	02		16	
						11 typical		
Switching characteristics.								
Differential output voltage rise time	t_r	V_{ID} = -3 V to 3 V, see figure 5		-40°C to +85°C	01		6	ns
						2 typical		
				-55°C to +125°C	02		7	
						2 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching characteristics – continued.							
Differential output voltage fall time	t_f	V_{ID} = -3 V to 3 V, see figure 5	-40°C to +85°C	01		6	ns
					2 typical		
			-55°C to +125°C	02		7	
					2 typical		
Propagation delay time, low to high level output	t_{PLH}	V_{ID} = -3 V to 3 V, see figure 5	-40°C to +85°C	01	9	16	ns
					12 typical		
			-55°C to +125°C	02	8	18	
					12 typical		
Propagation delay time, high to low level output	t_{PHL}	V_{ID} = -3 V to 3 V, see figure 5	-40°C to +85°C	01	9	16	ns
					12 typical		
			-55°C to +125°C	02	8	18	
					12 typical		
Propagation delay time, high impedance to high level output	t_{PZH}	See figure 6	-40°C to +85°C	01		38	ns
					27 typical		
			-55°C to +125°C	02		39	
					27 typical		
Propagation delay time, high level output to high impedance	t_{PHZ}	See figure 6	-40°C to +85°C	01		22	ns
					7 typical		
			-55°C to +125°C	02		24	
					7 typical		
Propagation delay time, high impedance to low level output	t_{PZL}	See figure 7	-40°C to +85°C	01		38	ns
					29 typical		
			-55°C to +125°C	02		39	
					29 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching characteristics – continued.							
Propagation delay time, low level output to high impedance	t_{PLZ}	See figure 7	-40°C to +85°C	01		16	ns
					12 typical		
			-55°C to +125°C	02		18	
					12 typical		
Pulse skew ($\lvert t_{PLH} - t_{PHL} \rvert$)	$t_{sk(p)}$		-40°C to +85°C	01		1	ns
					0.2 typical		
			-55°C to +125°C	02		2	
					0.2 typical		
Output skew 4/	$t_{sk(o)}$		-40°C to +85°C	01		2	ns
			-55°C to +125°C	02		3	
Part-to-part skew 5/	$t_{sk(pp)}$		-40°C to +85°C	01		2	ns
			-55°C to +125°C	02		3	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

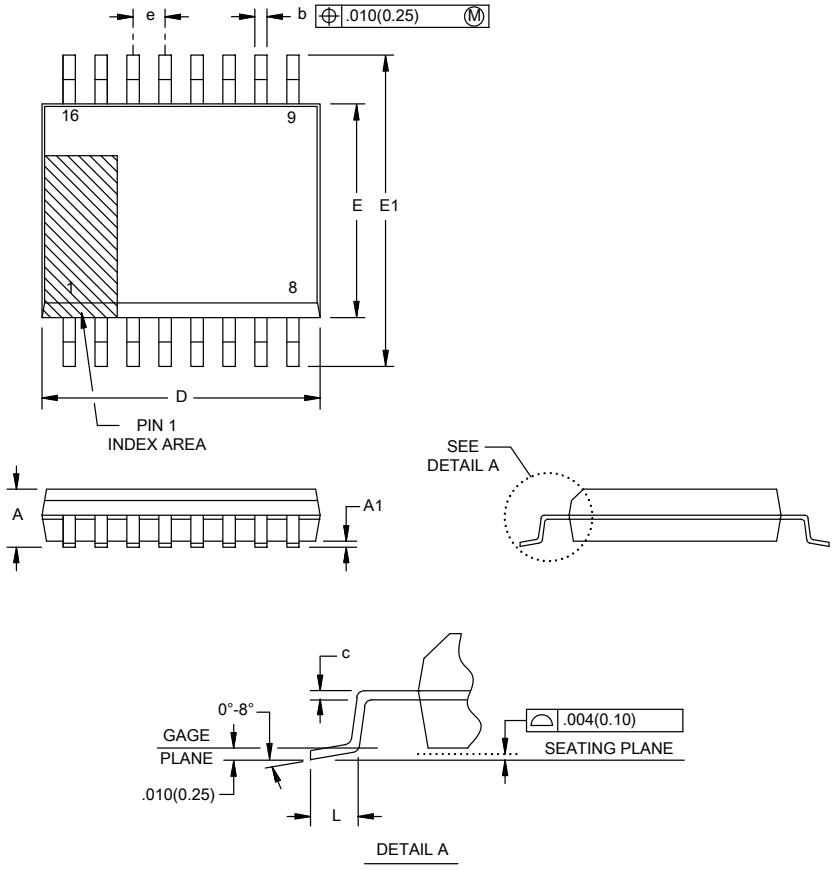
2/ Over recommended operating conditions.

3/ All typical values are at V_{CC} = 5 V and 25°C.

4/ Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

5/ Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.104		2.65	E	.291	.299	7.40	7.60
A1	.004	.012	0.10	0.30	E1	.393	.419	9.97	10.63
b	.012	.020	0.31	0.51	e	.050 BSC		1.27 BSC	
c	.008	.013	0.20	0.33	L	.016	.050	0.40	1.27
D	.398	.413	10.10	10.50					

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed .006 inches (0.15 mm).
3. Falls within JEDEC MS-013 variation AA.

FIGURE 1. Case outline.

Device types	01 and 02		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	1B	I	RS485 differential input (inverting).
2	1A	I	RS485 differential input (noninverting).
3	1Y	O	Logic level output.
4	G	I	Active high select.
5	2Y	O	Logic level output.
6	2A	I	RS485 differential input (noninverting).
7	2B	I	RS485 differential input (inverting).
8	GND	---	Ground.
9	3B	I	RS485 differential input (inverting).
10	3A	I	RS485 differential input (noninverting).
11	3Y	O	Logic level output.
12	$\overline{G}$	I	Active low select.
13	4Y	O	Logic level output.
14	4A	I	RS485 differential input (noninverting).
15	4B	I	RS485 differential input (inverting).
16	V_{CC}	---	Power supply.

FIGURE 2. Terminal connections.

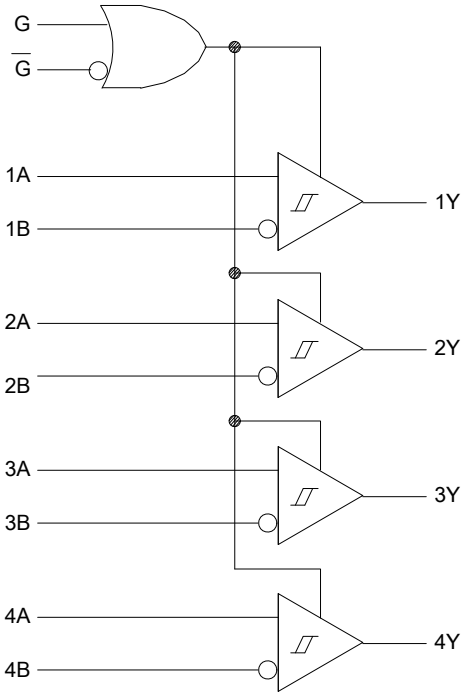


FIGURE 3. Logic diagram.

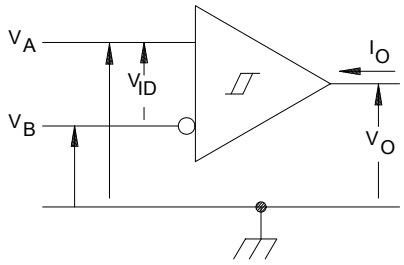
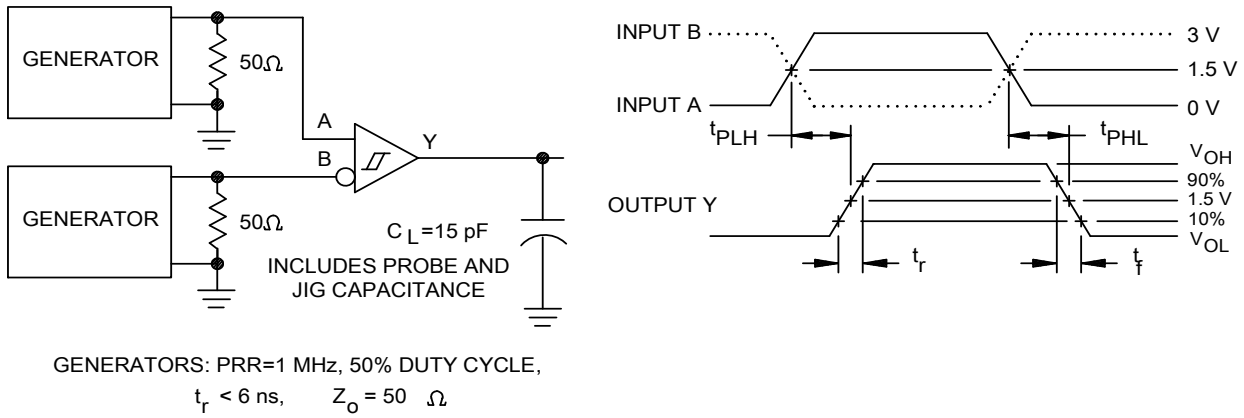
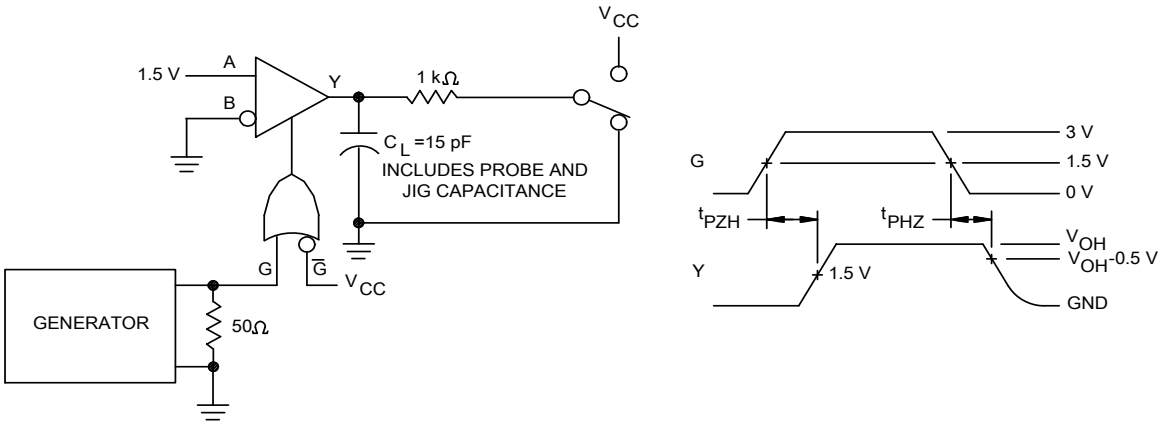


FIGURE 4. Voltage and current definitions.



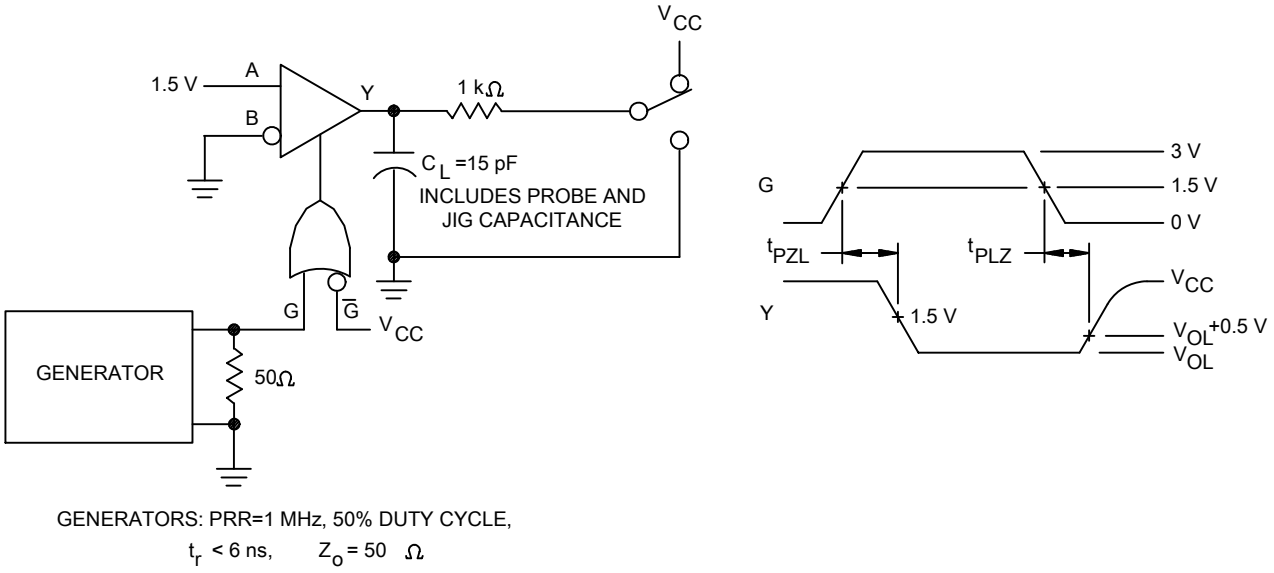
GENERATORS: PRR=1 MHz, 50% DUTY CYCLE,
t_r < 6 ns, Z_o = 50 Ω

FIGURE 5. Switching test circuit and waveforms.



GENERATORS: PRR=1 MHz, 50% DUTY CYCLE,
t_r < 6 ns, Z_o = 50 Ω

FIGURE 6. Test circuit waveforms, t_{PZH} and t_{PHZ}.



GENERATORS: PRR=1 MHz, 50% DUTY CYCLE,
t_r < 6 ns, Z_o = 50 Ω

FIGURE 7. Test circuit waveforms, t_{PZL} and t_{PLZ}.

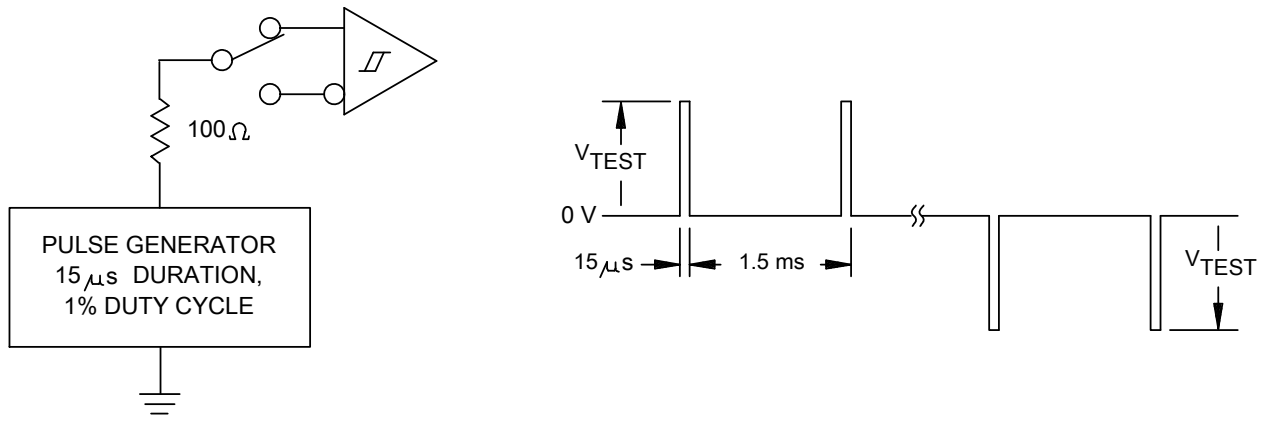


FIGURE 8. Test circuit and waveform, transient over-voltage test.

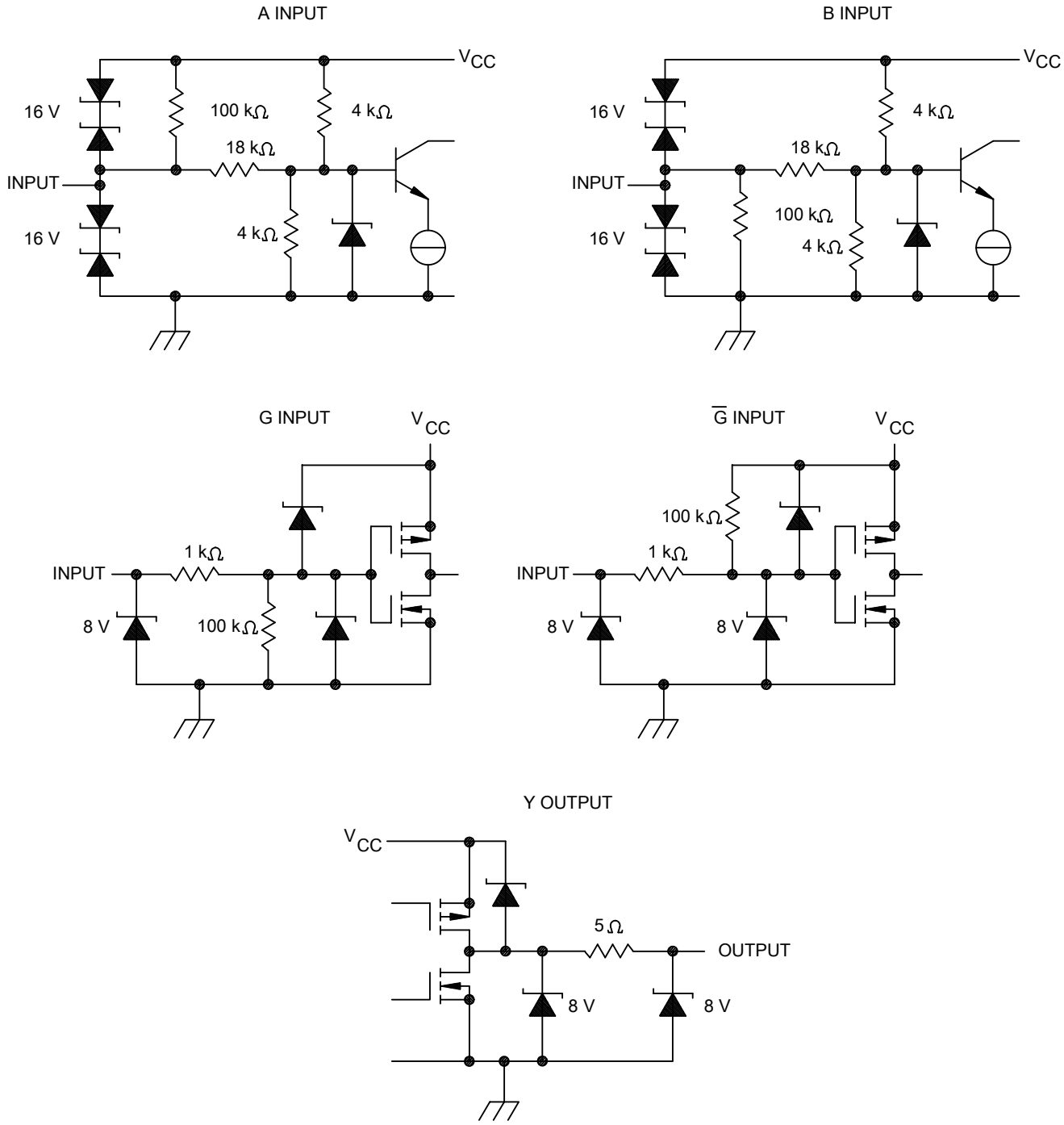


FIGURE 9. Equivalent input and output schematic diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13623
		REV B	PAGE 15

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Temperature range	Top side marking	Vendor part number
V62/13623-01XE	3/	-40°C to +85°C	LBC173EP	SN65LBC173ADREP
V62/13623-02XE	01295	-55°C to +125°C	LBC173AEP	SN65LBC173AMDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.
3/ No longer available from an approved source of supply.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243