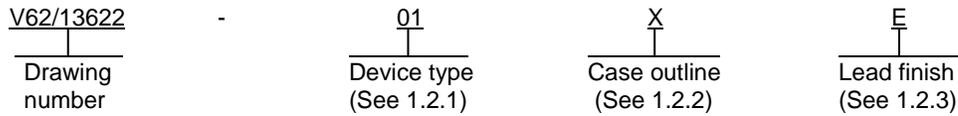


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance digital PWM system controller with 4-bit, 6-bit, or 8-bit VID support microcircuit, with an operating temperature range of -55°C to +115°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	UCD9222 -EP	Digital PWM system controller with 4-bit, 6-bit, or 8-bit VID support

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	48	JEDEC MO-220	Plastic quad flatpack no-lead

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 2

1.3 Absolute maximum ratings. 1/

Voltage applied at V _{33D} to DGND	-0.3 V to 3.8 V
Voltage applied at V _{33D} to AGND	-0.3 V to 3.8 V
Voltage applied at to any pin	-0.3 V to 3.8 V 2/
Storage temperature range	-55°C to 150°C

1.4 Recommended operating conditions.

Supply voltage during operation, V _{33D} , V _{33DIO} , V _{33A} (V)	3.0 V to 3.6 V
Operating junction temperature range	-55°C to 115°C
Maximum junction temperature	125°C

1.5 Thermal characteristics.

Thermal metric 3/	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} 4/	27.1	°C/W
Junction to case (top) thermal resistance, θ_{JcTop} 5/	12.9	
Junction to board thermal resistance, θ_{JB} 6/	4.3	
Junction to top characterization parameter, Ψ_{JT} 7/	0.2	
Junction to board characterization parameter, Ψ_{JB} 8/	4.3	
Junction to case (bottom) thermal resistance, θ_{Jcbot} 9/	0.6	

-
- 1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
 - 2/ All voltage referenced to GND.
 - 3/ For more information about traditional and new thermal metrics, see manufacturer data.
 - 4/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.
 - 5/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
 - 6/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
 - 7/ The junction to top characterization parameter, Ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
 - 8/ The junction to board characterization parameter, Ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
 - 9/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 3

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).
- JESD51-2a – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-8 – Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

- ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Applications for copies should be addressed to the American National Standards Institute, Semiconductor Equipment and Materials International, 1819 L Street, NW, 6 th floor, Washington, DC 20036 or online at <http://www.ansi.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal function. The terminal function shall be as shown in figure 2.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Supply current						
Supply current	I_{V33}	Total V33 supply current, $V_{33A} = V_{33DIO} = 3.3\text{ V}$		54	80	mA
	I_{V33DIO}	$V_{33DIO} = 3.3\text{ V}$		42	55	
	I_{V33A}	$V_{33A} = 3.3\text{ V}$		8	15	
	I_{V33D}	$V_{33D} = 3.3\text{ V}$ storing configuration parameters in flash memory		52	65	
Internal regulator controller Inputs/Outputs						
3.3 V linear regulator	V_{33}	Emitter of NPN transistor	3.25	3.3	3.6	V
3.3 V linear regulator feedback	V_{33FB}			4	4.6	
Series pass base driver	I_{V33FB}	$V_{IN} = 12\text{ V}$	0.2	0.4	8	mA
Series NPN pass device	Beta		40	100		
External supplied 3.3 V power						
Digital 3.3 V power	$V_{33D}, V_{33DIO1},$ V_{33DIO2}	$T_J = 25^\circ\text{C}$	3.0		3.6	V
Analog 3.3 V power	V_{33A}	$T_J = 25^\circ\text{C}$	3.0		3.6	
Error amplifier inputs EAPn, EANn						
Common mode voltage each pin	V_{CM}		0		1.8	V
Internal error voltage range	V_{ERROR}	AFE_GAIN field of CLA_GAINS = 1X 3/	-256		248	mV
Error voltage digital resolution	EAP-EAN	AFE_GAIN field of CLA_GAINS = 8X		1		mV
Input impedance	R_{EA}	Ground reference, $T_J = 25^\circ\text{C}$		1.5		MΩ
Input offset current	I_{OFFSET}	1 kΩ source impedance	-5		5	μA
Vref 10 bit DAC						
Reference voltage setpoint	V_{ref}		0		1.7	V
Reference voltage resolution	V_{refres}			1.56		mV
Analog input CS1A, CS2A, VinMon, linMon, Vtrack, Temp1, Temp2, Addr0, Addr1						
Measurement range for voltage monitoring	V_{ADC_RANGE}	Inputs: VinMon, linMon, Vtrack, Temp1, Temp2, CS1A, CS2A	0		2.6	V
Input offset voltage	V_{offset}		-27		27	mV
Over current comparator threshold voltage range 4/	V_{OC_THRS}	Inputs: CS1A, CS2A	0.032		2	V
Over current comparator threshold voltage range	V_{OC_RES}	Inputs: CS1A, CS2A		31.25		mV
Int. temperature sense accuracy	$Temp_{internal}$	Over range from 0°C to 100°C	-15		15	°C
ADC integral nonlinearity	INL	$T_J = -40^\circ\text{C}$ to 115°C	-2.5		2.5	mV
Input leakage current	I_{lkg}	3V applied to pin			100	nA
Input impedance	R_{IN}	Ground reference		8		MΩ
Current sense input capacitance	C_{IN}			10		pF

See footnote at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 5

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits		Unit
			Min	Max	
Digital Inputs/Outputs					
Low level output voltage	V _{OL}	I _{OL} = 6 mA <u>5/</u> , V _{33DIO} = 3 V		Dgnd + 0.3	V
High level output voltage	V _{OH}	I _{OH} = -6 mA <u>6/</u> , V _{33DIO} = 3 V	V _{33DIO} -0.6V		
High level input voltage	V _{IH}	V _{33DIO} = 3V	2.1	3.6	
Low level input voltage	V _{IL}	V _{33DIO} = 3.5 V		1.4	
System performance					
Voltage where device comes out of reset	V _{RESET}	V _{33D} Pin	2.3	2.4	V
Pulse width need for reset	t _{RESET}	nRESET pin	2		µs
Setpoint reference accuracy	V _{RefAcc}	Vref commanded to be 1V, at 25°C AFEgain = 4, 1V input to EAP/N measured at output of the EADC <u>7/</u>	-10	10	mV
Setpoint reference accuracy over temperature		-55°C to 115°C	-40	40	mV
Differential offset between gain settings	V _{DiffOffset}	AFEgain = 4 compared to AFEgain = 1, 2, or 8	-4	4	mV
Digital compensator delay	t _{Delay}		240	240 + 1 switching cycle	ns
Switching frequency	F _{SW}		15.260	2000	kHz
Accuracy			-5%	5%	
Max and Min duty cycle	Duty		0%	100%	
Minimum V33 slew rate	V _{33Slew}	V33 slew rate between 2.3 V and 2.9 V, T _J = -40°C to 115°C	0.25		V/ms
Retention of configuration parameters <u>8/</u>	t _{retention}	T _J = 25°C	100		Years
Number of nonvolatile erase/write cycles	Write_Cycles	T _J = 25°C	20		K cycles
Max VID message rate	Rate _{VID}	All rails configured to accept 4-bit VID messages <u>9/</u>		1	msg/msec
		All rails configured to accept 6-bit VID messages <u>9/</u>		4	
		All rails configured to accept 8-bit VID messages <u>10/</u>		4	

See footnote at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 6

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
ADC monitoring intervals and response times						
ADC single sample time	t _{ADC}			3.84		μs
ADC sequencer interval	t _{ADC_SEQ}	Min = 2 x 1 Rail + 6 = 8 samples Max = 2 x 2 Rail + 6 = 10 samples	30.72		38.40	
Output voltage monitoring interval	t _{VOUT}			200		
Output current monitoring interval	t _{IOUT}			200 x N _{Rails}		
Input voltage monitoring interval	t _{VIN}			1		ms
Input current monitoring interval	t _{IIN}			1		
Temperature monitoring interval	t _{TEMP}			100		
Auxiliary ADC monitoring interval	t _{AUXADC}			100		

Test	Symbol	Test conditions	Limits			Unit
			Typ	MAX no VID	Max /w VID <u>11/</u>	
ADC monitoring intervals and response times - Continued						
Over/under voltage fault response time during normal operation	t _{OVF} , t _{UVF}	Normal regulation, no PMBus activity 4 stages enabled		250	800	μs
Over/under voltage fault response time during data logging	t _{OVF} , t _{UVF}	During data logging to nonvolatile memory <u>12/</u>		800	1000	
Over/under voltage fault response time, when tracking or sequencing enable	t _{OVF} , t _{UVF}	During tracking and soft start ramp		400		
Over/under current fault response time during normal operation	t _{OCF} , t _{UCF}	Normal regulation, no PMBus activity, 4 stages enabled 75% to 125% current step <u>13/</u>		100 + (600 x NRails)	5000	
Over/under current fault response time during data logging	t _{OCF} , t _{UCF}	During data logging to nonvolatile memory 75% to 125% current step		600 + (600 x NRails)	5000	
Over temperature fault response time	t _{OTF}	Temperature rise of 10°C, at OT threshold	1.60			sec
Time to tristate the PWM output after a shutdown is initiated	t _{3-State}	DRIVER_CONFIG = 0x01	5.5			μs

See footnote at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 7

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Hardware fault detection latency						
Time to disable DPWM output base on active FAULT pin signal	t _{FAULT}	High level on FAULT pin			18	μs
Time to disable DPWM A output base on internal analog comparator	t _{CLF}	Step change in CS voltage from 0 V to 2.5 V			4	Switch Cycles
I²C/SMBus/PMBus timing requirements <u>14/</u>						
SMBus/PMBus operating frequency	f _{SMB}	Slave mode; SMBC 50% duty cycle	10		1000	kHz
I ² C operating frequency	f _{I2C}	Slave mode; SCL 50% duty cycle	10		1000	
Bus free time between start and stop	t _(BUF)		5			μs
Hold time after (repeated) start	t _(HD:STA)		0.3			
Repeated start setup time	t _(SU:STA)		0.3			
Stop setup time	t _(SU:STO)		0.3			
Data hold time	t _(HD:DAT)	Receive mode	0			ns
Data setup time	t _(SU:DAT)		55			
Error signal/detect	t _(TIMEOUT)	See <u>15/</u>			35	ms
Clock low period	t _(LOW)		0.55			μs
Clock high period	t _(HIGH)	See <u>16/</u>	0.3		50	
Cumulative clock low slave extend time	t _(LOW:SEXT)	See <u>17/</u>			25	ms
Clock/data fall time	t _{FALL}	Rise time t _{RISE} = (V _{ILMAX} - 0.15) to (V _{IHMIN} + 0.15), T _J = -40°C to 115°C			1000	ns
Clock/data rise time	t _{RISE}	Fall time t _{FALL} = 0.9 V ₃₃ to (V _{ILMAX} - 0.15) T _J = -40°C to 115°C			1000	
	C _{IN}					

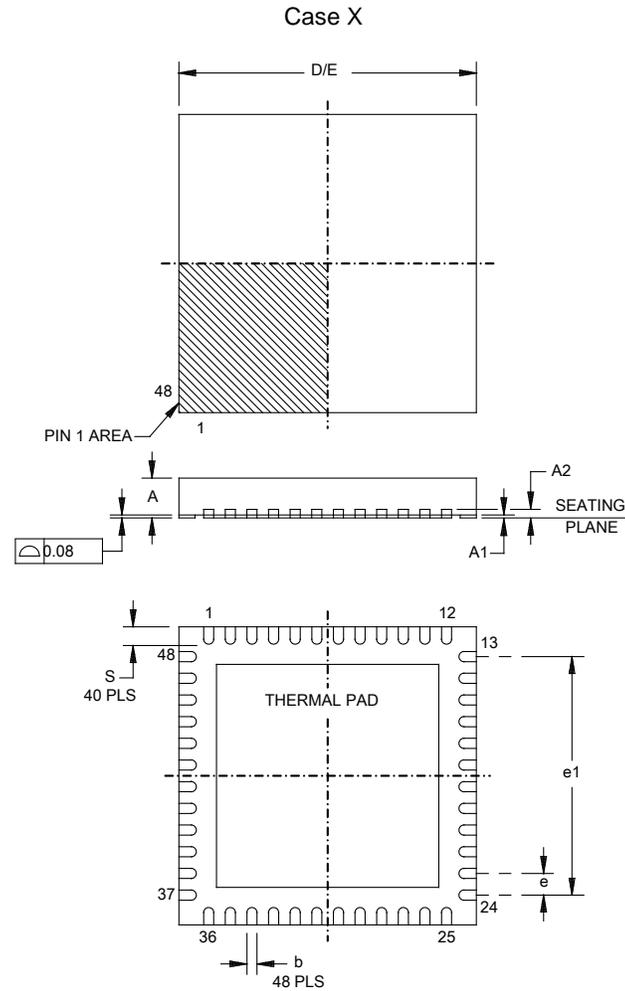
See footnote at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 8

TABLE I. Electrical performance characteristics - Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over operating junction temperature range (unless otherwise noted).
- 3/ See the UCD92xx PMBus Command Reference from manufacturer Data sheet for the description of the AFE_GAIN field of CLA_GAINS command.
- 4/ Can be disabled by setting to '0'.
- 5/ The maximum I_{OL} , for all outputs combined should not exceed 12 mA to hold the maximum voltage drop specified.
- 6/ The maximum I_{OH} , for all outputs combined should not exceed 48 mA to hold the maximum voltage drop specified.
- 7/ With default device calibration. PMBus calibration can be used to improve the regulation tolerance.
- 8/ The data retention specification is based on accelerated stress testing at 170°C for 420 hours and using an Arrhenius model with activation energy of 0.6 eV.
- 9/ VID message rate on each interface. Measured over a 1.0 msec interval.
- 10/ VID message rate on PMBus interface.
- 11/ Controller receiving VID commands at a rate of 4000 msg/sec.
- 12/ During a STORE_DEFAULT_ALL command, which stores the entire configuration to nonvolatile memory, the fault detection latency can be up to 10 ms.
- 13/ Because the current measurement is averaged with a smoothing filter, the response time to an over-current condition depends on a combination of the time constant (T) from table 3., the recent measurement history, and how much the measured value exceeds the over current limit.
- 14/ $T_J = -55^\circ\text{C}$ to 115°C , $3\text{ V} < V_{33} < 3.6\text{ V}$, typical values at $T_J = 25^\circ\text{C}$.
- 15/ The device times out when any clock low exceeds t_{TIMEOUT} .
- 16/ t_{HIGH} , max, is the minimum bus idle time. SMBC = SMBD = 1 for $t > 50\text{ ms}$ causes reset of any transaction involving this device in progress.
- 17/ $t_{\text{(LOW:SEXT)}}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 9



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	D/E	6.85	7.15
A1	0.00	0.05	e	0.50 BSC	
A2	0.20 REF		e1	5.50 BSC	
b	0.18	0.30	S	0.30	0.50

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Quad Flatpack, No-leads (QFN) package configuration.
4. The package thermal pad must be soldered to the board for thermal and mechanical performance.
5. See the additional figure in the manufacturer data sheet for details regarding the exposed thermal pad features and dimensions.
6. Falls within JEDEC MO-220.

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 10

Terminal No.	Terminal name	Description
1	linMon/AuxADC4	Input current monitor, or Auxiliary ADC input 4
2	Temp2/AuxADC2	Temperature sense input for Rail 2, or Auxiliary ADC input 2
3	CS2A	Power stage 2A current sense input and input to analog comparator 2
4	VinMon	Input voltage monitor
5	nRESET	Active low device reset input. Pull up to 3.3V with a 10kΩ resistor
6	FLT1A	Fault indicator for stage 1A
7	VID1S	VID Select pin for Rail 1
8	FLT2A	Fault indicator for stage 2A
9	VID2S	VID Select pin for Rail 2
10	PMBus_Clk	PMBus Clock. Pull up to 3.3V with a 2kΩ resistor
11	PMBus_Data	PMBus Data. Pull up to 3.3V with a 2kΩ resistor
12	DPWM1A	Digital Pulse Width Modulator output 1A
13	PG1	Rail 1 Power Good Indicator
14	DPWM2A	Digital Pulse Width Modulator output 2A
15	PG2	Rail 2 Power Good Indicator
16	VID1A	VID input pin for Rail 1 – least significant bit
17	PowerGood	Power Good Indication
18	VID1B	VID input pin for Rail 1
19	PMBus_Alert	PMBus Alert. Pull up to 3.3V with a 10kΩ resistor
20	PMBus_Cntrl	PMBus Control. Pull up to 3.3V with a 10kΩ resistor
21	VID1C	VID input pin for Rail 1 – most significant bit
22	VID2A	VID input pin for Rail 2 – least significant bit
23	VID2B	VID input pin for Rail 2
24	VID2C	VID input pin for Rail 2 – most significant bit
25	EN1	Rail 1 Enable
26	EN2	Rail 2 Enable
27	JTAG_TCK	JTAG Test Clock
28	SyncOut/JTAG_TDO	Mux'ed pin JTAG Test Data Output, DPWM Sync Output
29	SyncIn/JTAG_TDI	Mux'ed pin – JTAG Test Data In, DPWM Sync Input
30	JTAG_TMS	JTAG Test mode select. Pull up to 3.3V with a 10kΩ resistor
31	JTAG) nTRST	JTAG Test Reset – Tie to ground with a 10kΩ resistor
32	Dgnd3	Digital Ground
33	V33DIO	3.3V supply for Digital I/O and Core
34	V33A	Analog 3.3V supply
35	BPCap	1.8V Bypass Capacitor – tie 0.1 μF cap to analog ground
36	Agnd2	Analog ground
37	EAp1	Error analog, differential voltage, Positive channel 1 input
38	EAn1	Error analog, differential voltage, Negative channel 1 input
39	EAp2	Error analog, differential voltage, Positive channel 2 input
40	EAn2	Error analog, differential voltage, Negative channel 2 input

FIGURE 2. Terminal function.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 11

Terminal No.	Terminal name	Description
41	V33FB	Connection to the base of 3.3V linear regulator transistor (no connect if unused)
42	CS1A	Power stage 1A current sense input and input to analog comparator 1
43	Addr1	PMBus Address sense. Channel 1.
44	Addr0	PMBus Address sense. Channel 0.
45	Vtrack/AuxADC3	Tracking voltage input, or Auxiliary ADC input 3
46	Temp1/AuxADC1	Temperature sense input for Rail 1, or Auxiliary ADC input 1
47	Agnd3	Analog ground
48	ADC_Ref	ADC Reference. Tie to analog ground through 0.1µF capacitor
PowerPad		It is recommended that this pad be connected to analog ground

FIGURE 2. Terminal function - Continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 12

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/13622-01XE	24355	UCD9222WRGZREP	UCD9222

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13622
		REV	PAGE 13