

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	19-04-29	Thomas M. Hess
B	Add thermal resistance characteristics information to paragraph 1.3. Add ANSI and JEDEC references to paragraph 2. Add conditions to ICC, Ioff, VOL, and VOH parameters under Table I. Update document paragraphs to current requirements. - ro	24-12-04	James R. Eschmeyer



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

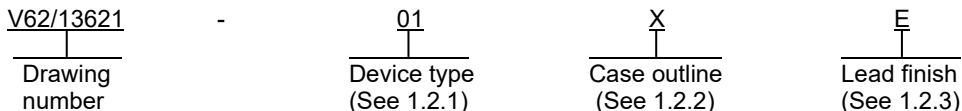
REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17			

PMIC N/A Original date of drawing YY-MM-DD 14-02-18	PREPARED BY Phu H. Nguyen		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime	
	CHECKED BY Phu H. Nguyen		TITLE MICROCIRCUIT, LINEAR, RS-232	
	APPROVED BY Thomas M. Hess		TRANSCEIVER WITH SPLIT SUPPLY PIN FOR LOGIC SIDE, MONOLITHIC SILICON	
	SIZE A	CAGE CODE 16236	DWG NO. V62/13621	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance RS-232 transceiver with split supply pin for logic side microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type.

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TRS3253E-EP	RS-232 transceiver with split supply pin for logic side

1.2.2 Case outline. The case outline are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>Package style</u>
X	32	Plastic quad flatpack no-lead

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

VCC to GND.....	-0.3 V to 6.0 V
VL to GND	-0.3 V to VCC + 0.3 V
V+ to GND	-0.3 V to 7.0 V
V- to GND	0.3 V to -7.0 V
Maximum V+ + V- 	13.0 V <u>2/</u>
Input voltage, (Vi):	
DIN, FORCEOFF to GND, FORCEON to GND	-0.3 V to 6.0 V
Maximum RIN to GND	±25.0 V
Output voltage, (Vo):	
Maximum DOUT to GND	±13.2 V
ROUT	-0.3 V to VL + 0.3 V
Junction temperature, (Tj)	150°C
Storage temperature, (Tstg)	-65°C to 150°C
Typical ESD protection, (RIN, DOUT):	
Thermal resistance, junction to ambient (θJA)	37.2°C/W <u>3/</u>
Thermal resistance, junction to case top (θJC(top))	30.1°C/W <u>4/</u>
Thermal resistance, junction to board (θJB)	7.8°C/W <u>5/</u>
Characterization parameter, junction to top (ψJT)	0.4°C/W <u>6/</u>
Characterization parameter, junction to board (ψJB)	7.6°C/W <u>7/</u>
Thermal resistance, junction to case (bottom) (θJC(bot))	2.4°C/W <u>8/</u>
Electrostatic discharge (ESD) receiver inputs (RIN), driver inputs (DOUT):	
Human body model (HBM)	±15 kV
IEC 61000-4-2 Air Gap discharge	±8 kV
IEC 61000-4-2 Contact discharge	±8 kV

-
- 1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
 - 2/ V+ and V- can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.
 - 3/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.
 - 4/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
 - 5/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
 - 6/ The junction to top characterization parameter, ψJT, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θJA, using a procedure described in JESD51-2a (sections 6 and 7).
 - 7/ The junction to board characterization parameter, ψJB, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θJA, using a procedure described in JESD51-2a (sections 6 and 7).
 - 8/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

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1.4 Recommended operating conditions.

Supply voltage, (VCC)	3.0 V to 5.5 V
Supply voltage, (VL)	1.65 V to VCC
Maximum input logic threshold low, (DIN, $\overline{\text{FORCEOFF}}$, FORCEON):	
VL = 3.0 V or 5.5 V	0.8 V
VL = 2.3 V	0.6 V
VL = 1.65 V	0.5 V
Minimum input logic threshold high, (DIN, $\overline{\text{FORCEOFF}}$, FORCEON):	
VL = 5.5 V	2.4 V
VL = 3.0 V	2.0 V
VL = 2.3 V	1.4 V
VL = 1.95 V	1.25 V
Operating temperature	-55°C to 125°C
Receiver input voltage	-25 V to 25 V

2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE, SEMICONDUCTOR EQUIPMENT and MATERIALS INTERNATIONAL

ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available online at <https://www.ansi.org>.)

International Electrotechnical Commission

IEC 61000-4-2 – Electromagnetic Compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test

(Copies of these documents are available online at <https://www.iec.org>.)

JEDEC Solid State Technology Association

EIA/JESD51-2a – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
 EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
 EIA/JESD 51-8 – Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board

(Copies of these documents are available online at <https://www.jedec.org>.)

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 Receiver propagation delay times. The receiver propagation delay times shall be as shown in figure 6.

3.5.7 Receiver enable and disable times. The receiver enable and disable times shall be as shown in figure 7.

3.5.8 Driver slew rate. The driver slew rate shall be as shown in figure 8.

3.5.9 Driver pulse skew. The driver pulse skew shall be as shown in figure 9.

3.5.10 INVALID propagation delay times and supply enabling time. The INVALID propagation delay times and supply enabling time shall be as shown in figure 10

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ 3/	Max	
Electrical characteristics 4/						
Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON	I _I		±0.01	±2.9	µA
Supply current (T _A = 25°C)	Auto powerdown plus disabled	I _{CC}	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at VCC	0.5	1.11	mA
	Power off		No load, $\overline{\text{FORCEOFF}}$ at GND	1	10	µA
	Auto powerdown plus enabled		No load, $\overline{\text{FORCEOFF}}$ at VCC, FORCEON at GND, all RIN are open or grounded	1	10	

RECEIVER SECTION 5/ 6/

Electrical characteristics							
Output leakage current	I _{off}	R _{OUT} , receivers disabled			±0.05	±25	µA
Output voltage low	V _{OL}	I _{OUT} = 1.6 mA				0.4	V
Output voltage high	V _{OH}	I _{OUT} = -1 mA		V _L - 0.6	V _L - 0.1		V
Input threshold low	V _{IT-}	T _A = 25°C	V _L = 5 V	0.8	1.2		V
			V _L = 3.3 V	0.6	1.5		V
Input threshold high	V _{IT+}	T _A = 25°C	V _L = 5 V		1.8	2.4	V
			V _L = 3.3 V		1.5	2.4	V
Input hysteresis	V _{hys}				0.5		V
Input resistance		T _A = 25°C		3	5	7	kΩ
Switching characteristics. See figures 6 and 7							
Receiver propagation delay	t _{PHL}	Receiver input to receiver output			0.15		µs
	t _{PLH}	C _L = 150 pF			0.15		
Receiver skew	t _{PHL} - t _{PLH}				50		ns
Receiver output enable time	t _{en}	From $\overline{\text{FORCEOFF}}$			200		ns
Receiver output disable time	t _{dis}	From $\overline{\text{FORCEOFF}}$			200		ns

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions <u>5/</u>	Limits			Unit
			Min	Typ	Max	
DRIVER SECTION						
Electrical characteristics <u>6/</u>						
Output voltage swing	VOH	All driver output load with 3 kΩ to ground, VCC = 3.1 V to 5.5 V	±5	±5.4		V
Output resistance	rO	VCC = V+ = V- = 0, Driver output = ±2V	300	10M		Ω
Output short circuit current	IOS	VT_OUT = 0			±60	mA
Output leakage current	IOZ	VT_OUT = ±12 V, FORCEOFF = GND, VCC = 3 V to 3.6 V			±25	μA
		VT_OUT = ±12 V, FORCEOFF = GND, VCC = 4.5 V to 5.5 V			±25	
Driver input hysteresis					0.5	V
Input leakage current		DIN, FORCEOFF, FORCEON		±0.01	±2.9	μA
Timing requirements. See figures 8 and 9.						
Maximum data rate		RL = 3 kΩ, CL = 200 pF, One driver switching	1000			kbps
Time to exit powerdown		VT_OUT > 3.7 V		100		μs
Driver skew <u>7/</u>	tPHL - tPLH			100		ns
Transition region slew rate	tTHL - tTLH	VCC = 3.3 V, TA = 25°C, RL = 3 kΩ to 7 kΩ, Measured from 3 V to -3 V or -3 V to 3 V, CL = 150 pF to 1000 pF	15		150	V/μs
AUTO POWERDOWN SECTION						
Electrical characteristics <u>6/ 8/</u>						
Receiver input threshold for $\overline{\text{INVALID}}$ high level output voltage	VT+(valid)	FORCEON = GND, FORCEOFF = VL			2.7	V
Receiver input threshold for $\overline{\text{INVALID}}$ high level output voltage	VIT-(valid)	FORCEON = GND, FORCEOFF = VL	-2.7			V
Receiver input threshold for $\overline{\text{INVALID}}$ low level output voltage	VT(invalid)	FORCEON = GND, FORCEOFF = VL	-0.3		0.3	V
$\overline{\text{INVALID}}$ high level output voltage	VOH	IOH = -1 mA, FORCEON = GND, FORCEOFF = VL	VL - 0.6			V
$\overline{\text{INVALID}}$ low level output voltage	VOL	IOH = 1.6 mA, FORCEON = GND, FORCEOFF = VL			0.4	V
Switching characteristic <u>6/ 8/</u> (See figure 10)						
Propagation delay time, low to high level output	tvalid			0.1		μs
Propagation delay time, high to low level output	tinvalid			50		μs
Supply enable time	ten			25		μs
Receiver or driver edge to auto powerdown plus	tdis			30		μs

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over operating free air temperature range, $V_{CC} = V_L = 3\text{ V to }5.5\text{ V}$, $C1 - C4 = 0.1\text{ }\mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\text{ }\mu\text{F}$, $C2 - C4 = 0.33\text{ }\mu\text{F}$ (tested at $5\text{ V} \pm 10\%$) (unless otherwise noted).
- 3/ All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.
- 4/ Testing supply conditions are $C1-C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$; $C1-C4 = 0.22\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, and $C1 = 0.047\text{ }\mu\text{F}$ and $C2-C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.
- 5/ Over operating free air temperature range, $V_{CC} = V_L = 3\text{ V to }5.5\text{ V}$, $C1 - C4 = 0.1\text{ }\mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\text{ }\mu\text{F}$, $C2 - C4 = 0.33\text{ }\mu\text{F}$ (tested at $5\text{ V} \pm 10\%$), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted).
- 6/ Typical values are at $V_{CC} = V_L = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.
- 7/ Driver skew is measured at the driver zero cross point.
- 8/ Over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted).

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Case X

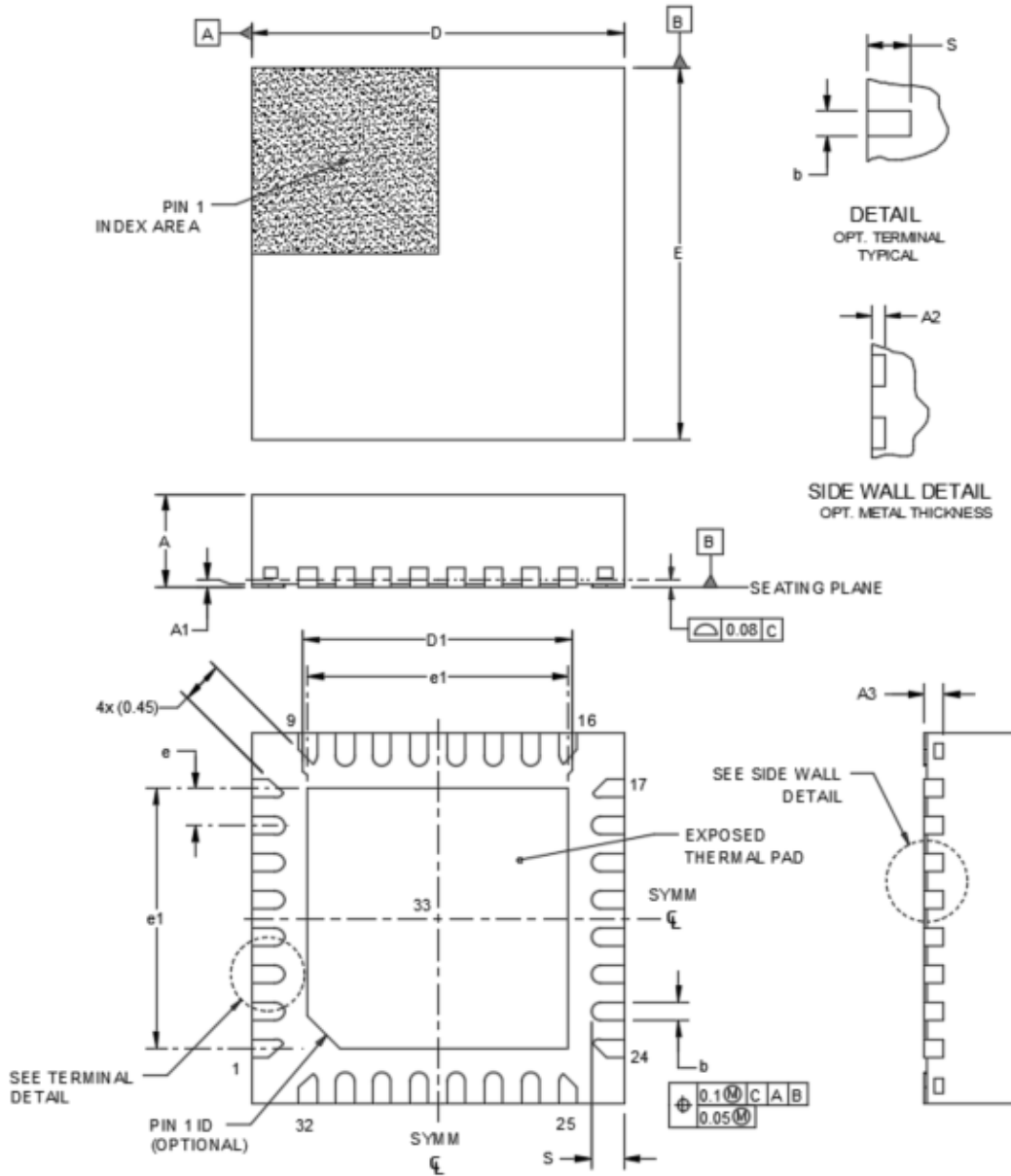


FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeter	
	Minimum	Maximum	Minimum	Maximum
A	---	.039	---	1.00
A1	.000	.002	0.00	0.05
A2	.004 REF		0.10 REF	
A3	.008 REF		0.20 REF	
b	.006	.010	0.15	0.25
D	.153	.161	3.90	4.10
D1	.108	.112	2.75	2.85
E	.153	.161	3.90	4.10
e	.016 BSC		0.4 BSC	
e1	.110 BSC		2.8 BSC	
S	.010	.018	0.25	0.45

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

FIGURE 1. Case outline - Continued.

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Case outline X							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	C2+	9	FORCEON	17	RIN5	25	DOUT1
2	C2-	10	ROUT5	18	RIN4	26	GND
3	V-	11	ROUT4	19	RIN3	27	VCC
4	DIN1	12	ROUT3	20	RIN2	28	$\overline{\text{FORCEOFF}}$
5	DIN2	13	ROUT2	21	RIN1	29	C1+
6	$\overline{\text{INVALID}}$	14	ROUT1	22	DOUT3	30	V+
7	DIN3	15	VL	23	DOUT2	31	C1-
8	NC	16	NC	24	NC	32	NC

FIGURE 2. Terminal connections.

Terminal symbol	Terminal number	Description
C1+, C2+	29, 1	Positive terminal of the voltage-doubler charge pump capacitor.
V+	30	5.5 V supply generated by the charge pump.
C1-, C2-	31, 2	Negative terminal of the voltage doubler charge pump capacitor.
INVALID	6	Invalid output pin.
V-	3	-5.5 V supply generated by the charge pump.
DIN1	4	Driver inputs.
DIN2	5	Driver inputs.
DIN3	6	Driver inputs.
ROUT5 – ROUT1	10, 11, 12, 13, 14	Receiver outputs. Swing between 0 and VL .
VL	15	Logic level supply. All CMOS inputs and outputs are reference to this supply.
RIN5 – RIN1	17, 18, 19, 20, 21	RS-232 receiver inputs.
DOUT3	22	RS-232 driver outputs.
DOUT2	23	RS-232 driver outputs.
DOUT1	25	RS-232 driver outputs.
GND	26	Ground.
VCC	27	3 V to 5.5 V supply voltage.
$\overline{\text{FORCEOFF}}$	28	Powerdown Control input (Refer to truth table).
FORCEON	9	Powerdown Control input (Refer to truth table).

FIGURE 3. Terminal functions.

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Each Driver

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	Time elapsed since last RIN or DIN transition		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto powerdown plus disabled
H	H	H	X	L	
L	L	H	< 30 μs	H	Normal operation with auto powerdown plus enabled
H	L	H	< 30 μs	L	
L	L	H	> 30 μs	Z	Power off by auto-powerdown plus feature
H	L	H	> 30 μs	Z	

H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver

INPUTS			OUTPUTS	RECEIVER STATUS
RIN1-RIN5	$\overline{\text{FORCEOFF}}$	Time elapsed since last RIN or DIN transition	ROUT1 – ROUT5	
X	L		Z	Powered off
L	H	< 30 μs	H	Normal operation with auto powerdown plus disabled/enabled
H	H	< 30 μs	L	
Open	H	< 30 μs	H	

H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

FIGURE 4. Function tables.

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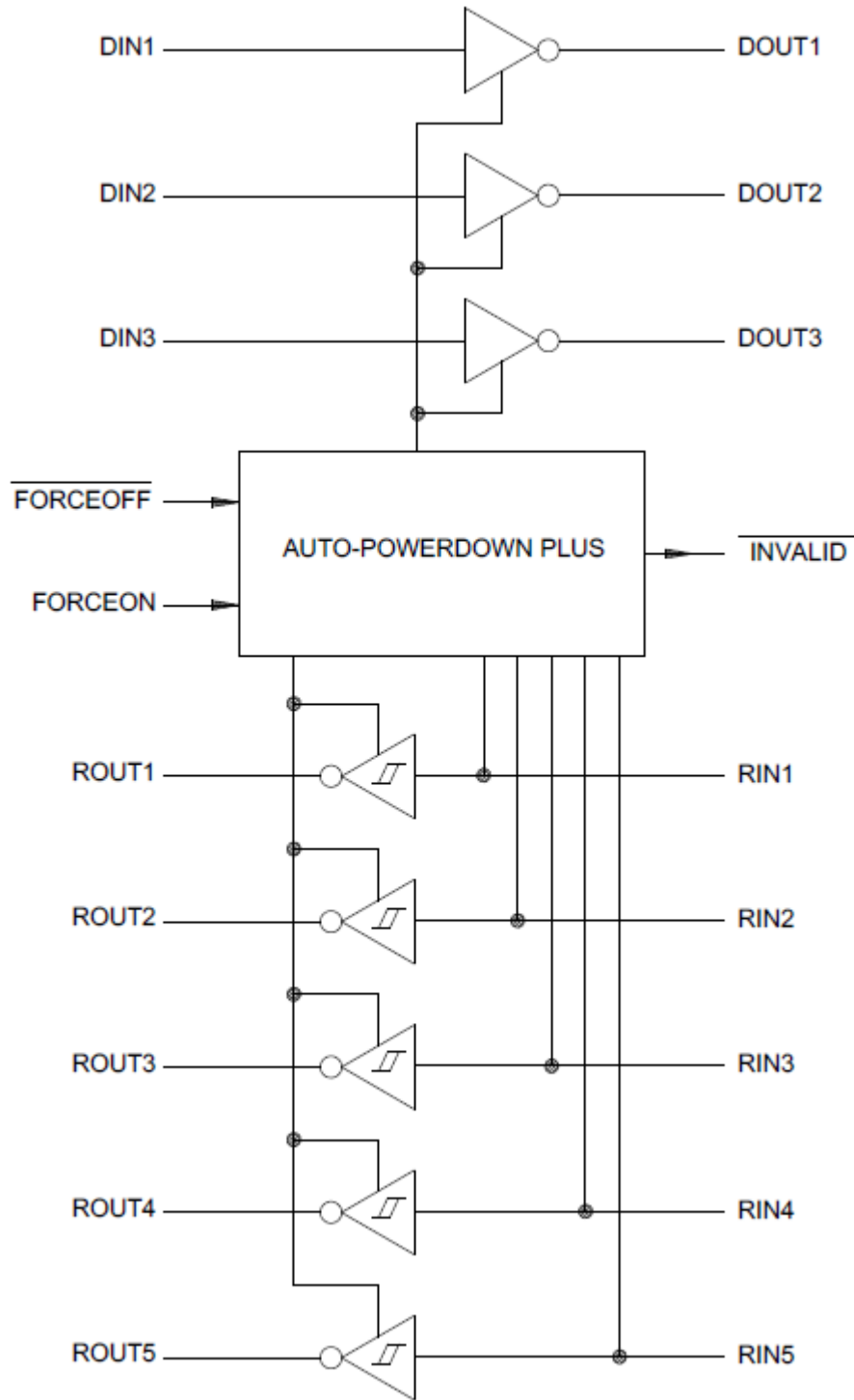
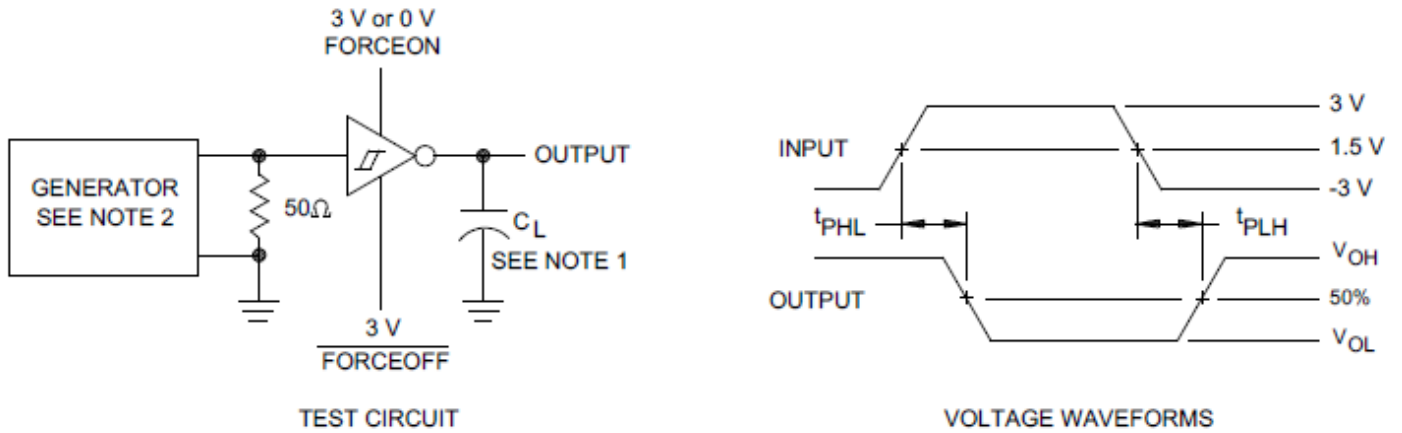


FIGURE 5. Functional block diagram.

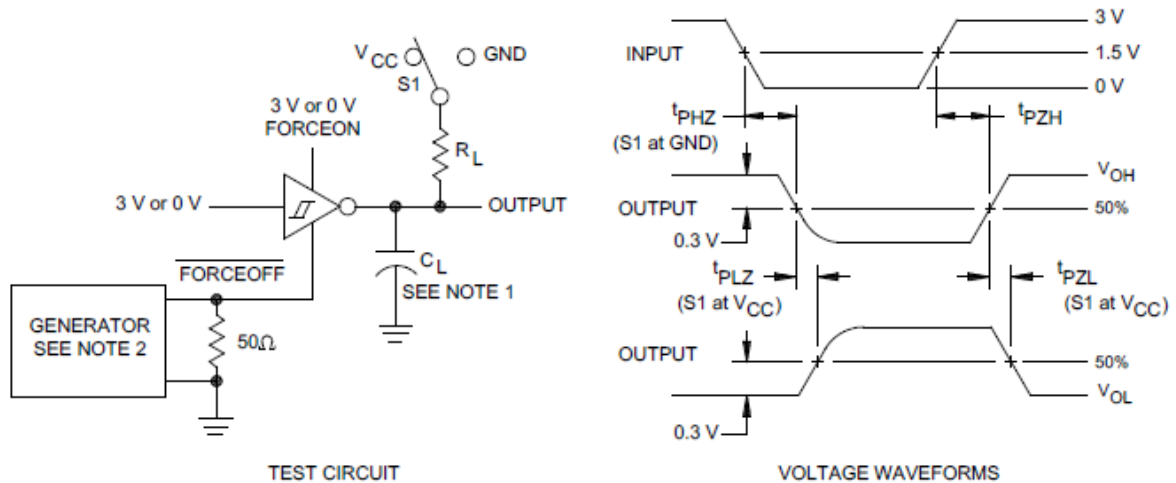
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NOTES:

1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

FIGURE 6. Receiver propagation delay times

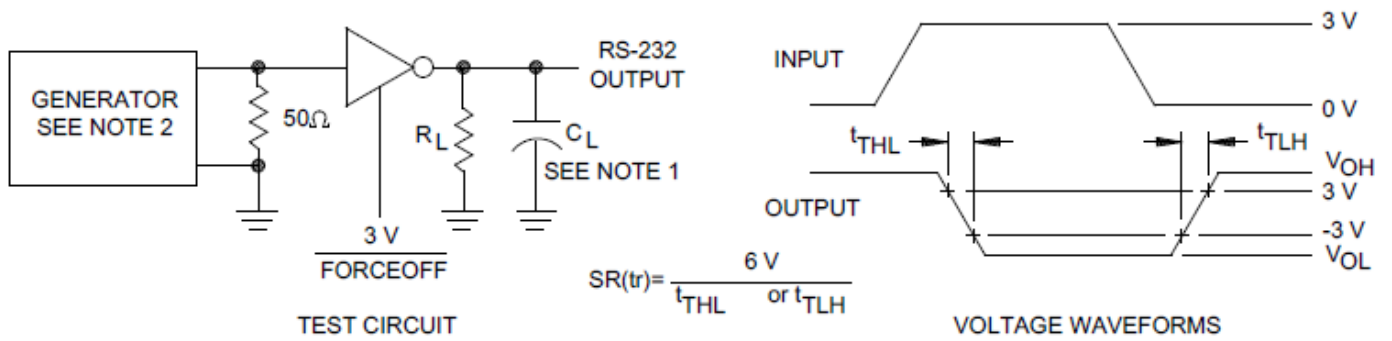


NOTES:

1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
3. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
4. t_{PZL} and t_{PZH} are the same as t_{en} .

FIGURE 7. Receiver enable and disable times.

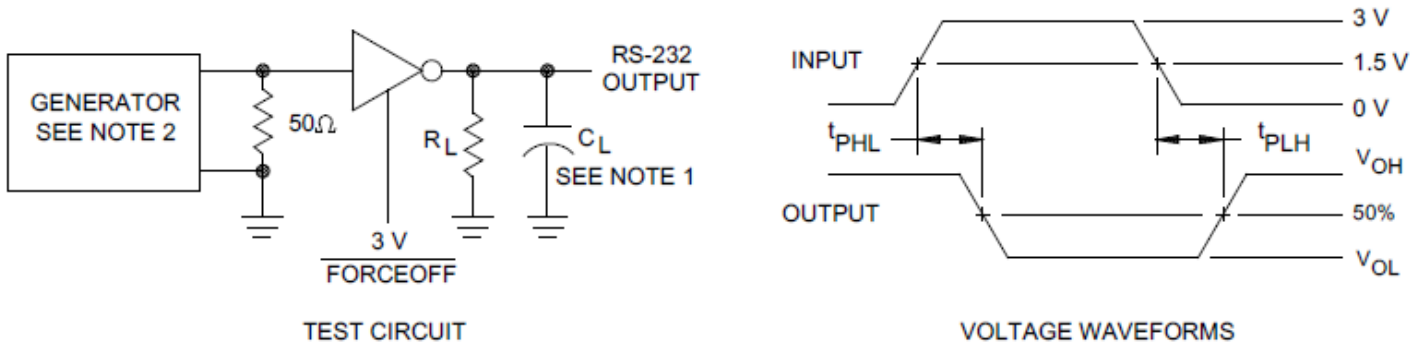
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NOTES:

1. CL includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, ZO = 50 Ω, 50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns.

FIGURE 8. Driver slew rate.

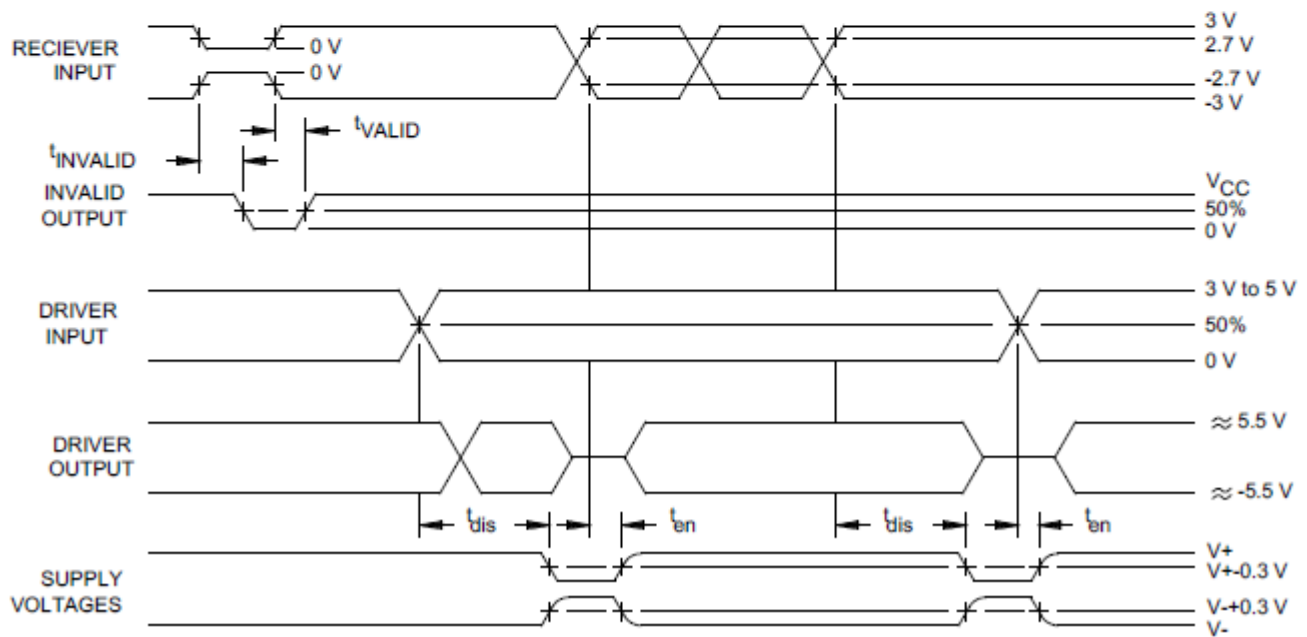
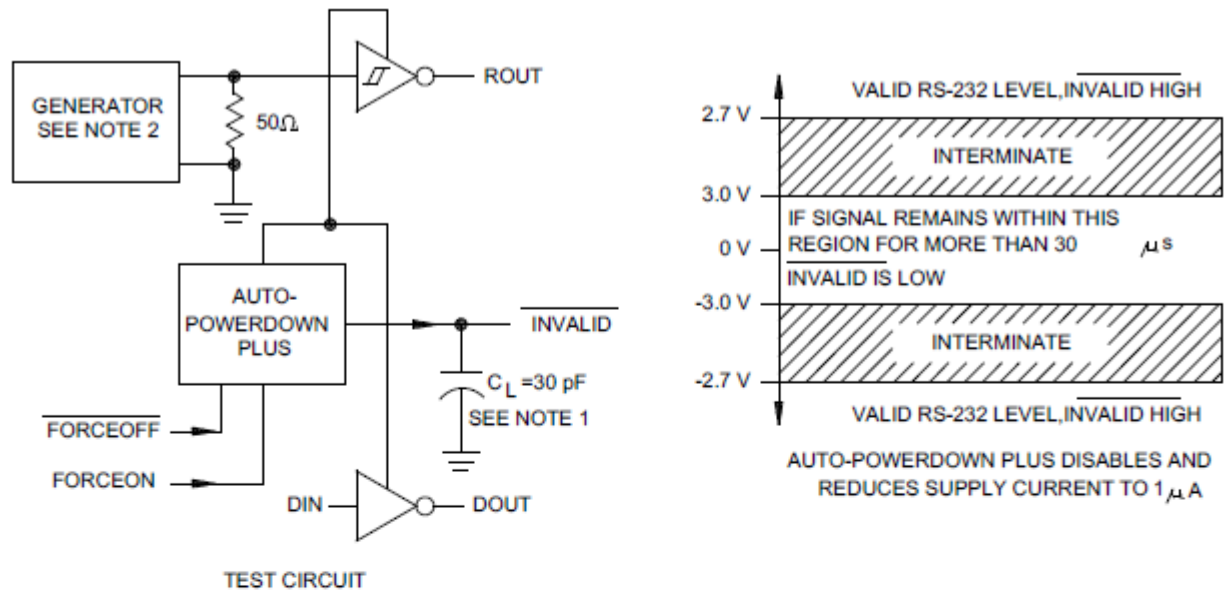


NOTES:

1. CL includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, ZO = 50 Ω, 50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns.

FIGURE 9. Driver pulse skew

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NOTES:

1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

FIGURE 10. $\overline{INVALID}$ propagation delay times and supply enabling time.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/13621-01XE	01295	RS53EP	TRS3253EMRSMREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Incorporated
12500 I Blvd.
Dallas, TX 75243

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13621
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