REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Delete the Continuous total power dissipation table from paragraph 1.3. Add two footnotes to paragraph 6.3. Update document paragraphs to current requirements. - ro	18-09-25	C. SAFFLE
B	Update boilerplate paragraphs to current VID description requirements. - PHN	23-12-12	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B			
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PMIC N/A

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Original date of drawing
YY-MM-DD
13-08-27

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TITLE

MICROCIRCUIT, LINEAR, FAULT-PROTECTED RS-485 TRANSCEIVERS WITH EXTENDED COMMON-MODE RANGE, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**	**DWG NO.**
A	**16236**	**V62/13620**

REV **B**

PAGE 1 **OF** 14

AMSC N/A

5962-V031-24

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance fault protected RS-485 transceivers with extended common mode range microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13620	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65HVD1792-EP	Fault protected RS-485 transceivers with extended common mode range

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	JEDEC MS-012-AB	Plastic Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage, (V_{CC}) ..... -0.5 V to 7.0 V
Voltage range at bus pins (A, B pins) ..... -70 V to 70 V
Input voltage range at any logic pin ..... -0.3 V to V_{CC} + 0.3 V
Transient overvoltage pulse through 100 Ω per TIA-485 ..... -100 V to 100 V
Receiver output current ..... -24 mA to 24 mA
Junction temperature, (T_J) ..... 170°C
IEC 60749-26 ESD (human body model), bus terminals and GND ..... ±16 kV
JEDEC standard 22:
  Test method A114 (human body model), bus terminal and GND ..... ±16 kV
  Test method A114 (human body model), all pins ..... ±4 kV
  Test method C101 (charged-device model), all pins ..... ±2 kV
  Test method A115 (machine model), all pins ..... ±400 V

1.4 Thermal characteristics.

Thermal metric 2/	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} 3/	70.8	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 4/	29.4	
Junction to board thermal resistance, θ_{JB} 5/	25.3	
Junction to top characterization parameter, Ψ_{JT} 6/	8.2	
Junction to board characterization parameter, Ψ_{JB} 7/	25	
Junction to case (bottom) thermal resistance, θ_{JCbot} 8/	N/A	

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ For more information about traditional and new thermal metrics, see manufacturer data.
3/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.
4/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
5/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
6/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
7/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
8/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

1.5 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V to 5.5 V
Input voltage at any bus terminal (separately or common mode) (V_I)	-20 V to 25 V 9/
High level input voltage (driver, driver enable, and receiver enable inputs) (V_{IH})	2 V to V_{CC}
Low level input voltage (driver, driver enable, and receiver enable inputs) (V_{IL})	0 V to 0.8 V
Differential input voltage (V_{ID})	-25 V to 25 V
Output current, (I_O):	
Driver	-60 mA to 60 mA
Receiver	-8 mA to 8 mA
Minimum differential load resistance (R_L)	54 Ω
Typical differential load capacitance (C_L)	50 pF
Maximum signaling rate ($1/t_{UI}$)	1 Mbps
Operating free air temperature (T_A) (see manufacturer application section for thermal information)	-40°C to 105°C
Junction temperature (T_J)	-40°C to 150°C

2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE, SEMICONDUCTOR EQUIPMENT and MATERIALS INTERNATIONAL

ANSI SEMI STANDARD G30-88 - Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available online at https://www.ansi.org.)

International Electrotechnical Commission

IEC 60749-26 – Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM)

(Copies of these documents are available online at https://www.iec.ch)

JEDEC Solid State Technology Association

JEDEC JESD51	–	Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
EIA/JESD51-2a	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
EIA/JEDEC 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
EIA/JESD51-8	–	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JESD22-A114	–	Electrostatic Discharge Sensitivity Testing Human Body Model (HBM)
JESD22-A115	–	Electrostatic Discharge Sensitivity Testing Machine Model (MM)

(Copies of these documents are available online at https://www.jedec.org.)

9/ By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic Diagram (Positive logic). The logic diagram (Positive logic) shall be as shown in figure 3.

3.5.4 Driver function table. The Driver function table shall be as shown in figure 4.

3.5.5 Receiver function table. The Receiver function table shall be as shown in figure 5.

3.5.6 Measurement of Driver differential output voltage with common mode load. The measurement of Driver differential output voltage with common mode load shall be as shown in figure 6.

3.5.7 Measurement of Driver differential and common mode output with RS-485 load. The measurement of Driver differential and common mode output with RS-485 load shall be as shown in figure 7.

3.5.8 Measurement of Driver differential output rise and fall times and propagation delays. The measurement of Driver differential output rise and fall times and propagation delays shall be as shown in figure 8.

3.5.9 Measurement of Driver enable and disable times with active high output and pulldown load. The measurement of Driver enable and disable times with active high output and pulldown load shall be as shown in figure 9.

3.5.10 Measurement of Driver enable and disable times with active low output and pulldown load. The measurement of Driver enable and disable times with active low output and pulldown load shall be as shown in figure 10.

3.5.11 Measurement of receiver output rise and fall times and propagation delays. The measurement of receiver output rise and fall times and propagation delays shall be as shown in figure 11.

3.5.12 Measurement of receiver enable/disable times with drives enabled. The measurement of receiver enable/disable times with drives enabled shall be as shown in figure 12.

3.5.13 Measurement of receiver enable times with driver disabled. The measurement of receiver enable times with driver disabled shall be as shown in figure 13.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/			Limits			Unit
					Min	Typ	Max	
Driver differential output voltage magnitude	$\|V_{OD}\|$	RS-485 with common-mode load, V_{CC} > 4.75 V, see FIGURE 6			1.37			V
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V			1.5	2		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V			2	2.5		
Change in magnitude of driver differential output voltage	$\Delta\|V_{OD}\|$	R_L = 54 Ω			-0.2	0	0.2	V
Steady state common mode output voltage	$V_{OC(SS)}$				1	$V_{CC}/2$	3	V
Change in differential driver output common mode voltage	$\Delta V_{OC(SS)}$				-100	0	100	mV
Peak to peak driver common mode output voltage	$V_{OC(PP)}$	Center of two 27 Ω load resistors, See FIGURE 7				500		mV
Differential output capacitance	C_{OD}					23		pF
Positive going receiver differential input voltage threshold	V_{IT+}	V_{CM} = -20 V to 25 V				-100	-10	mV
Negative going receiver differential input voltage threshold	V_{IT-}				-205	-150		mV
Receiver differential input voltage threshold hysteresis	V_{HYS}				30	50		mV
Receiver high level output voltage	V_{OH}	I_{OH} = -8 mA			2.4	V_{CC} – 0.3		V
		I_{OH} = -400 µA			4			
Receiver low level output voltage	V_{OL}	I_{OL} = 8 mA				0.2	0.5	V
Driver input, driver enable, and receiver enable input current	I_I				-100		100	µA
Receiver output high impedance current	I_{OZ}	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}			-1		1	µA
Driver short circuit output current	I_{OS}				-250		250	mA
Bus input current (disable driver)	I_I	V_{CC} = 4.5 V to 5.5 V or	V_I = 12 V			75	125	µA
		V_{CC} = 0 V, DE at 0 V	V_I = -7 V		-100	-40		
Supply current (quiescent)	I_{CC}	Driver and receiver enabled	DE = V_{CC}, RE = GND, no load			4	6.3	mA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, no load			3	5.2	
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load			2	4.3	
		Driver and receiver disabled	DE = GND, D = open, RE = V_{CC}, no load	T_J = -40°C to 105°C		0.5	5.2	µA
				T_J = 150°C		15	29	
Supply current (dynamic)		See manufacturer data						

See footnote at end of table.

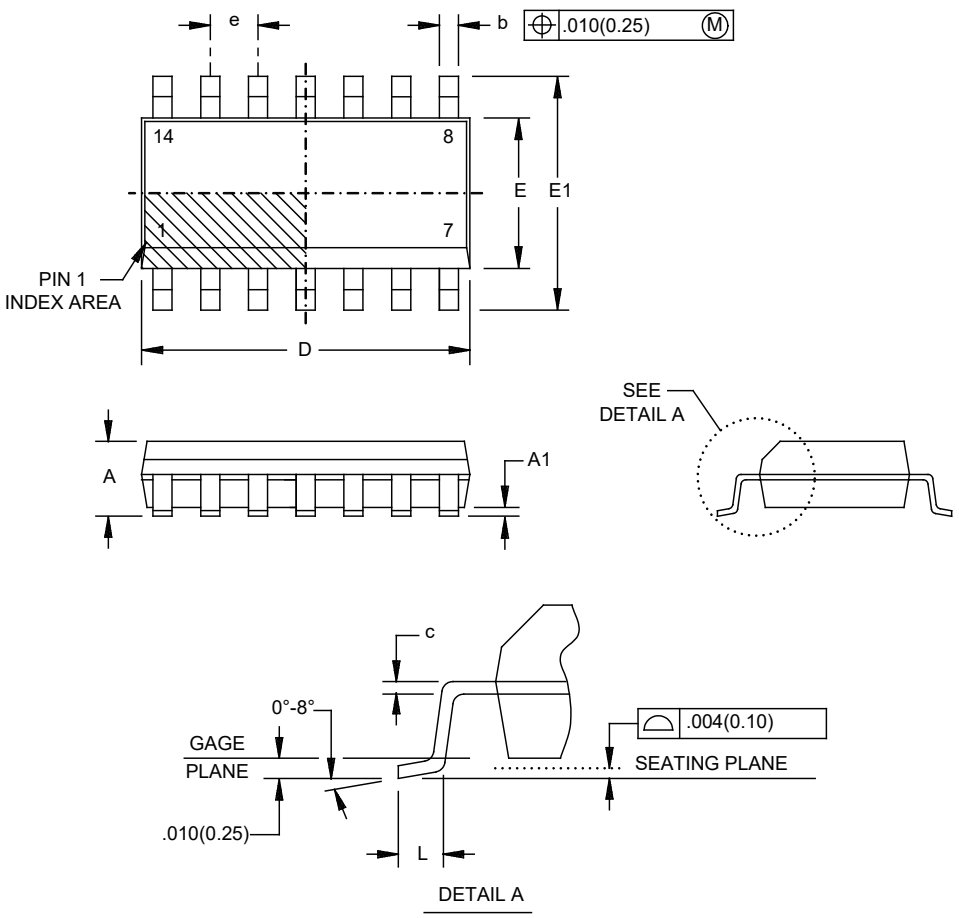
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/		Limits			Unit
				Min	Typ	Max	
SWITCHING CHARACTERISTICS							
Driver							
Driver differential output rise/fall time	t_r, t_f	R_L = 54 Ω, C_L = 50 pF, see FIGURE 8		50		300	ns
Driver propagation delay	t_{PHL}, t_{PLH}					200	ns
Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	$t_{SK(P)}$					29	ns
Driver disable time	t_{PHZ}, t_{PZL}		See FIGURE 9 and 10			3	µs
Driver enable time	t_{PZH}, t_{PZL}	Receiver enabled				300	ns
		Receiver disabled				10	µs
		Receiver enabled	$V_{CM} > V_{CC}$		500		ns
Receiver							
Receiver output rise/fall time	t_r, t_f	CL = 15 pF, see FIGURE 11			4	15	ns
Receiver propagation delay time	t_{PHL}, t_{PLH}				100	200	ns
Receiver output pulse skew, $\|t_{PHL} - t_{PLH}\|$	$t_{SK(P)}$				6	20	ns
Receiver disable time	t_{PLZ}, t_{PHZ}	Driver enabled, see FIGURE 12			15	100	ns
Receiver enable time	$t_{PZL(1)}$, $t_{PZH(1)}$	Driver enabled, see FIGURE 12			80	300	ns
	$t_{PZL(2)}$, $t_{PZH(2)}$	Driver disabled, see FIGURE 13			3	9	µs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over recommended operating conditions (unless otherwise noted).

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.069		1.75	E	.150	.157	3.80	4.00
A1	.004	.010	0.10	0.25	E1	.228	.244	5.80	6.20
b	.012	.020	0.31	0.51	e	.050 BSC		1.27 BSC	
c	.005	.010	0.13	0.25	L	.016	.050	0.40	1.27
D	.337	.344	8.55	8.75					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0.15) each side.
4. Body width does not include interlead flash. Interlead flash shall not exceed.017 (0.43) each side.
5. Falls within JEDEC MS-012 variation AB.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	14	V_{CC}
2	R	13	V_{CC}
3	$\overline{RE}$	12	A
4	DE	11	B
5	D	10	Z
6	GND	9	Y
7	GND	8	NC

NC = No internal connection
Pins 6 and 7 are connected together internally.
Pins 13 and 14 are connected together internally.

FIGURE 2. Terminal connections.

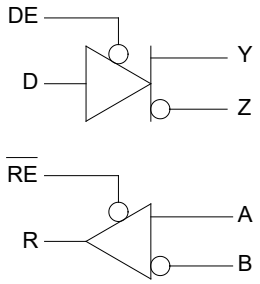


FIGURE 3. Logic diagram (Positive logic).

Input	Enable	Outputs		
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	Open	Z	Z	Driver disabled by default
Open	H	H	L	Actively drive bus high by default

FIGURE 4. Driver function table.

Differential Input	Enable	Output	
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Intermediate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	Open	Z	Receiver disabled by default
Open circuit bus	L	H	Fail safe high output
Short circuit bus	L	H	Fail safe high output
Idle(Terminated) bus	L	H	Fail safe high output

FIGURE 5. Receiver function table.

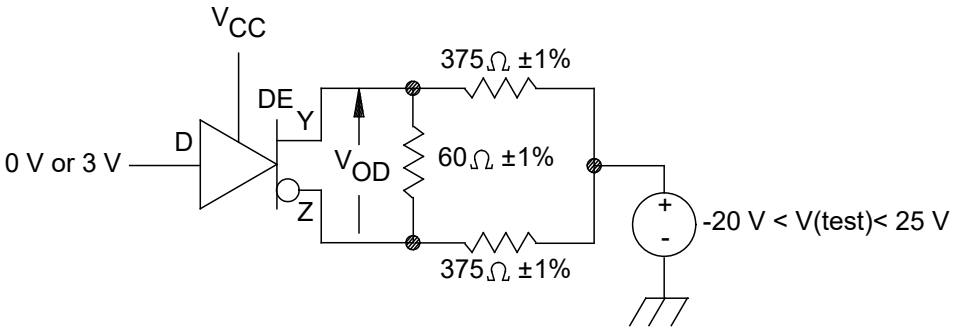


FIGURE 6. Measurement of driver differential output voltage with common mode load.

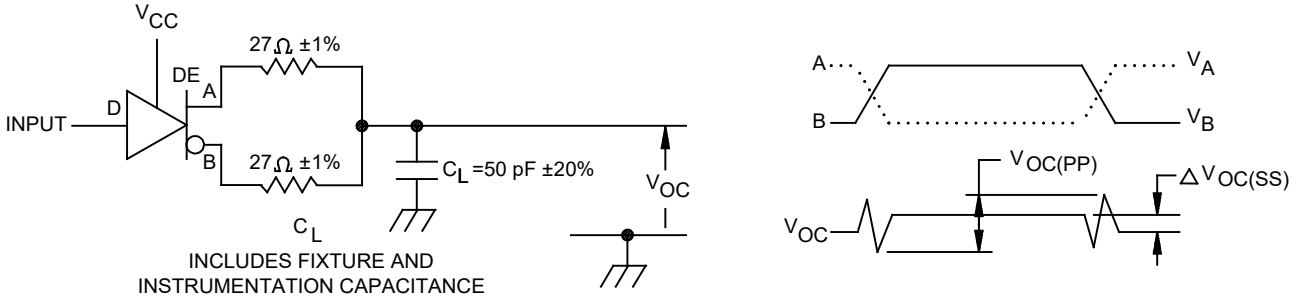


FIGURE 7. Measurement of driver differential and common mode output with RS-485 load.

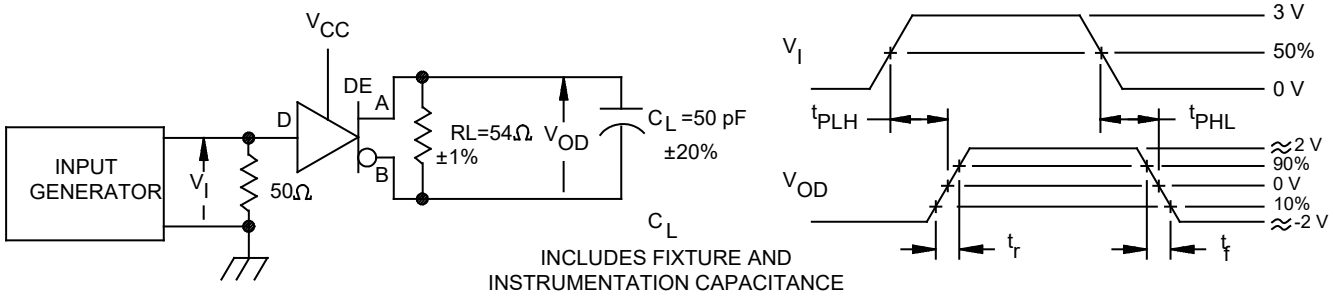
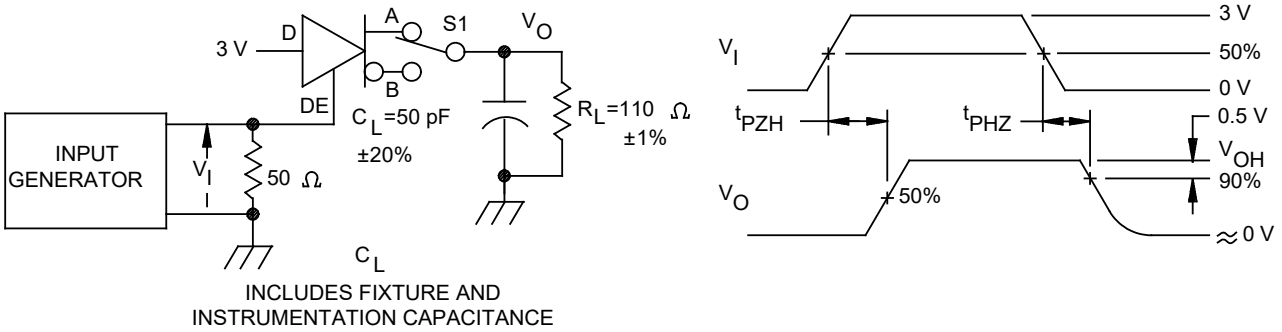
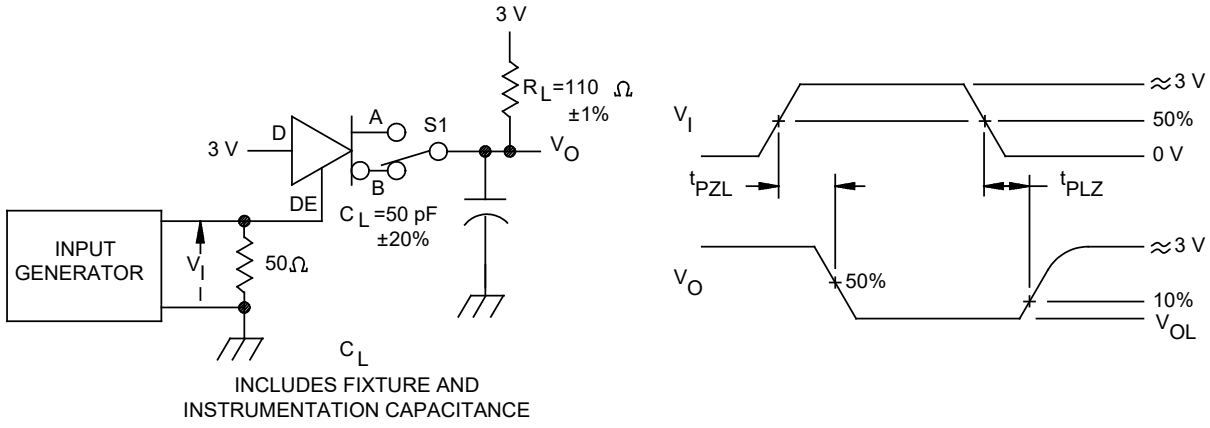


FIGURE 8. Measurement of driver differential output rise and fall times and propagation delays.



NOTE:
1. D at 3 V to test non-inverting output, D at 0 V to test inverting output

FIGURE 9. Measurement of driver enable and disable times with active high output and pulldown load.



NOTE:
1. D at 0 V to test non-inverting output, D at 3 V to test inverting output

FIGURE 10. Measurement of driver enable and disable times with active low output and pulldown load.

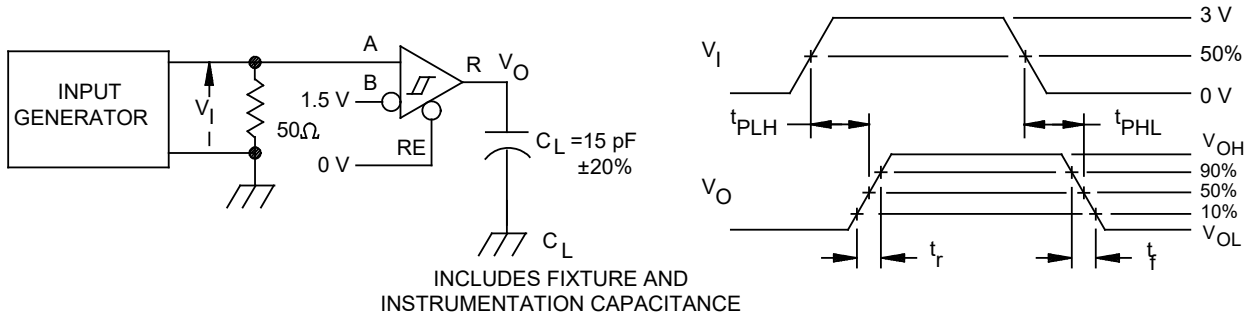


FIGURE 11. Measurement of receiver output rise and fall times and propagation delays.

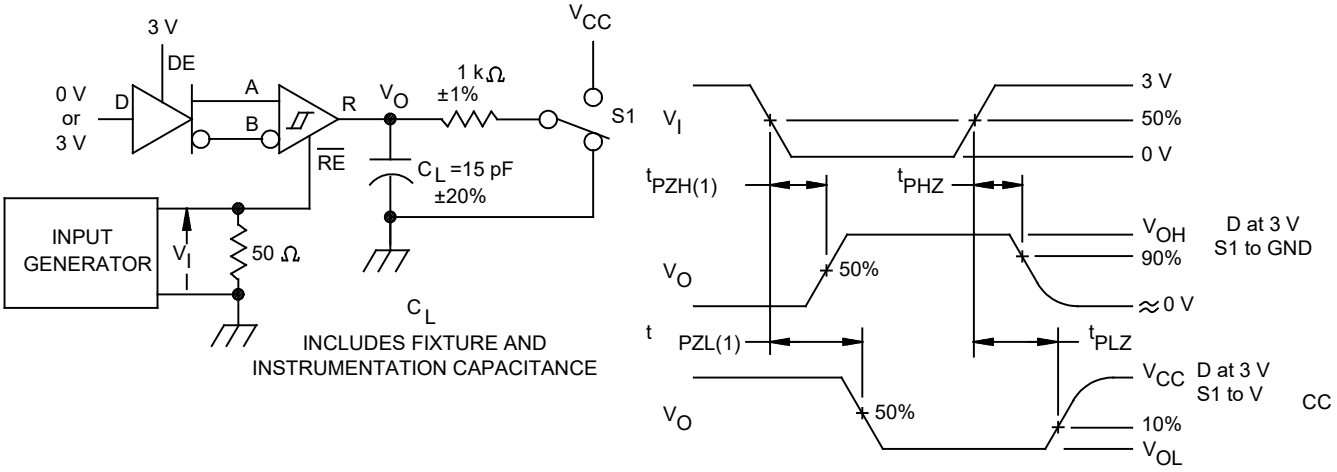


FIGURE 12. Measurement of receiver enable/disable times with drives enabled.

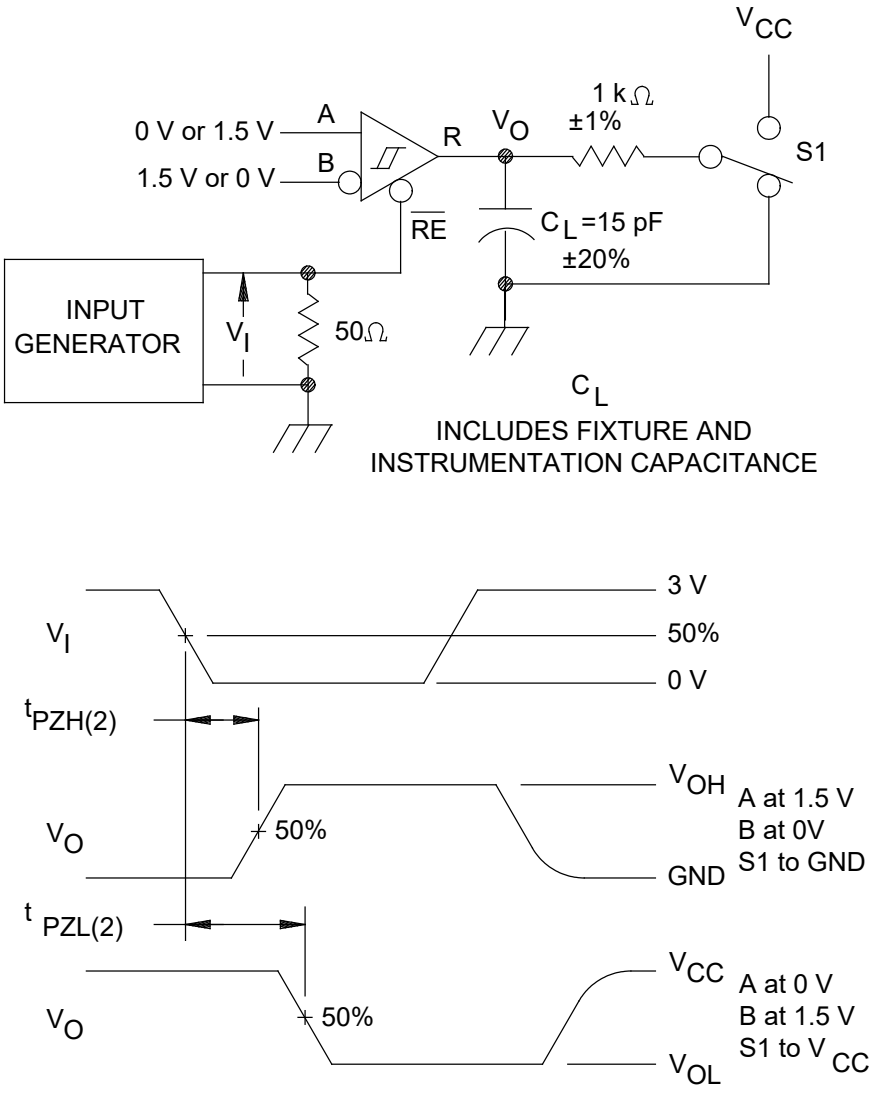


FIGURE 13. Measurement of receiver enable times with driver disabled.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/ 2/ 3/	Device manufacturer CAGE code	Transport media	Vendor part number
V62/13620-01XE	01295	Tape and real	SN65HVD1792TDREP
		Tube	SN65HVD1792TDEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet, or contact the manufacturer.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243