REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**																				
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17			

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 13-07-01	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, LINEAR-DIGITAL, PRESSURE SENSOR SIGNAL CONDITIONER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/13619**
	REV	**PAGE** 1 **OF** 17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance pressure sensor signal conditioner microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13619	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	PGA400-EP	Pressure sensor signal conditioner

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	36	JEDEC MO-220	Plastic quad flatpack no-lead

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Power supply voltage, (V_{DD} Continuous) ..... -5.5 V to 16.0 V
Voltage at VP_OTP ..... -0.3 V to 8.0 V
Voltage at sensor input and drive pins ..... -0.3 V to 3.6 V
Voltage at any IO pin except at VOUT1/OWI ..... -0.3 V to V_{DD} + 0.3 V
Voltage at VOUT1/OWI pin ..... -0.3 V to 7.5 V
Supply current, (I_{DD}, Short on VOUT1 or VOUT2) ..... -45 mA to +45 mA
Output current, (Iout1, Iout2) ..... -30 mA to +30 mA
Minimum ESD
Human Body Model (HBM) ..... ±2 kV
Field induced Charge Device Model (CDM) ..... ±500 V
Maximum junction Temperature, (T_{jmax}) ..... 150°C
Storage temperature, (T_{stg}) ..... -40°C to 150°C

1.4 Thermal characteristics.

Thermal metric	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} 2/	30.6	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 3/	16.4	
Junction to board thermal resistance, θ_{JB} 4/	5.4	
Junction to top characterization parameter, Ψ_{JT} 5/	0.2	
Junction to board characterization parameter, Ψ_{JB} 6/	5.4	
Junction to case (bottom) thermal resistance, θ_{JCbot} 7/	0.7	

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.
3/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
4/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
5/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
6/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
7/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

1.5 Recommended operating conditions.

Power supply voltage, (VDD)	4.5 V to 5.5 V
Maximum power supply current, (I_{DD}):	
Normal mode, V_{DD} = 5 V, No load on VBRG, No load on DAC1 and DAC2	13.6 mA
Low power mode, V_{DD} = 5 V, No load on VBRG, No load on DAC1 and DAC2, AFE turned OFF	9.5 mA
OTP programming voltage, (VP_OTP)	7.0 V to 7.8 V
Maximum OTP programming current, (I_VP_OTP)	3 mA
Minimum OTP programming timing per byte, (tprog_OTP)	120 µs
Operating ambient temperature, (TA)	-40°C to 125°C
Programming temperature, (OTP or EEPROM)	-40°C to 140°C
Maximum micro start-up time, (VDD ramp rate 1V/µs)	250 µs

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51	–	Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).
JESD51-2a	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-8	–	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Applications for copies should be addressed to the American National Standards Institute, Semiconductor Equipment and Materials International, 1819 L Street, NW, 6 th floor, Washington, DC 20036 or online at http://www.ansi.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	TYP	Max	
Over voltage protection						
Over voltage protection threshold	OV		5.5	6.1	7.0	V
Over voltage protection hysteresis	OV_{hyst}			410		mV
Regulators						
AVDD voltage	V_{AVDD}	C_{AVDD} = 100 nF		3.3		V
AVDD current	I_AVDD	V_{AVDD} = 3.3 V			5	mA
DVDD voltage	V_{DVDD}	No EEPROM programming		3.3		V
		EEPROM programming		3.6		
INTERNAL OSCILLATOR AND EXTERNAL CRYSTAL INTERFACE						
Internal Oscillator						
Internal Oscillator frequency		T_{amb} = 25°C	38.4	40	41.6	MHz
Internal Oscillator frequency		Across operating temperature	36.3		43.7	
External 40 MHz crystal						
Low level input voltage on XTAL			-0.3		0.1 x V_{DD}	V
High level input voltage on XTAL			0.7 x V_{DD}		V_{DD} + 0.3	
SENSOR SUPPLY						
VBRG supply for resistive bridge sensors						
Supply voltage	V_{BRG}	0.44 kΩ ≤ R_{BRG} ≤ 20 kΩ	3.2	3.33	3.4	V
Resistive Bridge Resistance	R_{BRG}		0.44		20	kΩ
Capacitive load	C_{BRG}	R_{BRG} = 20 kΩ			500	pF
Line regulation		V_{DD} = 4.5 V, 5.5 V, R_{BRG} = 0.44 kΩ	-40		40	mV
Load regulation		V_{DD} = 5.0 V, 10 µA ≤ I_{LOAD} ≤ 10 mA	-40		40	mV

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	TYP	Max	
SENSOR SUPPLY – Continued.						
ICAPx supply for capacitive sensors						
Supply current amplitude on ICAP, T_A = 25°C	ICAP_A	CI[2:0] = 000, ICAP_V = 100 mV	-5.3		-4.3	µA
		CI[2:0] = 001, ICAP_V = 100 mV	-8		-6.6	
		CI[2:0] = 010, ICAP_V = 100 mV	-10.8		-8.8	
		CI[2:0] = 011, ICAP_V = 100 mV	-13.5		-11.1	
		CI[2:0] = 100, ICAP_V = 100 mV	-16.2		-13.3	
		CI[2:0] = 101, ICAP_V = 100 mV	-18.9		-15.5	
		CI[2:0] = 110, ICAP_V = 100 mV	-21.6		-17.8	
		CI[2:0] = 111, ICAP_V = 100 mV	-24.4		-20.1	
		CI[2:0] = 000, ICAP_V = 3.2 V	4.5		5.6	
		CI[2:0] = 001, ICAP_V = 3.2 V	6.9		8.5	
		CI[2:0] = 010, ICAP_V = 3.2 V	9.2		11.3	
		CI[2:0] = 011, ICAP_V = 3.2 V	11.5		14.1	
		CI[2:0] = 100, ICAP_V = 3.2 V	13.6		16.7	
		CI[2:0] = 101, ICAP_V = 3.2 V	15.8		19.2	
		CI[2:0] = 110, ICAP_V = 3.2 V	18.1		22.1	
		CI[2:0] = 111, ICAP_V = 3.2 V	20.4		24.8	
Variation over temperature			-5.0		+5.0	%
Capacitive sensor drive – Voltage at CPx and CRx pin	CPx_V, CRx_V	CV[1:0] = 00	70	90	110	mV
		CV[1:0] = 01	255	300	345	
		CV[1:0] = 10	425	500	575	
		CV[1:0] = 11	595	700	805	
Self oscillating current mode demodulator for capacitive sensors						
Gain in transimpedance amplifier	R_F / R_{REF}	CR[1:0] = 00, R_{REF} = 78 kΩ	-1.07	-1.01	-0.94	V/V
		CR[1:0] = 01, R_{REF} = 78 kΩ	-2.13	-1.97	-1.82	
		CR[1:0] = 10, R_{REF} = 78 kΩ	-4.24	-3.93	-3.63	
		CR[1:0] = 11, R_{REF} = 78 kΩ	-8.45	-7.85	-7.26	
Feedback capacitor in Transimpedance amplifier	Cf		14	16	18	pF
TEMPERATURE SENSOR						
Temperature range			-55		125	°C
Temperature ADC resolution				10		bits
Temperature ADC update rate				8		ms
Gain 2/			2.7	2.8	2.9	LSB/°C
Offset 2/			-105		-66	LSB
Total error			-4		4	°C

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	TYP	Max	
		ANALOG FRONT ENDS				
Stage 1 Gain for resistive bridge sensors						
Gain steps		Sx_G1[2:0] = 000		3.0		V/V
		Sx_G1[2:0] = 001		4.4		
		Sx_G1[2:0] = 010		6.8		
		Sx_G1[2:0] = 011		10.2		
		Sx_G1[2:0] = 100		14.6		
		Sx_G1[2:0] = 101		25.5		
		Sx_G1[2:0] = 110		34.0		
		Sx_G1[2:0] = 111		51.0		
Band width		-3 dB, Gain = 111		7		KHz
Stage 2 Gain						
Gain steps		Sx_G2[4:0} = 00000	0.97	1.01	1.05	V/V
		Sx_G2[4:0} = 00001	1.06	1.11	1.16	
		Sx_G2[4:0} = 00010	1.18	1.23	1.28	
		Sx_G2[4:0} = 00011	1.31	1.37	1.42	
		Sx_G2[4:0} = 00100	1.45	1.52	1.58	
		Sx_G2[4:0} = 00101	1.61	1.68	1.76	
		Sx_G2[4:0} = 00110	1.79	1.87	1.94	
		Sx_G2[4:0} = 00111	1.98	2.07	2.16	
		Sx_G2[4:0} = 01000	2.20	2.29	2.39	
		Sx_G2[4:0} = 01001	2.44	2.55	2.65	
		Sx_G2[4:0} = 01010	2.71	2.83	2.94	
		Sx_G2[4:0} = 01011	3.00	3.13	3.26	
		Sx_G2[4:0} = 01100	3.34	3.48	3.62	
		Sx_G2[4:0} = 01101	3.74	3.90	4.06	
		Sx_G2[4:0} = 01110	4.12	4.30	4.48	
		Sx_G2[4:0} = 01111	4.61	4.81	5.01	
		Sx_G2[4:0} = 10000	5.09	5.31	5.54	
		Sx_G2[4:0} = 10001	5.67	5.92	6.16	
		Sx_G2[4:0} = 10010	6.26	6.52	6.79	
		Sx_G2[4:0} = 10011	6.93	7.23	7.53	
		Sx_G2[4:0} = 10100	7.70	8.04	8.37	
		Sx_G2[4:0} = 10101	8.57	8.95	9.32	
		Sx_G2[4:0} = 10110	9.54	9.96	10.37	
		Sx_G2[4:0} = 10111	10.62	11.06	11.51	
		Sx_G2[4:0} = 11000	11.76	12.27	12.79	
		Sx_G2[4:0} = 11001	13.02	13.58	14.15	
		Sx_G2[4:0} = 11010	14.48	15.10	15.72	
		Sx_G2[4:0} = 11011	16.03	16.71	17.40	
		Sx_G2[4:0} = 11100	17.72	18.53	19.34	
		Sx_G2[4:0} = 11101	19.61	20.49	21.37	
		Sx_G2[4:0} = 11110	21.72	22.70	23.68	
		Sx_G2[4:0} = 11111	23.85	25.06	26.28	
Bandwidth		-3dB, Gain setting = 11111	120			KHz

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	TYP	Max	
Offset and offset TC compensation						
Offset compensation low		Offset setting = 0x000, Stage 1 Gain setting = 0b000	-385	-324	-279	mV
Offset compensation high		Offset setting = 0x3FF, Stage 1 Gain setting = 0b000	279	324	385	mV
Offset compensation resolution		Stage 1 gain setting = 0b000	0.59		0.72	mV/step
Offset TC compensation low		Offset TC setting = 0x00, Stage 1 Gain value = 0b000		-371		µV/°C
Offset TC compensation high		Offset TC setting = 0x3F, Stage 1 Gain value = 0b000		361		µV/°C
Offset TC compensation resolution		Stage 1 gain value = 0b000		11.6		µV/V/°C/step
Reference temperature				22		°C
ANALOG TO DIGITAL CONVERTER						
ADC Buffer for 16 bit AD converter 1						
Gain			1.9	2	2.1	V/V
DC level shift		ADC_BUF bit = 1	-1.74	-1.65	-1.55	V
DC offset			-15		15	mV
ADC Buffer for 10 bit AD converter 2						
VIN3 Input voltage range			0.425		1.7	V
Gain			1.09	1.15	1.21	V/V
DC offset			-15		15	mV
VIN3 voltage versus ADC code						
Gain 3/			740	760	780	LSB/V
Offset 3/			-850	-820	-790	LSB
Gain temperature coefficient		T_{amb} = 25°C		0.02		LSB/V/°C
Offset temperature coefficient		T_{amb} = 25°C		-0.02		LSB/°C
Integral nonlinearity			-1		1	LSB
One wire interface						
Communication Baud rate			2400		115000	Bits per second
OWI enable	OWI_EN		6.5		7.0	V
OWI enable hysteresis	OWI_EN_{hys}			50		mV
Internal pullup				10		kΩ
Activation signal pulse low time			12			ms
Activation signal pulse high time			12			ms
OWI transceiver RX threshold	OWI_VIH		0.7 x V_{DD}		V_{DD} + 0.3	V
OWI transceiver RX threshold	OWI_VIL		-0.3		0.3 x V_{DD}	
OWI transceiver TX threshold	OWI_VOH	VDD = 5 v	4.0			
OWI transceiver TX threshold	OWI_VOL	VDD = 5 v			0.8	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 4/	Limits			Unit
			Min	TYP	Max	
Serial Peripheral interface (SPI) interface						
High-level input voltage	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Low-level input voltage	V_{IL}		-0.3		0.3 x V_{DD}	
High-level output voltage	V_{OH}		4.0			
Low-level output voltage	V_{OL}				0.8	
SPI frequency	f_{SCK}				4	MHz
$\overline{CS}$ low to first SCK rising edge	t_{CSSCK}		25			ns
Last SCK rising edge to $\overline{CS}$ rising edge	t_{SCKCS}		125			
$\overline{CS}$ disable time	t_{CSD}		500			
SDI setup time	t_{DS}		25			
SDI hold time	t_{DH}		25			
SDI Fall/Rise time	t_{SDIS}				7	
SCK rise time	t_{SCKR}				7	
SCK fall time	t_{SCKF}				7	
SCK high time	t_{SCKH}		125			
SCK low time	t_{SCKL}		125			
SDO enable time	t_{SDOE}		15			
SCK rising edge to SDO data valid	t_{ACCS}		15			
SDO disable time	t_{SDOD}				15	
SDO Rise/Fall time	t_{SDOS}		3		11	
Capacitive load for data output (SDO)	$C_{L(SDO)}$			10		pF
I2C interface						
High-level input voltage	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Low-level input voltage	V_{IL}		-0.3		0.3 x V_{DD}	
High-level output voltage	V_{OH}		4.0			
Low-level output voltage	V_{OL}				0.8	
SCL clock frequency	f_{SCL}				400	KHz
START condition setup time	t_{STASU}		500			ns
START condition hold time	t_{STAHD}		500			
SCL low time	t_{LOW}		1.25			µs
SCL high time	t_{HIGH}		1.25			
SCL and SDA rise time	t_{RISE}				7	ns
SCL and SDA fall time	t_{FALL}				7	
Data setup time	t_{DATSU}		500			
Data hold time	t_{DATHD}		500			
STOP condition setup time	t_{STOPSU}		500			

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	TYP	Max	
Non volatile memory						
OTP				8		KB
OTP number of Erase/Write cycles		Erase using UV light			10	Cycles
EEPROM		Programmable using SPI or OWI		89		Bytes
		Number of bytes writeable by 8051		16		
EEPROM Erase/Write cycles					1000	Cycles
GPIO						
High-level input voltage	V_{IH}	$R_{LOAD} \geq 10$ kΩ to V_{DD} or to 0 V	0.7 x VDD		VDD + 0.3	V
Low-level input voltage	V_{IL}	$R_{LOAD} \geq 10$ kΩ to V_{DD} or to 0 V	-0.3		0.3 x VDD	
High-level output voltage	V_{OH}	I_{OH} = 1 mA	4.0			
Low-level output voltage	V_{OL}	I_{OL} = -1 mA			0.8	
High-level output current	I_{OH}	V_{OH} = 4.5 V			1	mA
Low-level output current	I_{OL}	V_{OL} = 0.5 V			1	
Pull-up resistance	R_{PU}			160		kΩ
DAC1 and DAC2 output						
Settling time		DAC code 000h to FFFh step. Output is 90% of Full scale. R_{LOAD} = 5 kΩ, C_{LOAD} = 500 pF			7	µs
Zero scale error		DAC code = 000h, I_{DAC} = 1.5 mA			46	mV
Full scale voltage		Output when DAC code is FFFh, I_{DAC} = -1.5 mA	4.85		4.95	V
Output current amplitude		DAC code = 0FFFh, DAC code = 0000h			1.5	mA
Short circuit source current		V_{DD} = 5 V, DAC code = 000h	-34		-10	mA
Short circuit sink current		V_{DD} = 5 V, DAC code = FFFh	10		34	mA
INL (best-fit line)			-3.5		3.5	LSB
INPUT CAPTURE AND OUTPUT COMPARE						
Input capture ports						
High level input voltage	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Low level input voltage	V_{IL}		-0.3		0.3 x V_{DD}	V
Input capture timer clock frequency		10_20_MHz bit = 1		10		MHz
		10_20_MHz bit = 0		20		
Input capture timer bits				16		Bits
Output compare ports						
High level output voltage		I_{OH} = 1 mA	V_{DD} - 1.0			V
Low level output voltage		I_{OL} = -1 mA			0.8	V
Output compare timer frequency		10_20_MHz bit = 1		10		MHz
		10_20_MHz bit = 0		20		
output compare timer bits				16		Bits
High level output current					1	mA
Low level output current					1	mA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	TYP	Max	
Diagnostics						
8051 Software watchdog				500		ms
Main clock normal operation range			35	40	45	MHz
Sensor supply over voltage threshold	VBRG_OV		3.55	3.65	3.75	V
Sensor supply under voltage threshold	VBRG_UV		2.9	3.0	3.11	V
AVDD OV threshold			3.7		3.95	V
AVDD UV threshold			2.72		3.1	V
Output overvoltage threshold for gain stage 1 and 2	$Sensor_{OV}$		2.3	2.5	2.6	V
Output undervoltage threshold for gain stage 1 and 2	$Sensor_{UV}$		0.7	.85	1.0	V
Capacitive sensor interface clock high frequency fault threshold	f_cap_{High}		1.5		2.5	MHz
Capacitive sensor interface clock low frequency fault threshold	f_cap_{Low}		30		50	kHz
EEPROM CHG PUMP overvoltage threshold				14.65		V
EEPROM CHG PUMP undervoltage threshold				11.45		V
DAC loop back voltage gain			0.537	0.545	0.557	V/V
Open wire leakage current 1 – open VDD with pull up on VOUT1					2	µA
Open wire leakage current 2 – open GND with pull down on VOUT1					20	µA

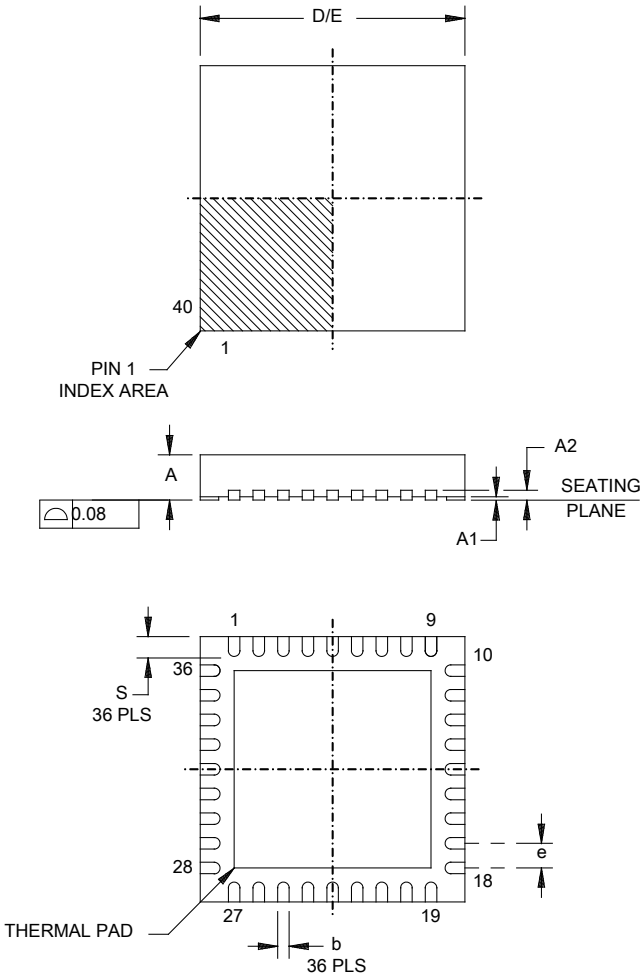
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ The temperature ADC value is given by the equation: ADC Code = Gain*Temperature (in°C) + Offset.

3/ ADC code = Gain*VIN3 + Offset.

4/ Over operating free air temperature range (unless otherwise noted).

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	D/E	5.90	6.10
A1		0.05	e	0.50 BSC	
A2	0.20 REF		S	0.45	0.65
b	0.18	0.30			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. QFN (Quad Flatpack No-Lead) package configuration.
4. The package thermal pad must be soldered to the board for thermal and mechanical performance.
5. See the additional figure in the Product Data Sheet from manufacturer for details regarding the exposed thermal pad features and dimensions.
6. Falls within JEDEC MO-220.

FIGURE 1. Case outline.

Case outline X							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GPIO_2	10	VIN1P	19	AVSS	28	MISO
2	GPIO_1	11	ICAP1	20	AVDD	29	AVDD
3	VP_OTP	12	VN1N	21	VDD	30	VDD
4	VOUT1	13	VIN2P	22	DVSS	31	DVSS
5	GND	14	ICAP2	23	NC	32	NC
6	VOUT2	15	VIN2N	24	DVDD	33	DVDD
7	TIP	16	VIN3	25	DVDD	34	DVDD
8	TIN	17	NC	26	GND	35	GND
9	VBRG	18	GND	27	CSN	36	CSN

FIGURE 2. Terminal connections.

Terminal		Description
Name	No.	
GPIO_2	1	General purpose IO 2 / input capture port 2
GPIO_1	2	General purpose IO 1 / input capture port 1 / I2C Data
VT_OTP	3	One time programmable memory programming voltage
VOUT1	4	DAC1 output / One wire interface
GND	5, 18, 26	Ground
VOUT2	6	DAC2 output
TIP	7	Test pin reserved
TIN	8	Test pin reserved
VBRG	9	Resistive bridge supply voltage
VIN1P	10	Resistive sensor 1 positive input / capacitive sensor 1 positive input
ICAP1	11	Capacitive sensor drive current 1
VIN1N	12	Resistive sensor 1 negative input / capacitive sensor 1 reference input
VIN2P	13	Resistive sensor 2 positive input / capacitive sensor 2 positive input
ICAP2	14	Capacitive sensor drive current 2
VIN2N	15	Resistive sensor 2 negative input / capacitive sensor 2 reference input
VIN3	16	External temperature sensor input
NC	17, 23	No connect
AVSS	19	Ground
AVDD	20	Linear regulator output for internal analog circuit supply
VDD	21	Input power supply
DVSS	22	Ground
DVDD	24, 25	Linear regulator output for internal digital circuit supply
CSN	27	Serial peripheral interface chip select
MISO	28	Serial peripheral interface slave data out
MOSI	29	Serial peripheral interface slave data in
SCK	30	Serial peripheral interface clock
TxD	31	8051 UART Tx (Port 3_1)
RxD	32	8051 UART Rx (Port 3_0)
XTAL	33	XTAL External crystal input
GPIO5	34	General purpose IO 5
GPIO4	35	General purpose IO 4 / output compare port 2
GPIO3	36	General purpose IO 3 / output compare port 1 / I2C Clock

FIGURE 3. Terminal description.

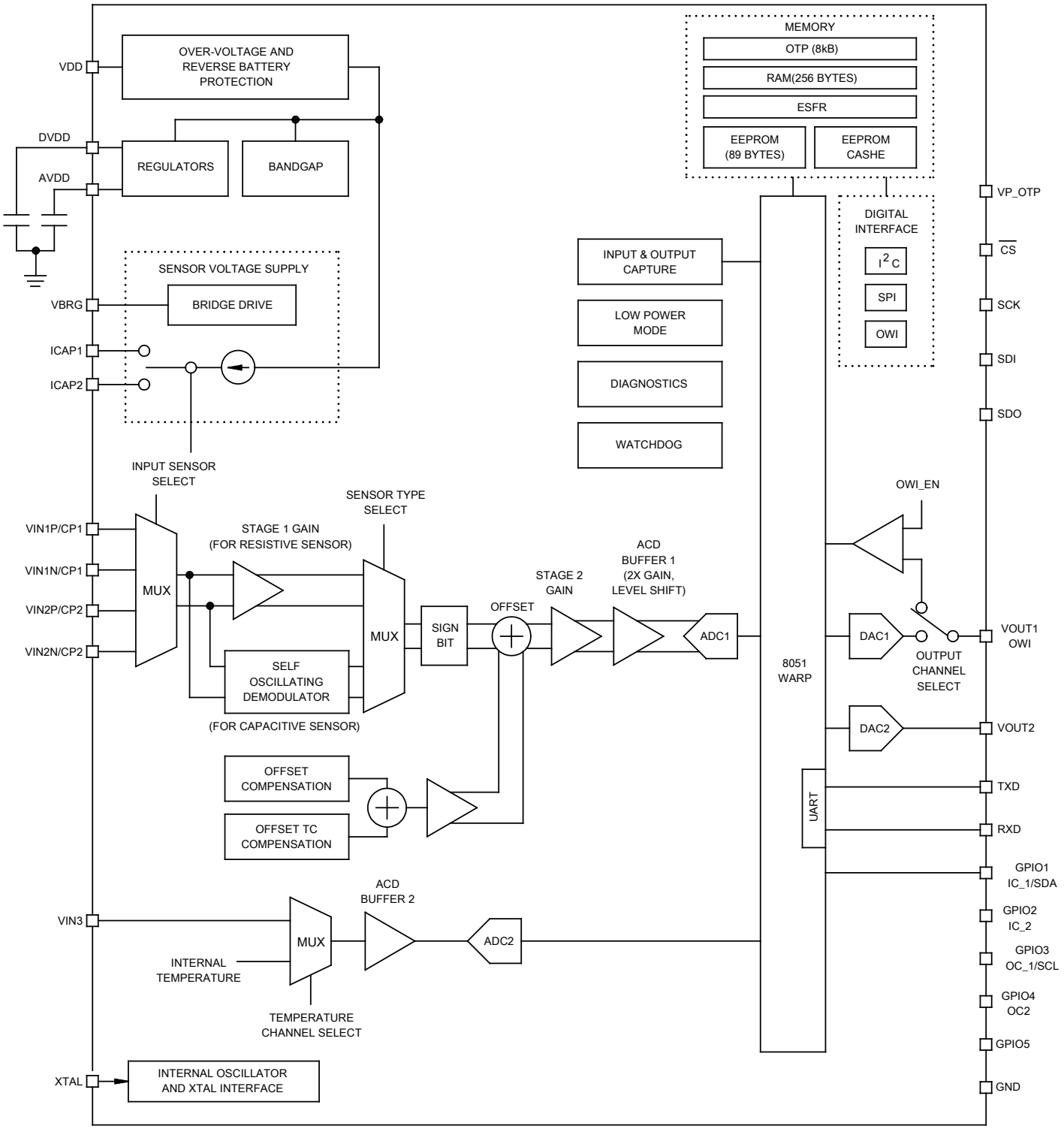


FIGURE 4. Functional block diagram.

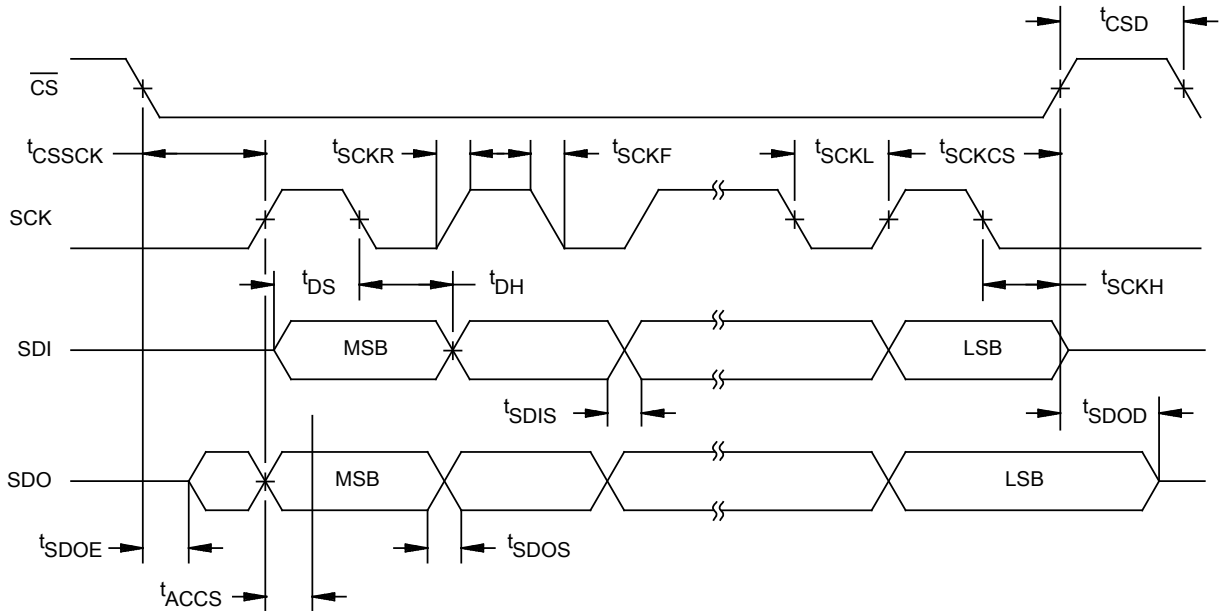


FIGURE 5. SPI timing.

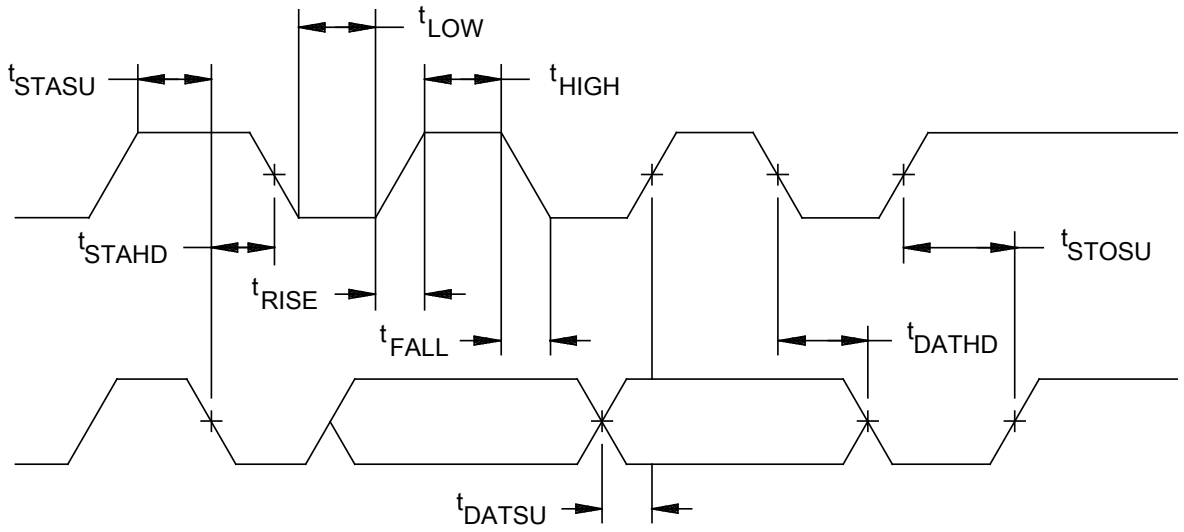


FIGURE 6. I^2C timing.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/13619-01XE	01295	PGA400QRHHTEP	PGA400QRHH-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493