REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13							

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 13-11-07	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	**TITLE** MICROCIRCUIT, LINEAR, DUAL PERIPHERAL NAND DRIVER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/13618**
	REV	**PAGE** 1 **OF** 13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual peripheral NAND driver microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13618	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65472-EP	Dual peripheral NAND driver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... 7 V maximum 2/
Input voltage (V_{IN}) ..... 5.5 V maximum
Inter-emitter voltage ..... 5.5 V maximum 3/
Off state output voltage (V_{OUT}) ..... 70 V
Continuous collector or output current ..... 400 mA 4/
Peak collector or output current ($t_W \leq 10$ ms, duty cycle $\leq$ 50%) ..... 500 mA 4/
Absolute maximum junction temperature range (T_J) ..... -40°C to +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage (V_{CC}) ..... 4.75 V minimum
5 V nominal
5.25 V maximum
High level input voltage (V_{IH}) ..... 2 V minimum
Low level input voltage (V_{IL}) ..... 0.8 V maximum
Operating free-air temperature range (T_A) ..... -40°C to +85°C
Operating virtual junction temperature (T_J) ..... -40°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Unless otherwise specified, voltage values are with respect to the network GND.

3/ This is the voltage between two emitters, A and B.

4/ Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient 6/	θ_{JA}	115.3	°C/W
Thermal resistance, junction-to-case (top) 7/	$\theta_{JC(TOP)}$	59.7	°C/W
Thermal resistance, junction-to-board 8/	θ_{JB}	56.2	°C/W
Characterization parameter, junction-to-top 9/	ψ_{JT}	13.5	°C/W
Characterization parameter, junction-to-board 10/	ψ_{JB}	55.6	°C/W

6/ The thermal resistance, junction-to-ambient under natural convection is obtained in a simulation on a JEDEC standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

7/ The thermal resistance, junction-to-case (top) is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

8/ The thermal resistance, junction-to-board is obtained by simulating in an environment with a ring cold plate fixture to control the printed circuit board (PCB) temperature, as described in JESD51-8.

9/ Characterization parameter, junction-to-top (ψ_{JT}) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

10/ Characterization parameter, junction-to-board (ψ_{JB}) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE

ANSI SEMI STANDARD G30-88 - Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Applications for copies should be addressed to the American National Standards Institute, Semiconductor Equipment and Materials International, 1819 L Street, NW, 6 th floor, Washington, DC 20036 or online at http://www.ansi.org)

JEDEC Solid State Technology Association

JESD 51-2a	-	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JEDEC 51-7	-	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD 51-8	-	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
JEDEC PUB 95	-	Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuits shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A 2/	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V_{IK}	V_{CC} = 4.75 V, I_{IN} = -12 mA	-40°C to +85°C	01		-1.5	V
			+25°C		-1.2 typical		
High level output current	I_{OH}	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 70 V	-40°C to +85°C	01		270	µA
Low level output voltage	V_{OL}	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA	-40°C to +85°C	01		0.4	V
			+25°C		0.25 typical		
		V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA	-40°C to +85°C			0.75	
			+25°C		0.5 typical		
Input current at maximum input voltage	I_{IN}	V_{CC} = 5.25 V, V_{IN} = 5.5 V	-40°C to +85°C	01		1	mA
High level input current	I_{IH}	V_{CC} = 5.25 V, V_{IN} = 2.4 V	-40°C to +85°C	01		44	µA
Low level input current	I_{IL}	V_{CC} = 5.2 5 V, V_{IN} = 0.4 V	-40°C to +85°C	01		-1.6	mA
			+25°C		-1 typical		
Supply current, outputs high	I_{CCH}	V_{CC} = 5.25 V, V_{IN} = 5 V	-40°C to +85°C	01		17	mA
			+25°C		13 typical		
Supply current, outputs low	I_{CCL}	V_{CC} = 5.25 V, V_{IN} = 0 V	-40°C to +85°C	01		76	mA
			+25°C		61 typical		
Switching characteristics.		V_{CC} = 5 V, T_A = +25°C					
Propagation delay time, low to high level output	t_{PLH}	I_O = 200 mA, C_L = 15 pF, R_L = 50 Ω, see figure 5	+25°C	01		65	ns
					45 typical		
Propagation delay time, high to low level output	t_{PHL}	I_O = 200 mA, C_L = 15 pF, R_L = 50 Ω, see figure 5	+25°C	01		50	ns
					30 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A 2/	Device type	Limits		Unit
					Min	Max	
Switching characteristics – continued. V_{CC} = 5 V, T_A = +25°C							
Transition time, low to high level output	t_{TLH}	I_O = 200 mA, C_L = 15 pF, R_L = 50 Ω, see figure 5	+25°C	01		25	ns
					13 typical		
Transition time, high to low level output	t_{THL}	I_O = 200 mA, C_L = 15 pF, R_L = 50 Ω, see figure 5	+25°C	01		20	ns
					10 typical		
High level output voltage after switching	V_{OH}	V_S = 55 V, I_O = 300 mA, see figure 5	+25°C	01	V_S - 18		mV

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All typical values are at V_{CC} = 5 V and T_A = +25°C.

Case X

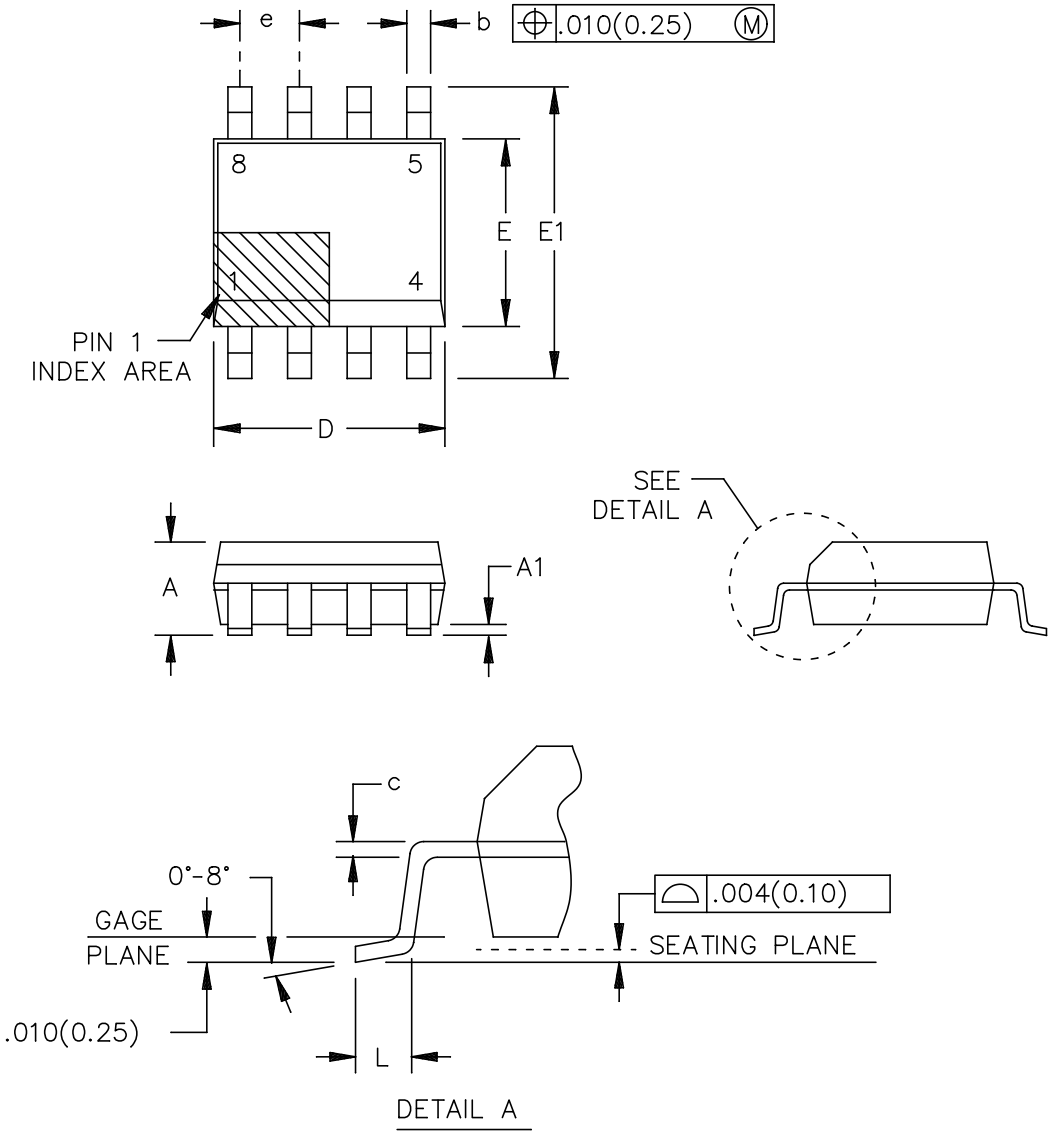


FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE **A**	CODE IDENT NO. **16236**	DWG NO. **V62/13618**
		REV	PAGE 8

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) each side.
4. Falls with JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	1A
2	1B
3	1Y
4	GND
5	2Y
6	2A
7	2B
8	V_{CC}

FIGURE 2. Terminal connections.

Inputs		Output
A	B	Y See note
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

NOTE: Positive logic = $Y = \overline{AB}$ or $\overline{A} + \overline{B}$.

FIGURE 3. Truth table.

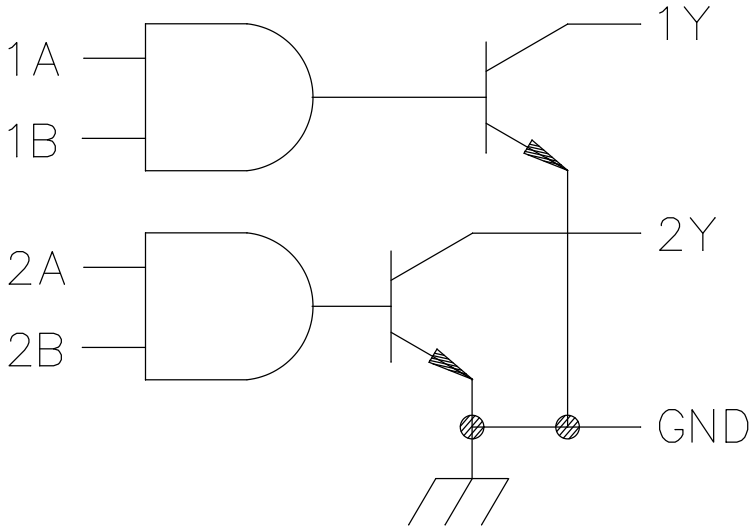
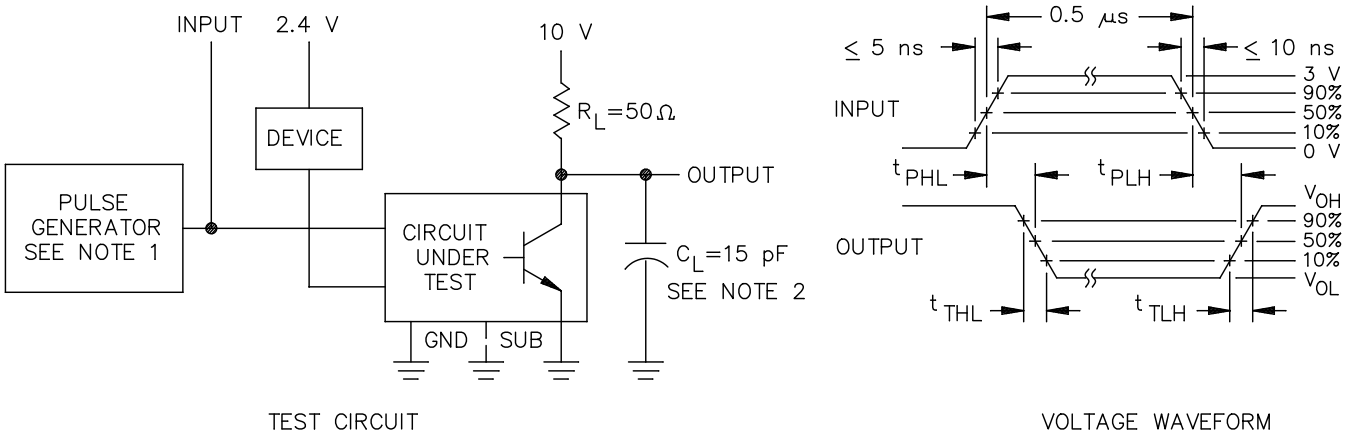


FIGURE 4. Logic diagram.

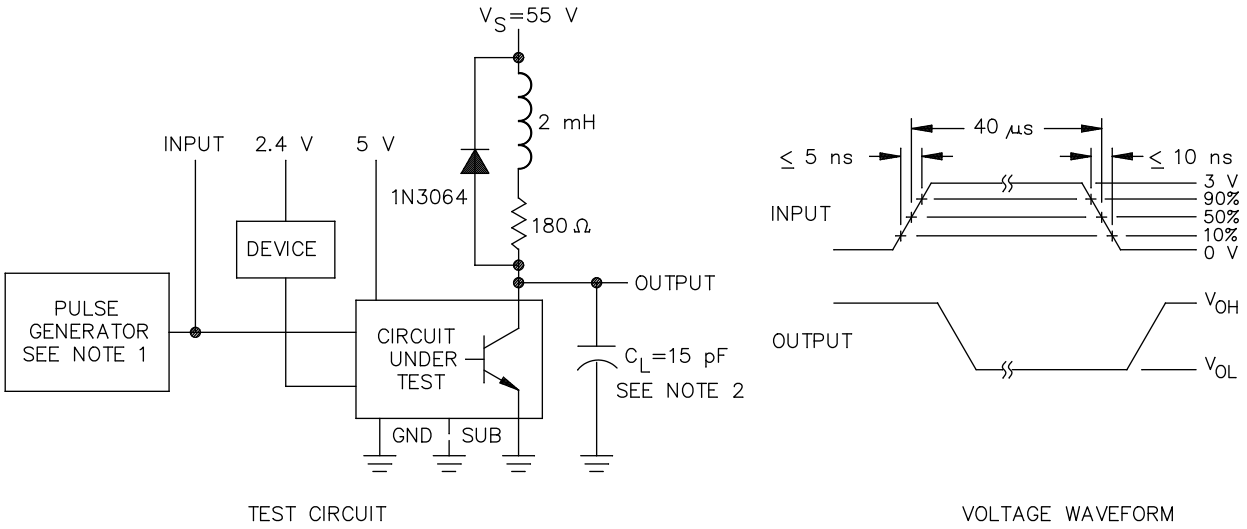
Switching times.



NOTES:

1. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω.
2. C_L includes probe and jig capacitance.

Latch up test.



NOTES:

1. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω.
2. C_L includes probe and jig capacitance.

FIGURE 5. Timing waveforms and test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Transportation mode and quantity	Top side marking	Vendor part number
V62/13618-01XE	01295	Tape of 75	65472	SN65472DEP
	01295	Reel of 2500	65472	SN65472DREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

3/ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493