REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Under figure 1, JEDEC standard MO-220-WEED has been updated to MO-220-WEED-2 along with dimensions b, D1/E1, and L1. Update document paragraphs to current requirements. - ro	18-12-05	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dla.mil/landandmaritime**
Original date of drawing YY-MM-DD 13-05-29	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, LOW NOISE, HIGH SPEED DIFFERENTIAL AMPLIFIER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/13615**
	REV **A**	**PAGE** 1 **OF** 17

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V111-18

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low noise, high speed differential amplifier microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13615	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADA4930-1-EP	Low noise, high speed differential amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-220-WEED-2	Lead frame chip scale

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_S) ..... 5.5 V
Power dissipation (P_D) at T_A = +105°C ..... 550 mW
Junction temperature range (T_J) ..... 150°C
Storage temperature range (T_{STG}) ..... -65°C to +125°C
Lead temperature (soldering, 10 seconds) ..... 300°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

1.4 Recommended operating conditions. 2/

Supply voltage range (V_S) ..... 3.3 V to 5 V
Operating free-air temperature range (T_A) ..... -55°C to +105°C

1.5 Thermal characteristics.

Thermal resistance, junction to ambient (θ_{JA}) ..... 81.6°C/W

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ V_S = 3.3 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance.							
-3 dB small signal bandwidth	SSBW	$V_{O,dm}$ = 0.1 V_{P-P}	+25°C	01	1430 typical		MHz
-3 dB large signal bandwidth	LSBW	$V_{O,dm}$ = 2 V_{P-P}	+25°C	01	887 typical		MHz
Bandwidth for 0.1 dB flatness		$V_{O,dm}$ = 0.1 V_{P-P}	+25°C	01	380 typical		MHz
Slew rate	SR	$V_{O,dm}$ = 2 V step, 25% to 75%	+25°C	01	2877 typical		V / μs
Settling time to 0.1%	t_S	$V_{O,dm}$ = 2 V step, R_L = 200 Ω	+25°C	01	6.3 typical		ns
Overdrive recovery time		G = 3, $V_{IN,dm}$ = 0.7 V_{P-P} pulse	+25°C	01	1.5 typical		ns
Noise / harmonic performance.							
Second harmonic distortion	HD2	$V_{O,dm}$ = 2 V_{P-P}, f_C = 10 MHz	-55°C to +105°C	01	-98 typical		dBc
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 30 MHz			-91 typical		
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 70 MHz			-79 typical		
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 100 MHz			-73 typical		
Third harmonic distortion	HD3	$V_{O,dm}$ = 2 V_{P-P}, f_C = 10 MHz	-55°C to +105°C	01	-97 typical		dBc
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 30 MHz			-88 typical		
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 70 MHz			-79 typical		
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 100 MHz			-73 typical		
Third order intermodulation distortion (IMD)		$V_{O,dm}$ = 1 V_{P-P} / tone, f_C = 70.05 MHz ±0.05 MHz	+25°C	01	91 typical		dBc
		$V_{O,dm}$ = 1 V_{P-P} / tone, f_C = 140.05 MHz ±0.05 MHz			86 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = 3.3 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Noise / harmonic performance - continued.							
Input voltage noise		f = 100 kHz	+25°C	01	1.15 typical		nV / $\sqrt{Hz}$
			-55°C to +105°C		1.2 typical		
Input current noise		f = 100 kHz	+25°C	01	3 typical		pA / $\sqrt{Hz}$
DC performance.							
Input offset voltage	V_{IO}	$V_{IP} = V_{IN} = V_{OCM}$ = 0 V, R_L = open circuit	-55°C to +105°C	01	-3.1	+3.1	mV
Input offset voltage drift	ΔV_{IO}		-55°C to +105°C	01	2.75 typical		µV / °C
Input bias current	I_{IB}		+25°C	01	-36	-16	µA
Input bias current drift	ΔI_{IB}		-55°C to +105°C	01	-0.05 typical		µA / °C
Input offset current	I_{IO}		+25°C	01	-1.8	+1.8	µA
Open loop gain		$R_F = R_G$ = 10 kΩ, ΔV_O = 0.5 V,	+25°C	01	64 typical		dB
		R_L = open circuit	-55°C to +105°C		61 typical		
Input characteristics.							
Input common mode voltage range			+25°C	01	0.3	1.2	V
Input resistance	RIN	Differential	+25°C	01	150 typical		kΩ
		Common mode			3 typical		MΩ

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = 3.3 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input characteristics – continued.							
Input capacitance	C_{IN}	Common mode	+25°C	01	1 typical		pF
Common mode rejection mode	CMRR	ΔV_{ICM} = 0.5 V dc;	+25°C	01		-77	dB
		$R_F = R_G$ = 10 kΩ, R_L = open circuit	-55°C to +105°C		-76 typical		
Output characteristics.							
Output voltage	V_{OUT}	Each single ended output,	+25°C	01	0.11	1.74	V
		$R_F = R_G$ = 10 kΩ	-55°C to +105°C			1.54	
Linear output current		Each single ended output, f = 1 MHz, THD ≤ 60 dBc	+25°C	01	30 typical		mA
Output balance error		f = 1 MHz	+25°C	01	55 typical		dB
3.3 V V_{OCM} to $V_{O,CM}$ performance.							
V_{OCM} dynamic performance.							
-3 dB bandwidth		$V_{O,CM}$ = 0.1 V_{P-P}	+25°C	01	745 typical		MHz
Slew rate	SR	$V_{O,CM}$ = 2 V_{P-P} , 25% to 75%	+25°C	01	828 typical		V / μs
V_{OCM} input characteristics.							
Input voltage range	V_{IN}		+25°C	01	0.8	1.1	V
Input resistance	R_{IN}		+25°C	01	7.0	10.3	kΩ
Input offset voltage	V_{IO}	$V_{OS,CM} = V_{O,CM} - V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 0 V	+25°C	01	-25	+31	mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = 3.3 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
3.3 V V_{OCM} to $V_{O,CM}$ performance – continued.							
V_{OCM} input characteristics continued.							
Input voltage noise		f = 100 kHz	+25°C	01	23.5 typical		nV / $\sqrt{Hz}$
Gain			+25°C	01	0.99	1.02	V / V
			-55°C to +105°C		1.01 typical		
Common mode rejection ratio		ΔV_{ICM} = 0.5 V dc;	+25°C	01		-77	dB
		R_F = R_G = 10 kΩ, R_L = open circuit	-55°C to +105°C		-76 typical		
3.3 V general performance.							
Power supply.							
Operating range			+25°C	01	3.3 typical		V
Quiescent current per amplifier		Enabled	+25°C	01	32	40	mA
		Enabled variation	-55°C to +105°C		81 typical		µA / °C
		Disabled	+25°C		0.44	2.35	mA
			-55°C to +105°C		2.4 typical		
Power supply rejection ratio	+PSRR	ΔV_{ICM} = 0.5 V dc;	+25°C	01		-70	dB
		R_F = R_G = 10 kΩ, R_L = open circuit	-55°C to +105°C		-68 typical		
	-PSRR	ΔV_{ICM} = 0.5 V dc;	+25°C			-76	
		R_F = R_G = 10 kΩ, R_L = open circuit	-55°C to +105°C		-77 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = 3.3 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
3.3 V general performance - continued.							
Power down ($\overline{PD}$).							
$\overline{PD}$ input voltage		Disabled	+25°C	01	< 0.8 typical		V
		Enabled			>1.3 typical		
Turn off time			+25°C	01	1 typical		µs
Turn on time			+25°C	01	12 typical		ns
$\overline{PD}$ pin bias current		Enabled, $\overline{PD}$ = 3.3 V	+25°C	01	0.09 typical		µA
		Disabled, $\overline{PD}$ = 0 V			97 typical		
Operating temperature range				01	-55	+105	°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = 5 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance.							
-3 dB small signal bandwidth	SSBW	$V_{O,dm}$ = 0.1 V_{P-P}	+25°C	01	1350 typical		MHz
-3 dB large signal bandwidth	LSBW	$V_{O,dm}$ = 2 V_{P-P}	+25°C	01	937 typical		MHz
Bandwidth for 0.1 dB flatness		$V_{O,dm}$ = 0.1 V_{P-P}	+25°C	01	369 typical		MHz
Slew rate	SR	$V_{O,dm}$ = 2 V step, 25% to 75%	+25°C	01	3400 typical		V / μs
Settling time to 0.1%	t_S	$V_{O,dm}$ = 2 V step, R_L = 200 Ω	+25°C	01	6 typical		ns
Overdrive recovery time		G = 3, $V_{IN,dm}$ = 0.7 V_{P-P} pulse	+25°C	01	1.5 typical		ns
Noise / harmonic performance.							
Second harmonic distortion	HD2	$V_{O,dm}$ = 2 V_{P-P}, f_C = 10 MHz	-55°C to +105°C	01	-104 typical		dBc
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 30 MHz			-91 typical		
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 70 MHz			-79 typical		
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 100 MHz			-73 typical		
Third harmonic distortion	HD3	$V_{O,dm}$ = 2 V_{P-P}, f_C = 10 MHz	-55°C to +105°C	01	-101 typical		dBc
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 30 MHz			-93 typical		
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 70 MHz			-82 typical		
		$V_{O,dm}$ = 2 V_{P-P}, f_C = 100 MHz			-75 typical		
Third order intermodulation distortion (IMD)		$V_{O,dm}$ = 1 V_{P-P} / tone, f_C = 70.05 MHz ±0.05 MHz	+25°C	01	94 typical		dBc
		$V_{O,dm}$ = 1 V_{P-P} / tone, f_C = 140.05 MHz ±0.05 MHz			90 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = 5 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Noise / harmonic performance - continued.							
Input voltage noise		f = 100 kHz	+25°C	01	1.2 typical		nV / $\sqrt{Hz}$
			-55°C to +105°C		1.3 typical		
Input current noise		f = 100 kHz	+25°C	01	2.8 typical		pA / $\sqrt{Hz}$
DC performance.							
Input offset voltage	V_{IO}	$V_{IP} = V_{IN} = V_{OCM}$ = 0 V, R_L = open circuit	-55°C to +105°C	01	-3.1	+3.1	mV
Input offset voltage drift	ΔV_{IO}		-55°C to +105°C	01	1.8 typical		µV / °C
Input bias current	I_{IB}		+25°C	01	-34	-15	µA
Input bias current drift	ΔI_{IB}		-55°C to +105°C	01	-0.05 typical		µA / °C
Input offset current	I_{IO}		+25°C	01	-0.82	+0.82	µA
Open loop gain		$R_F = R_G$ = 10 kΩ, ΔV_O = 1 V,	+25°C	01	64 typical		dB
		R_L = open circuit	-55°C to +105°C		61 typical		
Input characteristics.							
Input common mode voltage range			+25°C	01	0.3	2.8	V
Input resistance	R_{IN}	Differential	+25°C	01	150 typical		kΩ
		Common mode			3 typical		MΩ

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = 5 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input characteristics – continued.							
Input capacitance	C_{IN}	Common mode	+25°C	01	1 typical		pF
Common mode rejection mode	CMRR	ΔV_{ICM} = 1 V dc;	+25°C	01		-77	dB
		$R_F = R_G$ = 10 kΩ, R_L = open circuit	-55°C to +105°C		-76 typical		
Output characteristics.							
Output voltage	V_{OUT}	Each single ended output, $R_F = R_G$ = 10 kΩ	-55°C to +105°C	01	0.18	3.38	V
Linear output current		Each single ended output, f = 1 MHz, THD ≤ 60 dBc	+25°C	01	30 typical		mA
Output balance error		f = 1 MHz	+25°C	01	55 typical		dB
5 V V_{OCM} to $V_{O,CM}$ performance.							
V_{OCM} dynamic performance.							
-3 dB bandwidth		$V_{O,CM}$ = 0.1 V_{P-P}	+25°C	01	740 typical		MHz
Slew rate	SR	$V_{O,CM}$ = 2 V_{P-P} , 25% to 75%	+25°C	01	1224 typical		V / μs
V_{OCM} input characteristics.							
Input voltage range	V_{IN}		+25°C	01	0.5	2.3	V
Input resistance	R_{IN}		+25°C	01	7.0	10.2	kΩ
Input offset voltage	V_{IO}	$V_{OS,CM} = V_{O,CM} – V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 0 V	+25°C	01	-25	+15	mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = 5 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
5 V V_{OCM} to $V_{O,CM}$ performance – continued.							
V_{OCM} input characteristics - continued.							
Input voltage noise		f = 100 kHz	+25°C	01	23.5 typical		nV / $\sqrt{Hz}$
Gain			+25°C	01	0.99	1.02	V / V
			-55°C to +105°C		1 typical		
Common mode rejection ratio		ΔV_{OCM} = 1.5 V dc;	+25°C	01		-77	dB
		R_F = R_G = 10 kΩ, R_L = open circuit	-55°C to +105°C		-76 typical		
5 V general performance.							
Power supply.							
Operating range			+25°C	01	5 typical		V
Quiescent current per amplifier		Enabled	+25°C	01	31.1	38.4	mA
		Enabled variation	-55°C to +105°C		74.5 typical		µA / °C
		Disabled	+25°C		0.45	2.6	mA
			-55°C to +105°C		2.7 typical		
Power supply rejection ratio	+PSRR	ΔV_{ICM} = 1 V dc;	+25°C	01		-71	dB
		R_F = R_G = 10 kΩ, R_L = open circuit	-55°C to +105°C		-70 typical		
	-PSRR	ΔV_{ICM} = 1 V dc;	+25°C			-75	
		R_F = R_G = 10 kΩ, R_L = open circuit	-55°C to +105°C		-78 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = 5 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
5 V general performance.							
Power down ($\overline{PD}$).							
$\overline{PD}$ input voltage		Disabled	+25°C	01	< 2.5 typical		V
		Enabled			>3 typical		
Turn off time			+25°C	01	1 typical		µs
Turn on time			+25°C	01	12 typical		ns
$\overline{PD}$ pin bias current		Enabled, $\overline{PD}$ = 5 V	+25°C	01	0.09 typical		µA
		Disabled, $\overline{PD}$ = 0 V			97 typical		
Operating temperature range				01	-55	+105	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{ICM} = 0.9 V, V_{OCM} = 0.9 V, fixed resistance (R_F) = 301 Ω, gain resistance (R_G) = 301 Ω, load resistance ($R_{L,dm}$) = 1 kΩ, single ended input, differential output.

Case X

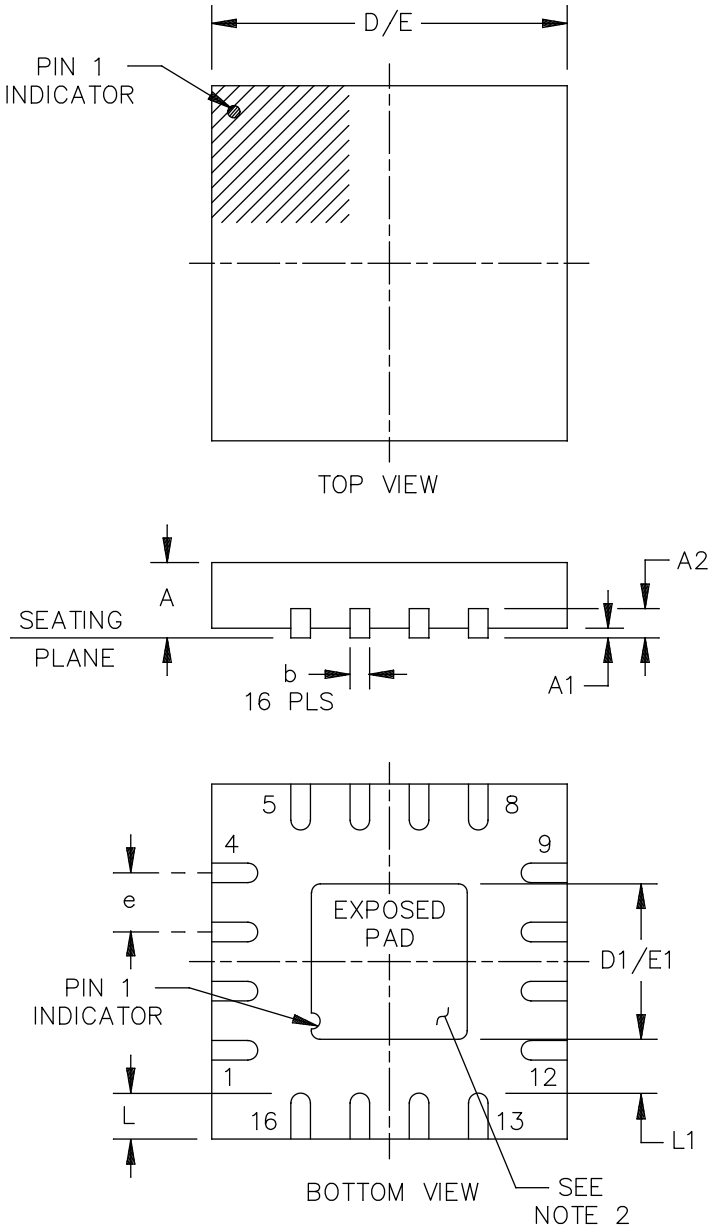

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13615
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Case X – continued.

Symbol	Dimensions					
	Inches			Millimeters		
	Min	Med	Max	Min	Med	Max
A	.027	.029	.031	0.70	0.75	0.80
A1	.0007	---	.001	0.02	---	0.05
A2	.007 REF			0.20 REF		
b	.007	.009	.012	0.20	0.25	0.32
D/E	.114	.118 SQ	.122	2.90	3.00 SQ	3.10
D1/E1	.062	.066 SQ	.070	1.60	1.70 SQ	1.80
e	.019 BSC			0.50 BSC		
L	.011	.015	.019	0.30	0.40	0.50
L1	.007	---	---	0.20	---	---

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The exposed pad should be connected to a thermal ground to dissipate heat. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
3. Falls within reference to JEDEC MO-220-WEED-2.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	-FB	Negative output for feedback component connection
2	+IN	Positive input summing node.
3	-IN	Negative input summing node.
4	+FB	Positive output for feedback component connection
5	$+V_S$	Positive supply voltage.
6	$+V_S$	Positive supply voltage.
7	$+V_S$	Positive supply voltage.
8	$+V_S$	Positive supply voltage.
9	V_{OCM}	Output common mode voltage.
10	+OUT	Positive output for load connection.
11	-OUT	Negative output for load connection.
12	$\overline{PD}$	Power down pin.
13	$-V_S$	Negative supply voltage.
14	$-V_S$	Negative supply voltage.
15	$-V_S$	Negative supply voltage.
16	$-V_S$	Negative supply voltage.
	EPAD	Exposed pad. The exposed pad is not electrically connected to the device. It is typically soldered to ground or a power plane on the printed circuit board (PCB) that is thermally conductive.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Transportation mode and order quantity	Vendor part number 2/
V62/13615-01XE	24355	Reel, 250	ADA4930-1SCPZ-EPR2
		Reel, 1,500	ADA4930-1SCPZ-EPR7
		Reel, 5,000	ADA4930-1SCPZ-EPRL

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Due to size limitation, the vendor will mark the part with "H2X" in lieu of the vendor part number.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland