

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update document paragraphs to current requirements. - ro	18-11-14	C. SAFFLE
B	Update figure 1 case outline package from MO-220 to a very thin profile quad flat no lead package (VQFN). Add typical limits to LIM, IGND, and VIT(PG) tests as specified under Table I. Update document to current requirements. - ro	24-02-08	J. ESCHMEYER



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B									
SHEET	1	2	3	4	5	6	7	8	9	10	11	12								

PMIC N/A Original date of drawing YY-MM-DD 13-06-12	PREPARED BY RICK OFFICER		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime	
	CHECKED BY RAJESH PITHADIA		TITLE MICROCIRCUIT, LINEAR, 2 AMP, FAST TRANSIENT, LOW DROPOUT VOLTAGE REGULATOR, MONOLITHIC SILICON	
	APPROVED BY CHARLES F. SAFFLE			
	SIZE A	CAGE CODE 16236	DWG NO. V62/13612	
	REV		B	PAGE 1 OF 12

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 2 amp, fast transient, low dropout voltage regulator microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/13612</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TPS7A7200-EP	2 amp, fast transient, low dropout voltage regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	MO-220	Plastic quad leadless flat pack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. ^{1/}

Supply voltage range:	
Supply voltage (IN), Power good (PG), Enable (EN)	-0.3 V to +7.0 V
Soft start (SS), Feedback (FB), Output voltage sense input (SNS),	
Regulated output (OUT)	-0.3 V to VIN + 0.3 V ^{2/}
50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V	-0.3 V to VOUT + 0.3 V
Current supply:	
OUT	Internally limited
PG (sink current into integrated circuit)	5 mA maximum
Junction temperature range (TJ)	-40°C to +150°C
Storage temperature range (TSTG)	-40°C to +150°C
Electrostatic discharge (ESD): ^{3/}	
Human body model (HBM)	2 kV
Charged device model (CDM)	500 V

^{1/} Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

^{2/} The absolute maximum rating is VIN + 0.3 V or +7.0 V, whichever is smaller.

^{3/} ESD testing is performed according to the respective JEDEC standard.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 2

1.4 Recommended operating conditions. 4/

Operating free-air temperature range (TA) -40°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient <u>5/</u>	θ_{JA}	35.7	°C/W
Thermal resistance, junction-to-case (top) <u>6/</u>	$\theta_{JC(TOP)}$	33.6	°C/W
Thermal resistance, junction-to-board <u>7/</u>	θ_{JB}	15.2	°C/W
Characterization parameter, junction-to-top <u>8/</u>	ψ_{JT}	0.4	°C/W
Characterization parameter, junction-to-board <u>9/</u>	ψ_{JB}	15.4	°C/W
Thermal resistance, junction-to-case (bottom) <u>10/</u>	$\theta_{JC(BOTTOM)}$	3.8	°C/W

- 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 5/ The thermal resistance, junction-to-ambient under natural convection is obtained in a simulation on a JEDEC standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- 6/ The thermal resistance, junction-to-case (top) is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- 7/ The thermal resistance, junction-to-board is obtained by simulating in an environment with a ring cold plate fixture to control the printed circuit board (PCB) temperature, as described in JESD51-8.
- 8/ Characterization parameter, junction-to-top (ψ_{JT}) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- 9/ Characterization parameter, junction-to-board (ψ_{JB}) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- 10/ The thermal resistance, junction-to-case (bottom) is obtained by simulating a cold plate test on the exposed thermal pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 3

2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE, SEMICONDUCTOR EQUIPMENT and MATERIALS INTERNATIONAL

ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available online at <https://www.ansi.org>.)

JEDEC Solid State Technology Association

- EIA/JESD 51-2a – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
- EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- EIA/JESD 51-8 – Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/ 3/ 4/ 5/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Input voltage range	V _{IN}		-40°C to +125°C	01	1.425	6.5	V
SS pin voltage	V _(SS)		+25°C	01	0.5 typical		V
Output voltage range	V _{OUT}	Adjustable with external feedback resistors	-40°C to +125°C	01	0.9	5.0	V
		Fixed with voltage setting pins			0.9	3.5	
Output voltage <u>6/ 7/</u> accuracy		Adjustable, 25 mA ≤ I _{OUT} ≤ 2 A	-40°C to +125°C	01	-2.0	+2.0	%
		Fixed, 25 mA ≤ I _{OUT} ≤ 2 A			-3.0	+3.0	
Line regulation	ΔV _{O(ΔV)}	I _{OUT} = 25 mA	+25°C	01	0.01 typical		%/V
Load regulation	ΔV _{O(ΔI_O)}	25 mA ≤ I _{OUT} ≤ 2 A	+25°C	01	0.1 typical		%/A
Dropout voltage <u>8/</u>	V _(DO)	V _{OUT} ≤ 3.3 V, I _{OUT} = 2 A, V _(FB) = GND	-40°C to +125°C	01		180	mV
		3.3 V < V _{OUT} , I _{OUT} = 2 A, V _(FB) = GND				470	
Output current limit	I _(LIM)	V _{OUT} forced at 0.9 x V _{OUT(TARGET)} , V _{IN} = 3.3 V, V _{OUT(TARGET)} = 0.9 V	-40°C to +125°C	01	2.4		A
					3.1 typical		
GND pin current	I _(GND)	Full load, I _{OUT} = 2 A	+25°C	01	2.6 typical		mA
		Minimum load, V _{IN} = 6.5 V, V _{OUT(TARGET)} = 0.9 V, I _{OUT} = 25 mA	-40°C to +125°C			4	mA
		Shutdown, PG = (open), V _{IN} = 6.5 V, V _(EN) < 0.5 V, V _{OUT(TARGET)} = 0.9 V				5	μA
		0.1 typical					
EN pin current	I _(EN)	V _{IN} = 6.5 V, V _(EN) = 0 V and 6.5 V	-40°C to +125°C	01		±0.1	μA
EN pin low level input voltage (disable device)	V _{IL(EN)}		-40°C to +125°C	01	0	0.5	V
EN pin high level input voltage (enable device)	V _{IH(EN)}		-40°C to +125°C	01	1.1	6.5	V

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 5

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/ 4/ 5/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
PG pin threshold	V _{IT(PG)}	For the direction PG↓ with decreasing V _{OUT}	-40°C to +125°C	01	0.85 x V _{OUT}	0.96 x V _{OUT}	V
					0.9 x V _{OUT} typical		
PG pin hysteresis	V _{hys(PG)}	For PG↑	+25°C	01	0.02 x V _{OUT} typical		V
PG pin low level output voltage	V _{OL(PG)}	V _{OUT} < V _{IT(PG)} , I _{PG} = -1 mA (current into device)	-40°C to +125°C	01		0.4	V
PG pin leakage current	I _{lkg(PG)}	V _{OUT} > V _{IT(PG)} , V(PG) = 6.5 V	-40°C to +125°C	01		1	μA
SS pin charging current	I(SS)	V(SS) = GND, V _{IN} = 3.3 V	-40°C to +125°C	01	3.5	7.2	μA
					5.1 typical		
Output noise voltage	V _n	BW = 100 Hz to 100 kHz, V _{IN} = 1.5 V, V _{OUT} = 1.2 V, I _{OUT} = 2 A	+25°C	01	40.65 typical		μV RMS
Thermal shutdown temperature	T _{sd}	Shutdown, temperature increasing		01	+160 typical		°C
		Reset, temperature decreasing			+140 typical		
Operating junction temperature	T _J			01	-40	+125	°C

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, $1.425\text{ V} \leq V_{IN} \leq 6.5\text{ V}$, $V_{IN} \geq V_{OUT}(\text{TARGET}) + 0.3\text{ V}$ or $V_{IN} \geq V_{OUT}(\text{TARGET}) + 0.5\text{ V}$.
When $V_{OUT} \leq 3.5\text{ V}$, $V_{IN} \geq (V_{OUT} + 0.3\text{ V})$ or 1.425 V , whichever is greater; when $V_{OUT} > 3.5\text{ V}$, $V_{IN} \geq (V_{OUT} + 0.5\text{ V})$.
V_{OUT}(TARGET) is the calculated target V_{OUT} value from the output voltage setting pins: 50 mV, 100 mV, 200 mV, 400 mV, 800 mV, and 1.6 V in fixed configuration, or the expected V_{OUT} value set by external feedback resistors in adjustable configuration.
- 3/ Unless otherwise specified, OUT connected to 50 Ω to GND. This 50 Ω load is disconnected when the test conditions specify an I_{OUT} value.
- 4/ Unless otherwise specified, V_{EN} = 1.1 V, C_{OUT} = 10 μF, C_{SS} = 10 nF, and C_{FF} = 0 pF.
C_{FF} is the capacitor between FB pin and OUT.
- 5/ Unless otherwise specified, PG pin pulled up to V_{IN} with 100 kΩ, $27\text{ k}\Omega \leq R_2 \leq 33\text{ k}\Omega$ for adjustable configuration.
R₂ is the bottom side of the feedback resistor between the FB pin and OUT.
- 6/ When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
- 7/ The device is not tested at V_{OUT} = 0.9, $2.7 \leq V_{IN} \leq 6.5\text{ V}$, and $500\text{ mA} \leq I_{OUT} \leq 2\text{ A}$ because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package.
- 8/ V(DO) is not defined for output voltage settings below 1.2 V.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 6

Case X

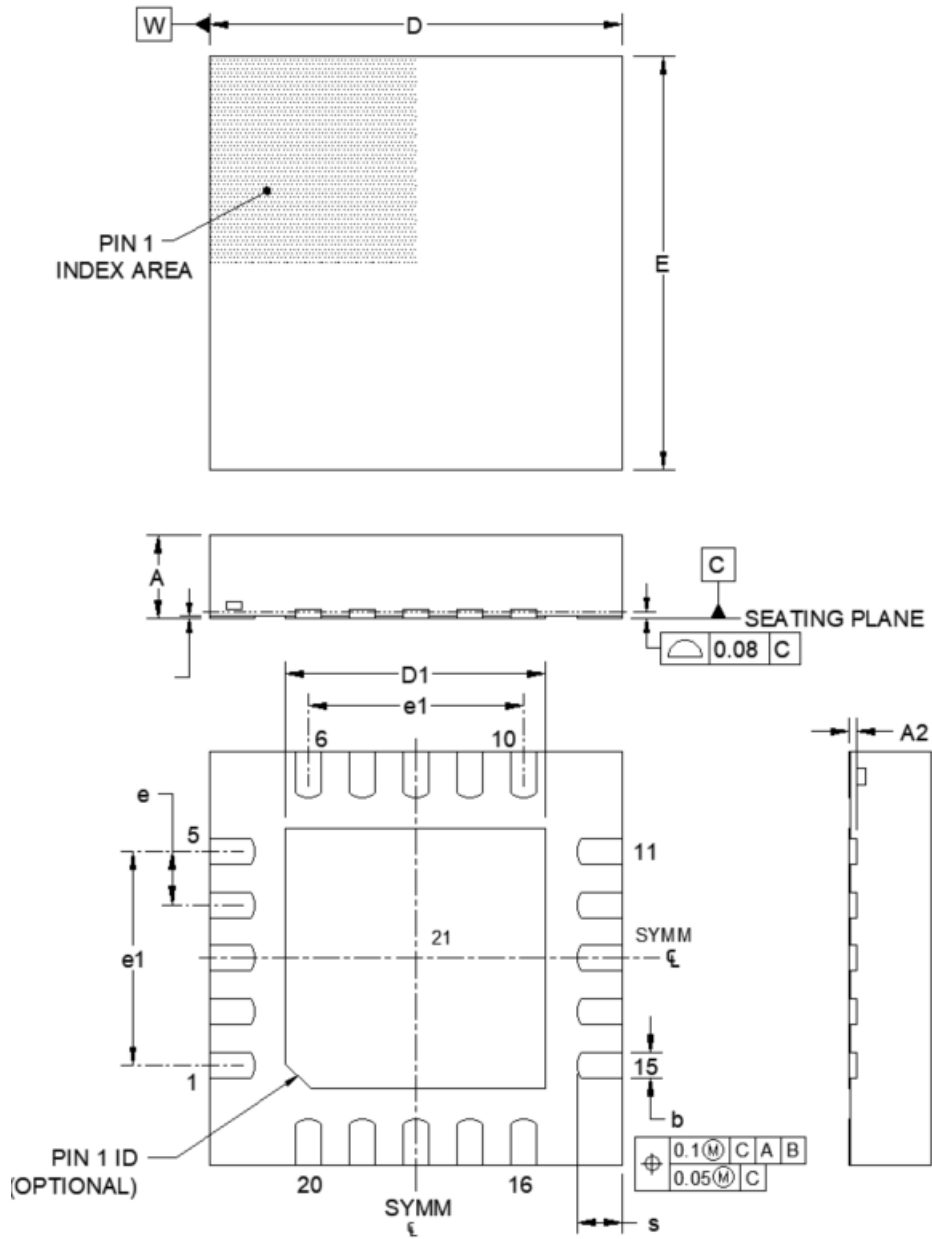


FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 7

Case X - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.039	---	1.0
A1	.000	.002	0.00	0.05
A2	.004 TYP		0.1 TYP	
b	.010	.014	0.26	0.36
D	.193	.201	4.9	5.1
D1	.120	.128	3.05	3.25
E	.193	.201	4.9	5.1
e	.026 BSC		0.65 BSC	
e1	.102 BSC		2.6 BSC	
s	.018	.025	0.45	0.65

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

FIGURE 1. Case outline - Continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 8

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUT
2	SNS
3	FB
4	PG
5	50 mV
6	100 mV
7	200 mV
8	GND
9	400 mV
10	800 mV
11	1.6 V
12	NC
13	SS
14	EN
15	IN
16	IN
17	IN
18	GND
19	OUT
20	OUT

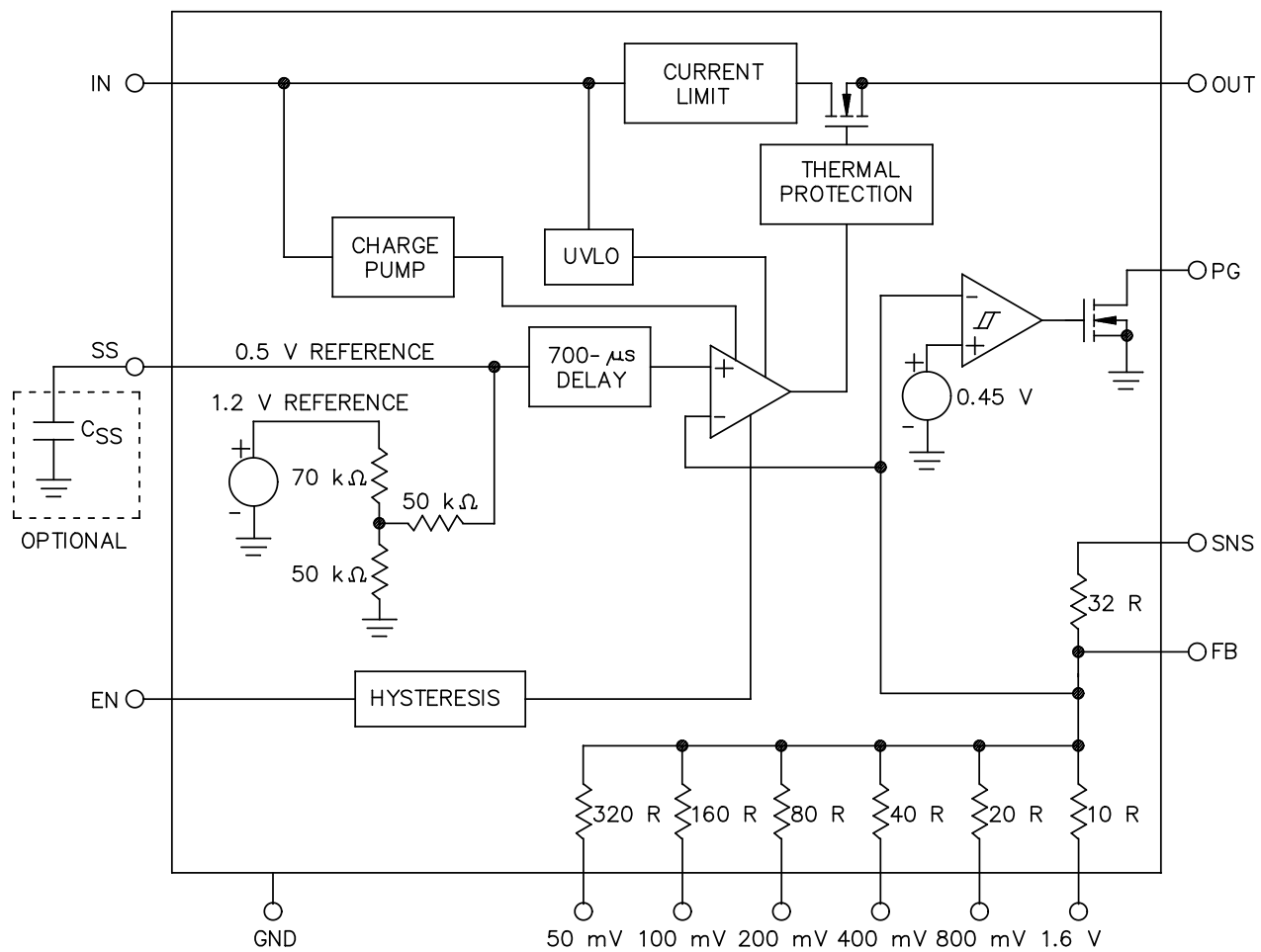
FIGURE 2. Terminal connections.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 9

Terminal symbol	Description
50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V	Output voltage setting pins. These pins should be connected to ground or left floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) when not in use. See the user configurable output voltage section in the manufacturer's datasheet for more details.
EN	Enable pin. Driving this pin to logic enables the device; driving the pin to logic low disables the device. See the enable and shutdown the device section in the manufacturer's datasheet for more details.
FB	Output voltage feedback pin. Connected to the error amplifier. See user configurable output voltage and traditional adjustable configuration section in the manufacturer's datasheet for more details. A 220 μ F ceramic capacitor from FB pin to OUT is highly recommended.
GND	Ground pin.
IN	Unregulated supply voltage pin. It is recommended to connect an input capacitor to this pin. See input capacitor requirements section in the manufacturer's datasheet for more details.
NC	Not internally connected. The NC pin is not connected to any electrical node. It is strongly recommended to connect this pin and the thermal pad to a large area ground plane. See the power dissipation section in the manufacturer's datasheet for more details.
OUT	Regulated output pin. A 4.7 μ F or larger capacitance is required for stability. See output capacitor requirements section in the manufacturer's datasheet for more details.
PG	Active high power good pin. An open drain output that indicates when the output voltage reaches 90% of the target. See power good section in the manufacturer's datasheet for more details.
SNS	Output voltage sense input pin. See the user configurable output voltage and traditional adjustable configuration section in the manufacturer's datasheet for more details.
SS	Soft start pin. Leaving this pin open provides soft start of the default setting. Connecting an external capacitor between this pin and the ground enables the soft start function by forming an RC delay circuit in combination with integrated resistance on the silicon. See soft start section in the manufacturer's datasheet for more details.
Thermal pad	It is strongly recommended to connect the thermal pad to a large area ground plane. If available, connect an electrically floating, dedicated thermal plane to the thermal pad as well.

FIGURE 2. Terminal connections - Continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 10



NOTE: 320R = 1.024 MΩ (which is, 1R = 3.2 kΩ).

FIGURE 3. Block diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 11

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/ 2/ 3/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/13612-01XE	01295	SJK	TPS7A7200QRGWREP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer’s data sheet.
- 3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/13612
		REV B	PAGE 12