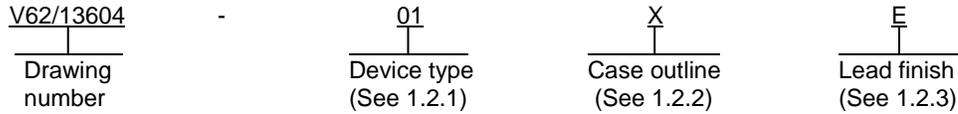


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 2.2 V to 4 V, 14 A output synchronous buck PWM switcher with integrated FETs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TPS54010-EP	2.2 V to 4 V, 14 A output synchronous buck PWM switcher with integrated FETs

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	28	JEDEC MO-153	Plastic Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Input voltage range, (V _I):	
SS/ENA, SYNC	-0.3 V to 7 V
RT	-0.3 V to 6 V
VSENSE	-0.3 V to 4 V
PVIN, VIN	-0.3 V to 4.5 V
BOOT	-0.3 V to 10 V
Output voltage range, (V _O):	
VBIAS, COMP, PWRGD	-0.3 V to 7 V
PH	-0.6 to 6 V
Source current, (V _O):	
PH	internally limited,
COMP, VBIAS	6 mA
Sink current, (I _S):	
PH	25 A
COMP	6 mA
SS/ENA, PWRGD	10 mA
Voltage differential , AGND to PGND	±0.3 V
Junction temperature range, (T _J):	-55°C to +150°C
Storage temperature range, (T _{stg})	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	300°C
Electrostatic Discharge (ESD) ratings:	
Human body model (HBM)	1.5 kV
CDM	750 V

1.4 Recommended operating conditions. 2/

Input voltage, (V _{IN}).....	3 V to 4 V
Power input voltage, (PVIN)	2.2 V to 4 V
Operating junction temperature	-55°C to +125°C

- 1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- 2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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1.5 Thermal characteristics.

Thermal metric <u>3/</u>	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} <u>4/</u>	30.5	°C/W
Junction to case (top) thermal resistance, θ_{JcTop} <u>5/</u>	13.5	
Junction to board thermal resistance, θ_{JB} <u>6/</u>	11.6	
Junction to top characterization parameter, Ψ_{JT} <u>7/</u>	0.4	
Junction to board characterization parameter, Ψ_{JB} <u>8/</u>	11.4	
Junction to case (bottom) thermal resistance, θ_{Jcbot} <u>9/</u>	0.9	

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).
- JESD51-2a – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-8 – Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

- ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Applications for copies should be addressed to the American National Standards Institute, Semiconductor Equipment and Materials International, 1819 L Street, NW, 6 th floor, Washington, DC 20036 or online at <http://www.ansi.org>)

-
- 3/ For more information about traditional and new thermal metrics, see manufacturer data.
 - 4/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.
 - 5/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
 - 6/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
 - 7/ The junction to top characterization parameter, Ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
 - 8/ The junction to board characterization parameter, Ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
 - 9/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Application circuit, 2.5 V to 1.5 V. The application circuit, 2.5 V to 1.5 V shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Supply voltage, VIN						
Input voltage	V _I		3		4	V
Supply voltage range	PVIN	Output = 1.8 V	2.2		4	
Quiescent current	VIN	f _s = 350 kHz, RT open, PH pin open, PVIN = 3.5 V, SYNC = 0 V		6.3	10	mA
		f _s = 550 kHz, RT open, PH pin open, PVIN = 3.5 V, SYNC ≥ 2.5 V		8.3	13	
		Shutdown, SS/EA = 0 V, PVIN = 2.5 V		1	1.4	
	PVIN	f _s = 350 kHz, RT open, PH pin open, PVIN = 3.3 V, SYNC = 0 V		6	8	mA
		f _s = 550 kHz, RT open, PH pin open, PVIN = 3.5 V, SYNC ≥ 2.5 V, VIN = 3.3 V		6	10	
		Shutdown, SS/EA = 0 V, VIN = 3.3 V		<140		
Under voltage lockout (VIN)						
Start threshold voltage	UVLO			2.95	3	V
Stop threshold voltage			2.7	2.8		
Hysteresis voltage				0.11		
Rising and falling edge deglitch 3/				2.5		
Bias voltage						
Output voltage	VBIAS	I _(VBIAS) = 0	2.7	2.8	2.95	V
Output current 4/					100	μA
Cumulative reference						
Accuracy	V _{ref}		0.879	0.891	0.903	V
Regulation						
Line regulation 3/ 5/		I _L = 7 A, f _s = 350 kHz, T _J = 85°C		0.05		%/V
Load regulation 3/ 5/		I _L = 0 A to 14 A, f _s = 350 kHz, T _J = 85°C PVIN = 2.5 V, VIN = 3.3 V		0.013		%/A
Oscillator						
Internally set – free running frequency		RT open 3/, SYNC ≤ 0.8 V	225	350	455	kHz
		RT open 3/, SYNC ≥ 2.5 V	435	550	660	
Externally set – free running frequency range		RT = 180 kΩ (1% resistor to AGND) 3/	252	280	308	
		RT = 100 kΩ (1% resistor to AGND)	432	500	540	
		RT = 68 kΩ (1% resistor to AGND) 3/	663	700	762	
High level threshold voltage, SYNC			2.5			V
Low level threshold voltage, SYNC					0.8	V
Pulse duration, SYNC 3/			50			ns
Frequency range, SYNC			300		700	kHz
Ramp valley 4/				0.75		V
Ramp amplitude (peak-to-peak) 4/				1		V
Minimum controllable on time 4/					200	ns
Maximum duty circle 4/			90%			

See footnote at end of table.

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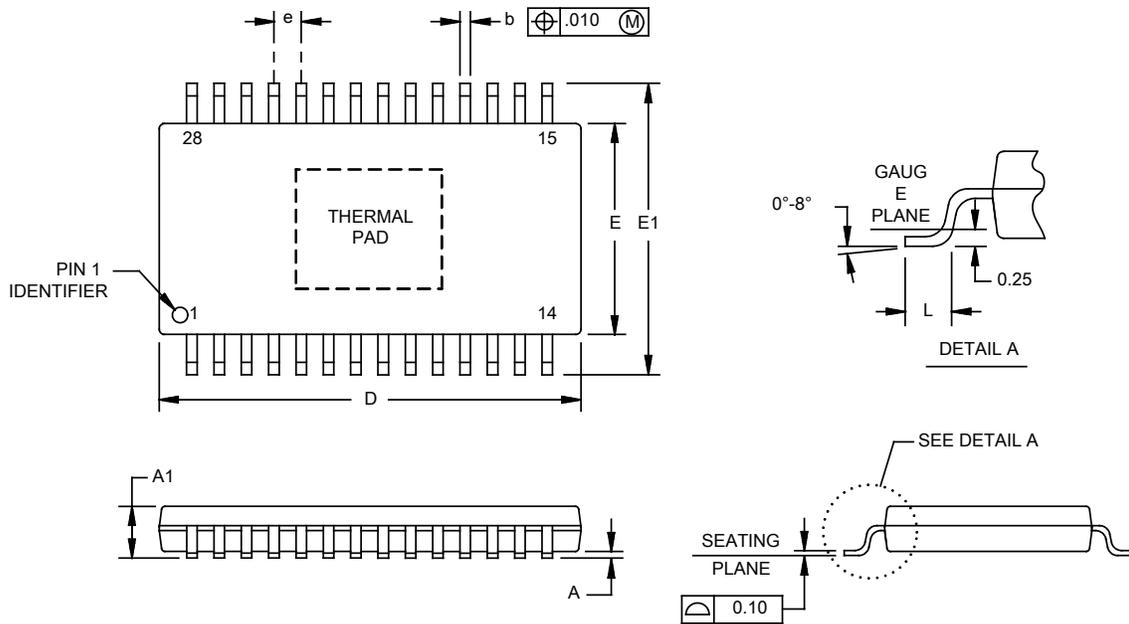
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Error amplifier						
Error amplifier open loop voltage gain		1 kΩ COMP to AGND <u>3/</u>	90	110		dB
Error amplifier unity gain bandwidth		Parallel 10 kΩ, 160 pF COMP to AGND <u>3/</u>	3	5		MHz
Error amplifier common mode input voltage range		Powered by internal LDO <u>3/</u>	0		VBIAS	V
Input bias current, VSENSE		VSENSE = V _{ref}		60	300	nA
Output voltage slew rate (symmetric), COMP				1.4		V/μs
PWM comparator						
PWM comparator propagation delay time, PWM comparator input to PH (excluding deadtime)		10 mV overdrive <u>3/</u>		70	85	ns
Slow-Start/Enable						
Enable threshold voltage, SS/ENA			0.82	1.2	1.4	V
Enable hysteresis voltage, SS/ENA <u>3/</u>				0.03		V
Falling edge deglitch, SS/ENA				2.5		μs
Internal slow start time			2.1	3.35	4.1	ms
Charge current, SS/ENA		SS/ENA = 0 V	2	5	8.3	μA
Discharge current, SS/ENA		SS/ENA = 0.2 V, VBIN = 2.7 V, PVIN = 2.5 V	1.3	2.3	4	mA
Power good						
Power good threshold voltage		VSENSE falling		93		%V _{ref}
Power good hysteresis voltage <u>3/</u>				3		%V _{ref}
Power good falling edge deglitch <u>3/</u>				35		μs
Output saturation voltage, PWRGD		I _(sink) = 2.5 mA		0.18	0.3	V
Leakage current, PWRGD		VIN = 3.3 V, PVIN = 2.5 V			1	μA
Current limit						
Current limit		VIN = 3.3 V, PVIN = 2.5 V <u>3/</u> , Output shorted	14.5	21		A
Current limit leading edge blanking time <u>3/</u>				100		ns
Current limit total response time <u>3/</u>				200		ns
Thermal shutdown						
Thermal shutdown trip point <u>3/</u>			135	165		°C
Thermal shutdown hysteresis <u>3/</u>				10		°C
Output power MOSFETS						
Power MOSFET switches	r _{DS(on)}	VIN = 3 V, PVIN = 2.5 V		8	21	mΩ
		VIN = 3.6 V, PVIN = 2.5 V		8	18	

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ T_J = -55°C to 125°C, VIN = 3 V to 4 V, PVIN = 2.2 V to 4 V (unless otherwise noted).
- 3/ Specified by design from -40°C to 125°C.
- 4/ Static resistive loads only.
- 5/ Specified by the circuit used in FIGURE 5.

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A1		1.20	E	4.30	4.50
A	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 BSC	
D	9.60	9.80	L	0.50	0.75

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
4. This package is designed to be soldered to a thermal pad on the board. Refer to manufacturer, Powerpad Thermally Enhanced Package, for information regarding recommended board layout.
5. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
6. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

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Case outline X							
Terminal number	Terminal symbol						
1	AGND	8	PH	15	PGND	22	PVIN
2	VSENSE	9	PH	16	PGND	23	PVIN
3	COMP	10	PH	17	PGND	24	VIN
4	PWRGD	11	PH	18	PGND	25	VBIAS
5	BOOT	12	PH	19	PGND	26	SS/ENA
6	PH	13	PH	20	PVIN	27	SYNC
7	PH	14	PH	21	PVIN	28	RT

FIGURE 2. Terminal connections.

Terminal Name	Terminal number	Description
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, and RT resistor. If using PowerPAD, connect it to AGND. See the Application information in manufacturer data for more details.
BOOT	5	Bootstrap output. 0.022 μ F to 0.1 μ F low-ESR capacitor connected from BOOT to PH generates floating drive for the high side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE.
PGND	15, 16, 17, 18, 19	Power ground. High current return for the low side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6 – 14	Phase output. Junction of the internal high side and low side power MOSFETs, and output inductor.
PVIN	20, 21, 22, 23	Input supply for the power MOSFET switches and internal bias regulator. Bypass the PVIN pins to the PGND pins close to device package with a high quality, low ESR 10 μ F ceramic capacitor.
PWRGD	4	Power good open drain output. High when VSENSE > 90% V_{ref} , otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s .
SS/ENA	26	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	27	Synchronization input. data function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low-ESR 0.1 μ F to 1.0 μ F ceramic capacitor.
VIN	24	Input supply for the internal control circuits. Bypass the VIN pin to the PGND pins close to device package with a high quality, low ESR 1 μ F ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

FIGURE 3. Terminal function.

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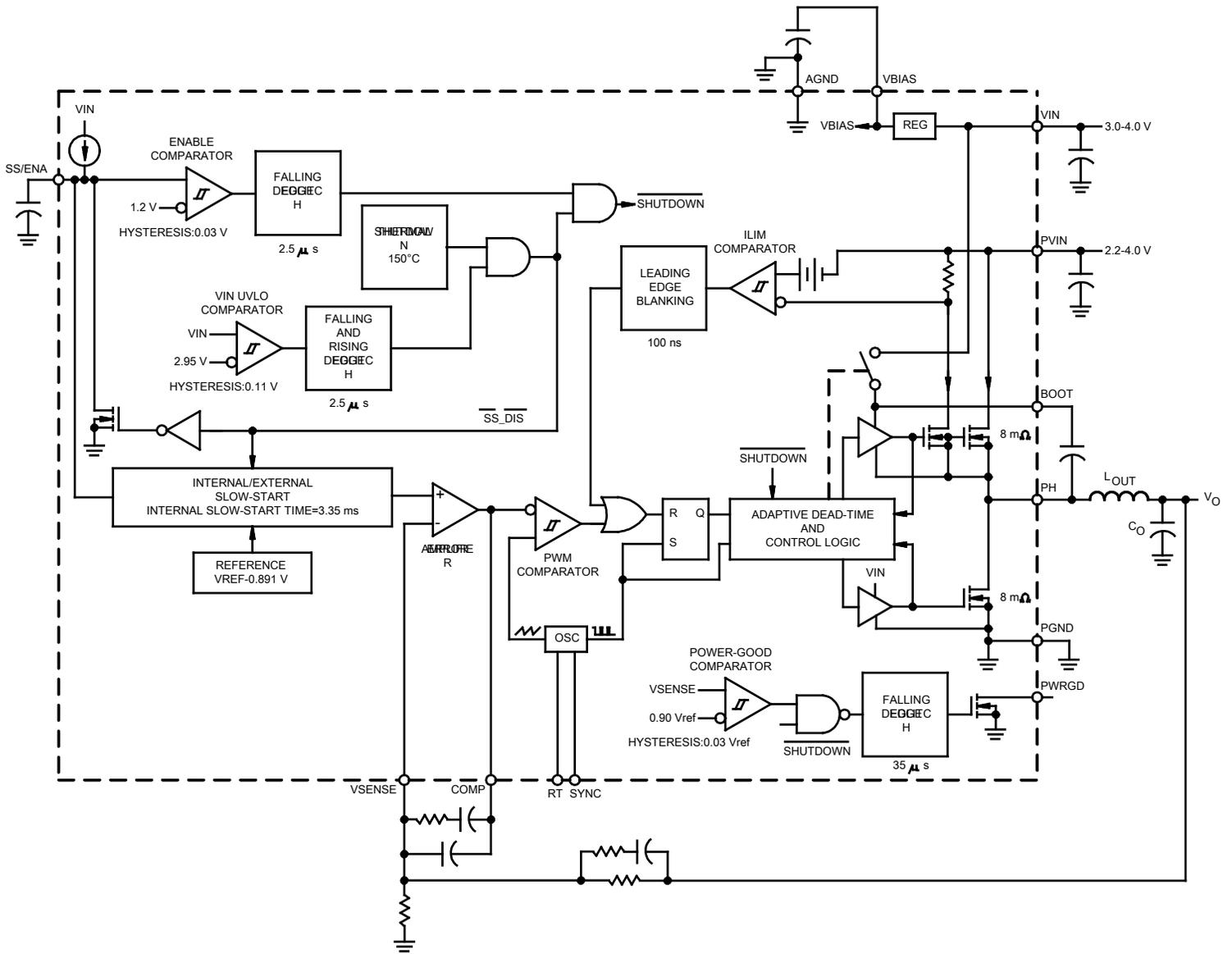


FIGURE 4. Functional block diagram.

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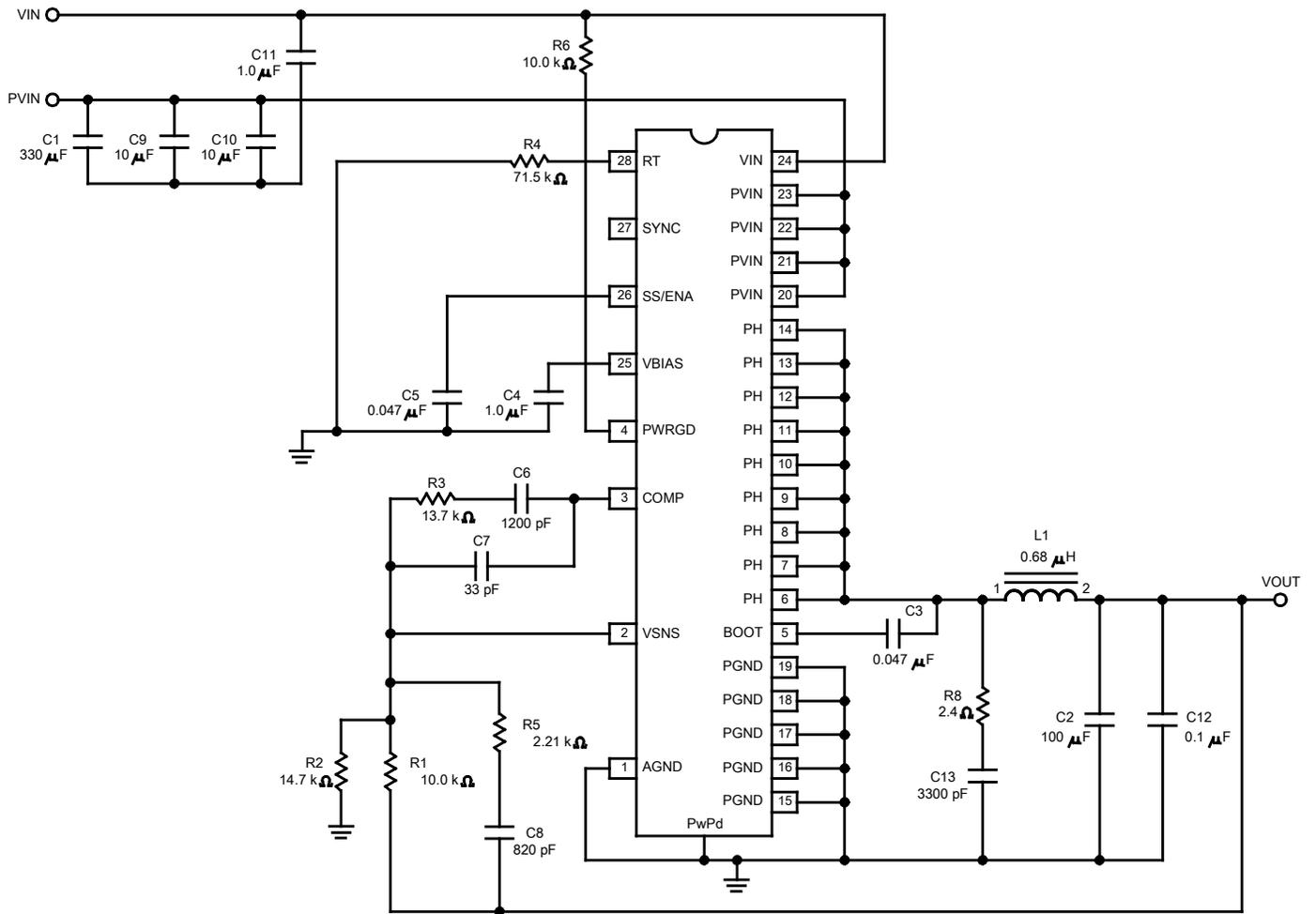


FIGURE 5. Application circuit, 2.5 V to 1.5 V.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Transport media	Vendor part number
V62/13604-01XE	01295	Tape and reel	TPS54010MPWPREP
		Tube	TPS54010MPWPEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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